TI Designs

4-GHz Clock Reference Design for 12-Bit High-Speed ADCs in Digital Oscilloscopes and Wireless Testers

Description

The TIDA-01015 is a clocking solution reference design for high-speed direct RF sampling GSPS ADCs. This TI Design showcases the significance of the sampling clock to achieve high SNR for second Nyquist zone input signal frequencies. The ADC12J4000 device is a 12-bit, 4-GSPS RF sampling ADC with a 3-dB input bandwidth of 3.2 GHz capable of capturing signals up to 4 GHz. This design highlights a clocking solution for the ADC12J4000 using TRF3765 to achieve high SNR performance at high input frequencies used in applications such as digital storage oscilloscopes (DSO) and wireless testers.

Features

- 12-Bit, 4-GSPS RF Sampling ADC Clocking Solution
- Up to 4-GHz Input Signal Capture Capability
- JESD204B Compliant Low-Phase Noise Clocking Solution for RF Sampling ADC

Applications

- Oscilloscopes
- Wireless Communication Testers
- Phased Array Radar
- Software Defined Radio

Resources

TIDA-01015	Design Folder
ADC12J4000EVM	Tool Folder
ADC12J4000	Product Folder
TRF3765	Product Folder
LMK04828	Product Folder
TSW14J56EVM	Tool Folder

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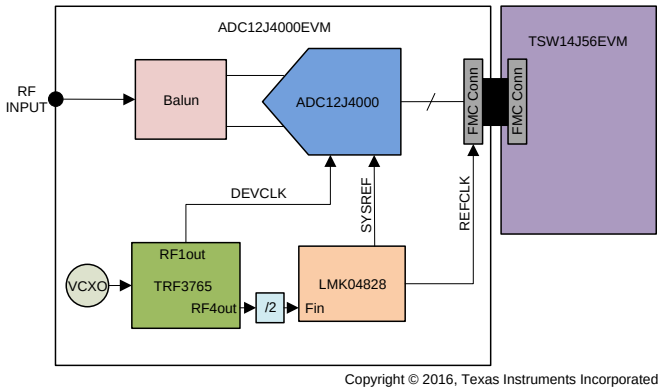

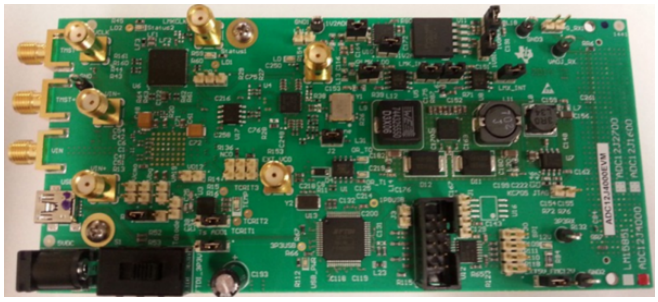

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1 System Overview

1.1 System Description

RF sampling ADCs are capable of capturing and digitizing RF signals higher than the sampling frequency. A high-speed GSPS RF sampling ADC requires a low-noise clocking solution to achieve high SNR. This TI Design focuses on the clocking solution for high-speed GSPS ADCs used in applications such as DSO, wireless testers, radar, and so on. In this TI Design, the TRF3765 RF synthesizer is used as a sampling clock source for the ADC12J4000. The TRF3765 is capable of generating clock frequencies up to 4.8 GHz and the ADC12J4000 is a 12-bit, 4-GSPS wideband ADC.

In this solution, the TRF3765 receives a 100-MHz VCXO reference signal and generates the ADC12J4000's DEVCLK (sampling clock). The TRF3765 is also used after being divided to clock the LMK04828, which is in clock distribution mode to generate SYSREF for the ADC and other clocks required for the JESD204B interface between the ADC and the FPGA.

Oscilloscopes require a wide bandwidth analog front-end (AFE). The ADC12J4000 ADC is well suited for these requirements. The clocking solution described in this TI Design provides an optimum solution for clocking the ADC12J4000 to achieve wide bandwidth and high SNR.

Wireless tester equipment requires high dynamic range and wide receiver bandwidth for 3G and later wireless standards. The ADC12J4000 ADC is well suited for these requirements. The clocking solution described in this TI Design provides an optimum solution for clocking the ADC12J4000 to achieve both high dynamic range and wide receiver bandwidth for wireless tester applications.

A radar end application needs high dynamic range, wide receiver bandwidth, and low latency. The signal chain solution based on the ADC12J4000, TRF3765, and LMK04828 helps to achieve optimum performance for radar applications.

RF-sampling software defined radio (SDR) technology needs high dynamic range, highly re-configurable receiver bandwidth, and wide input frequency range. This TI Design can meet most of the requirements of the high-performance SDRs in terms of dynamic range and re-configurability.

1.2 Key System Specifications

The objective of this TI Design is to study the TRF3675-LMK04828 clocking solution performance when used in within an ADC12J4000 signal chain. The design focuses on achieving high SNR for input signal frequencies in the second Nyquist zone. The input balun and passives were modified to enhance the input frequency range up to 4 GHz. Table 1 lists the key system level specifications for the signal chain from the clocking solution perspective. SNR is specified after considering the impact of the balun and other elements in the ADC12J4000EVM.

Table 1. Key System Level Specifications

PARAMETER	SPECIFICATIONS	CONDITIONS
Signal-to-noise ratio (SNR in dBFS)	55.0	350-MHz input signal
	54.8	600-MHz input signal
	52.0	900-MHz input signal
	51.2	1500-MHz input signal
	48.7	2400-MHz input signal
	48.5	2700-MHz input signal
	45.0	3700-MHz input signal

1.3 Block Diagram

The block diagram of the clocking solution for ADC12J4000EVM and data capture using the TSW14J56EVM are shown in Figure 1. The ADC12J4000EVM signal chain contains a balun to convert the single-ended input signal to differential and is provided to the ADC inputs.

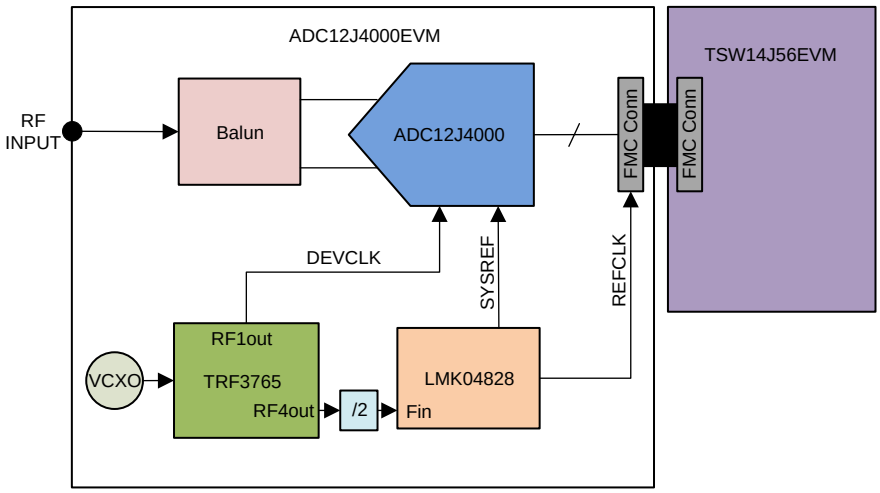

Figure 1. Block Diagram of ADC12J4000EVM and TSW14J56EVM Test Setup

1.4 Highlighted Products

1.4.1 ADC12J4000

The ADC12J4000 is a wideband sampling high speed ADC with JESD204B interface. It includes a 12-bit, 4-GSPS ADC with integrated DDC with programmable NCO and decimation settings (including an un-decimated 12-bit ADC output). It has a 3-dB input bandwidth of 3.2 GHz and is usable up to 3 GHz and beyond. The device input is buffered with an on-chip differential termination of 100 Ω.

1.4.2 TRF3765

The TRF3765 is a wideband integer-N and Fractional-N frequency synthesizer with an integrated, wideband voltage-controlled oscillator (VCO). The TRF3765 can generate continuous frequency coverage from 300 MHz to 4.8 GHz using the programmable output dividers.

1.4.3 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator. The device receives a divided frequency from the TRF3765 and operates in clock distribution mode. The LMK04828 supplies the SYSREF clock to the ADC and other clocks for the JESD204B FPGA interface.

2 Getting Started Hardware and Software

2.1 Hardware Configuration

2.1.1 ADC12J4000EVM Setup

Figure 2 shows the block diagram for the setup of the ADC12J4000EVM. Follow the ADC12J4000EVM user's guide[1] (SLAU551) for the ADC12J4000EVM hardware setup procedure. The ADC12J4000EVM has both internal as well as external options for clocking the ADC. Selecting the DEVCLK is based on the placement of capacitors on the shared pads. In external clock mode, connect a signal generator set for 4 GHz to the external clock input (DEVCLK).

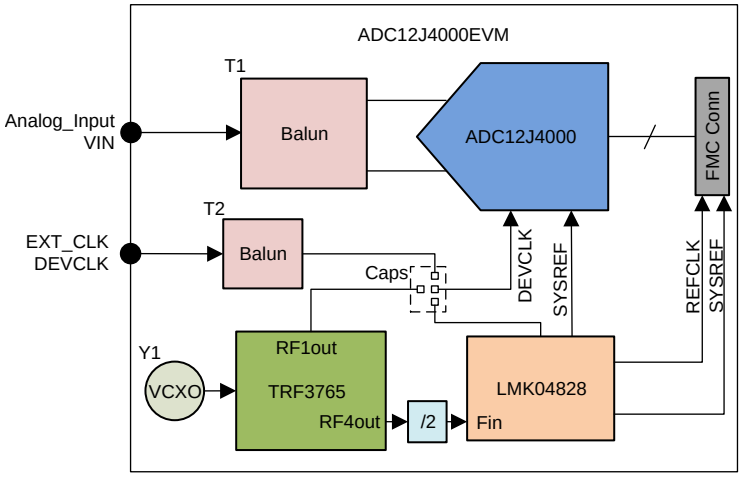

Figure 2. Block Diagram of ADC12J4000EVM

On the original EVM, the balun T1 supports an input frequency up to 3 GHz. In this TI Design, the balun was replaced with the BD2040J50100AHF to support frequencies up to 4 GHz.

2.1.2 TSW14J56EVM Setup

Follow the TSW14J56EVM user's guide[2] (SLWU086) for the TSW14J56EVM hardware setup procedure.

2.2 Software Configuration

2.2.1 ADC12J4000EVM Programming

Follow the ADC12J4000EVM user's guide[1] (SLAU551) to load the configuration files for ADC and clocks. The ADC12J4000EVM is put into bypass mode to use the full Nyquist zone of the device. The EVM is setup in onboard clock source selection mode, select a sampling frequency of 4000 Msps and click *Program Clocks and ADC*. Follow the ADC12J4000EVM user's guide for changing the onboard sampling frequency to a predefined frequency range.

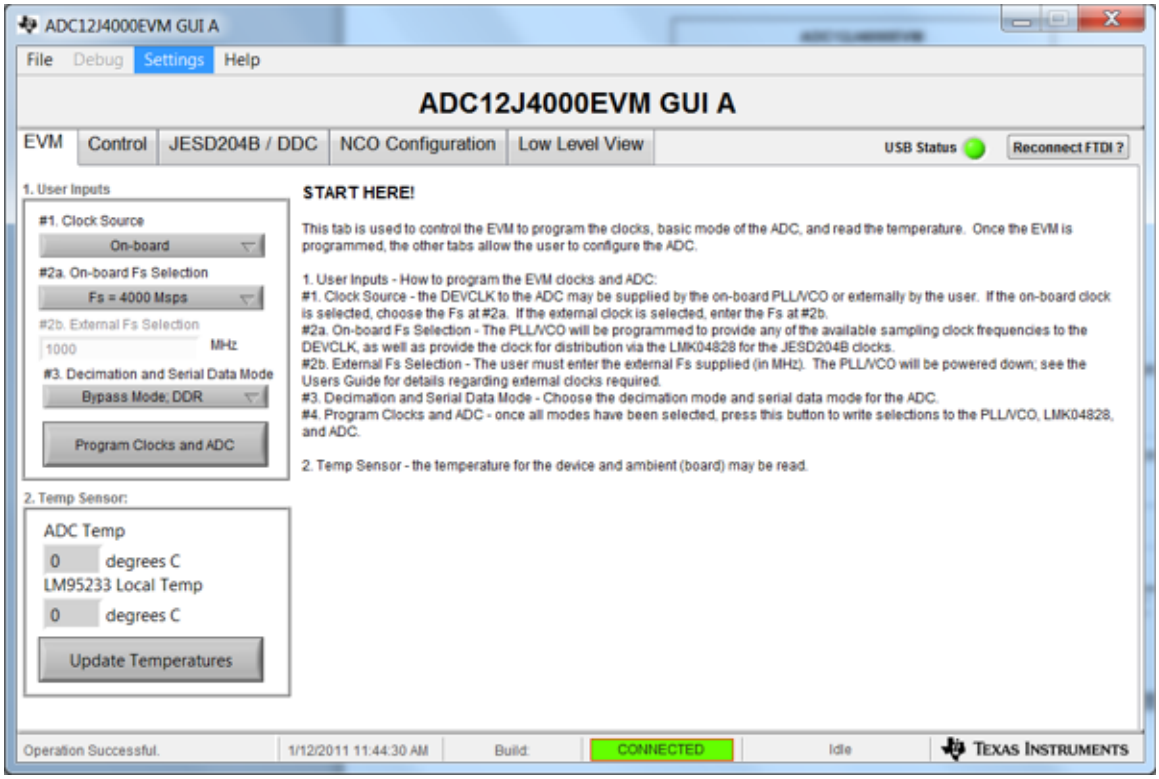

Figure 3. ADC12J4000EVM Programming

2.2.2 HSDC Pro Setup

The HSDC Pro software interfaces with the TSW14J56 to capture and analyze the digital data from the ADC12J4000. Follow the TSW14J56EVM user's guide[2] (SLWU086) for HSDC Pro setup and to capture and analyze the data.

3 Testing and Results

3.1 Test Setup

The ADC12J4000EVM connects to the TSW14J56EVM capture card, which is interfaced by HSDC Pro software to capture and analyze the data. A low-noise signal generator generates the required single-tone signal. A band-pass filter (BPF) suppresses the signal-generator harmonics. Balun T1 is replaced with the BD2040J50100AHF to enhance the input frequency range up to 4 GHz. In this TI Design, SNR measurements were performed at various frequencies with and without the clock BPF and measured results are tabulated in Section 3.2.

3.1.1 Internal Clock Input

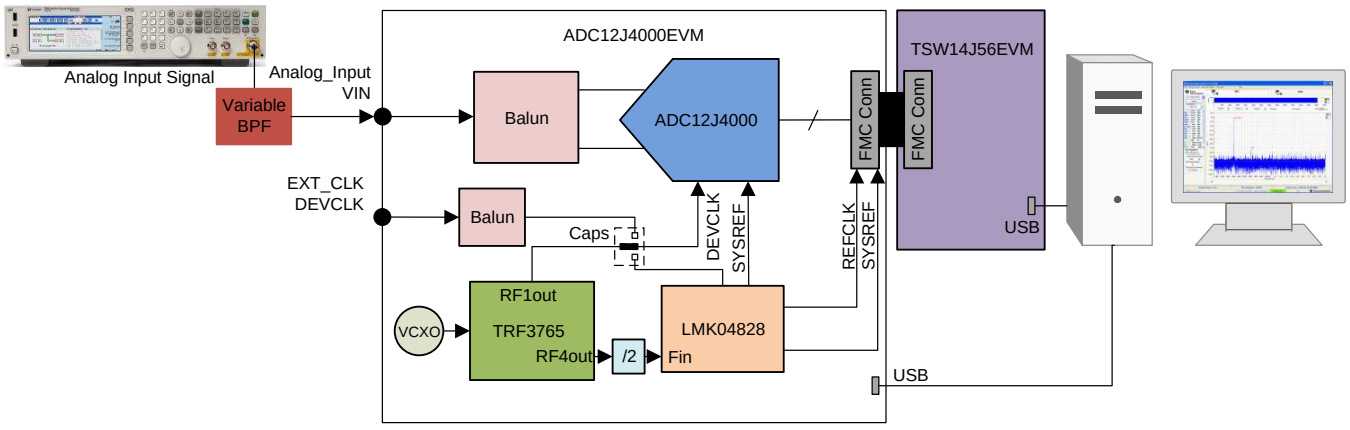

Figure 4. Test Setup for Internal Clock Signal

3.1.2 External Clock Input

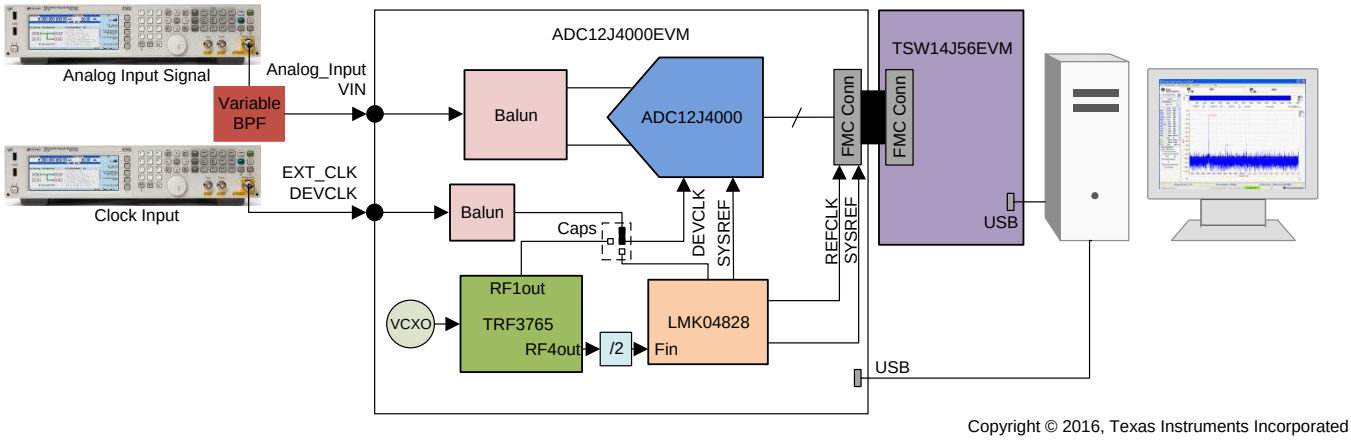

Figure 5. Test Setup for External Clock Signal

3.1.3 External Clock Input With BPF

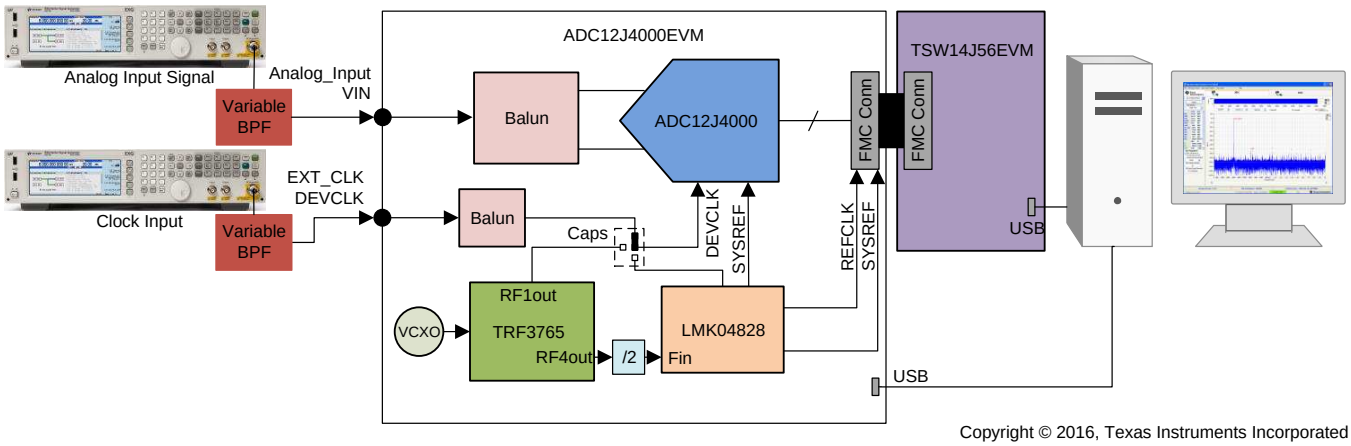

Figure 6. Test Setup for External Clock Signal With BPF

3.2 Results

Table 2 shows the measured SNR performance at various frequencies for a –1-dBFS differential input. The test results also show the SNR performance at the enhanced input frequency range around 4 GHz.

Table 2. Measured Results

INPUT FREQ (MHz)	EXPECTED SNR (dBFS)	MEASURED SNR (dBFS) (4-GHz EXTERNAL CLOCK)	MEASURED SNR (dBFS) (4-GHz INTERNAL CLOCK, TRF3765)
350	55.0	55.24	53.96
600	54.8	55.44	54.15
900	52.0	54.43	53.20
1500	51.2	53.07	52.97
2400	48.7	49.79	49.17
2700	48.5	49.13	49.02
3700	45.0	46.13	45.65

Table 3 shows the SNR improvement when the applied external clock signal is filtered and Figure 7 shows the SNR variation with and without clock filter. This test has been performed with the external clock input from a precision signal generator.

Table 3. Measured SNR Performance With and W/O Clock Filter

INPUT FREQ (MHz)	EXPECTED SNR (dBFS)	MEASURED SNR (dBFS) (4-GHz EXTERNAL CLOCK)	MEASURED SNR (dBFS) (4-GHz INTERNAL CLOCK, TRF3765)
		NO FILTER	BPF at CLK
350	55.0	55.24	55.58
600	54.8	55.44	55.55
900	52.0	54.43	54.80
1500	51.2	53.07	53.71
2400	48.7	49.79	50.59
2700	48.5	49.13	49.90
3700	45.0	46.13	46.74

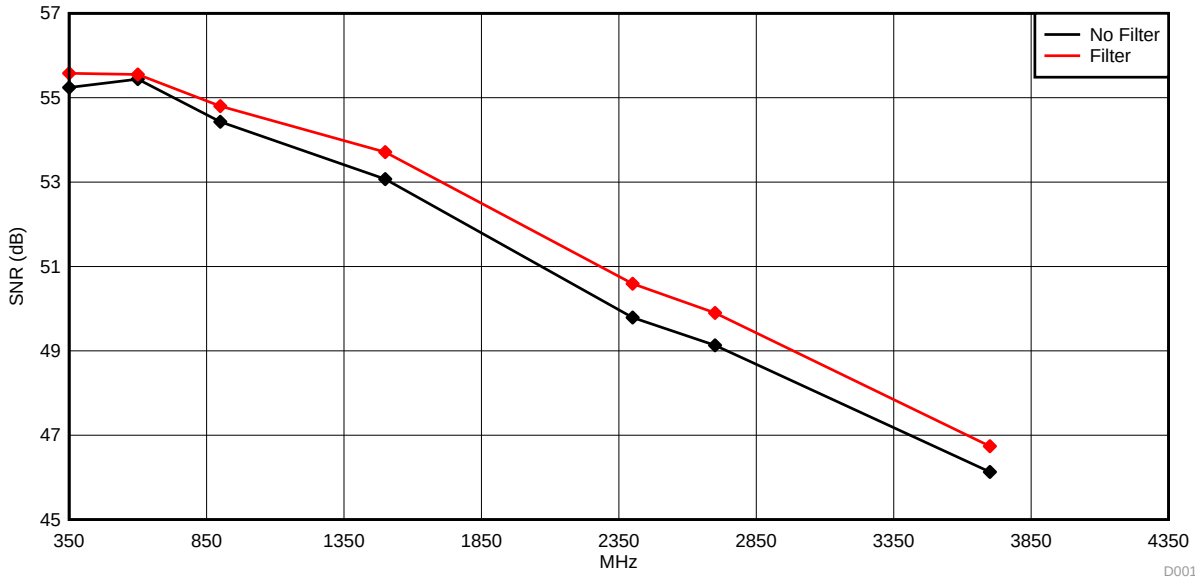

Figure 7. Measured SNR With and Without Clock Filter

Further analysis shows the significance of different clock frequencies for the same input frequency. Figure 8 and Figure 9 show the spectral results for a 2700-MHz input signal at two different clock frequencies, 3.5 GHz and 4.0 GHz, which are both in the second Nyquist zone.

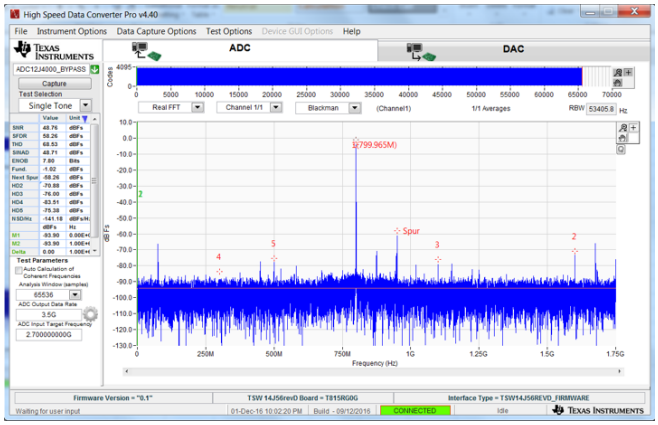

Figure 8. Spectrum at 3.5-GHz Clock for 2.7-GHz Input

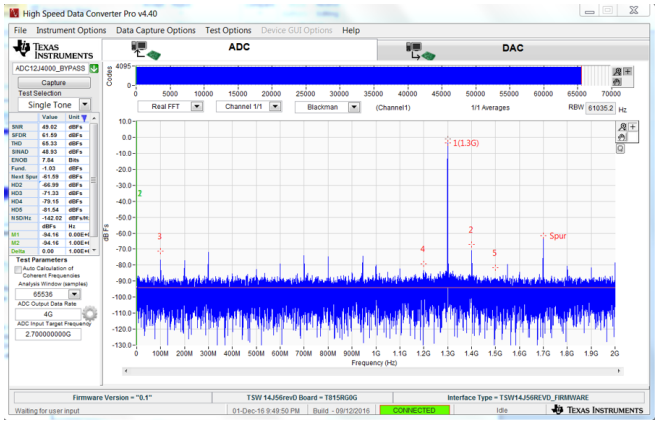

Figure 9. Spectrum at 4-GHz Clock for 2.7-GHz Input

As can be seen from the measured results, the SNR is better for the 4-GHz clock for the 2.7-GHz input. The performance improvement can be contributed to the reduced sampling attenuation effect at 4.0 GHz versus 3.5 GHz as shown in Figure 10.

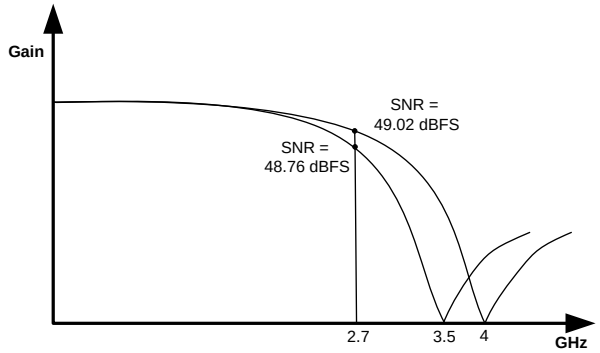

Figure 10. Approximate Gain Plot at Different Clock Frequencies

3.3 Summary

The TIDA-01015 is a clocking solution reference design for high-speed direct RF sampling GSPS ADCs that can be used for digital oscilloscopes, wireless testers, software defined radios, or other high-speed communication and data acquisition systems. This TI Design compares signal chain performance of using TI's high performance clocking solutions versus an ideal clocking source. Results with and without a clocking BPF are also studied. Finally, the significance and possible SNR improvement of using higher clock frequencies for second Nyquist inputs are demonstrated.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01015.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01015.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01015.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01015.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01015.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01015.

5 Software Files

To download the software files, see the design files at TIDA-01015.

6 Related Documentation

1. Texas Instruments, *ADC12J4000EVM User's Guide* (SLAU551)
2. Texas Instruments, *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card*, TSW14J56 User's Guide (SLWU086)

6.1 Trademarks

7 About the Authors

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