Five steps to a great PCB layout for a step-down converter

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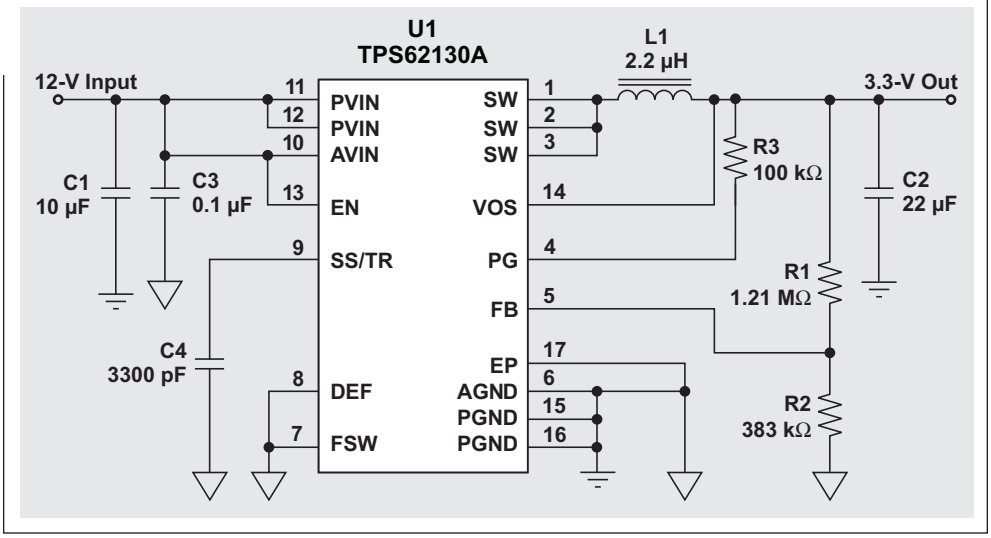
Introduction

Especially for switch-mode power supplies (SMPSs), the printed circuit board (PCB) layout is a critical but often under appreciated step in achieving proper performance and reliability. Errors in the PCB layout cause a variety of misbehaviors including poor output voltage regulation, switching jitter, and even device failure. Issues like these should be avoided at all costs, since fixing them usually requires a PCB design modification. However, these pitfalls are easily circumvented if time and thought are spent during the PCB layout process before the first PCBs are ever ordered. This article presents five simple steps to ensure that your next step-down converter's PCB layout is robust and ready for prototyping.

Figure 1. TPS62130A circuit used to step-down 12-V to 3.3-V

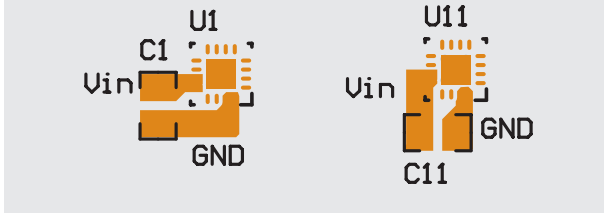


When designing a server, tablet, or electronic point-of-sale machine, a best-practice option with the least risk is to simply copy the PCB layout example found on the evaluation module (EVM) and shown in the datasheet. However, this may not always be possible for various reasons. This article was created for these cases and details a five-step procedure to design a good PCB layout for any TPS62xxx integrated-switch, step-down converter. The internal MOSFETs and integrated loop-compensation circuitry greatly simplify the PCB layout of these devices by reducing the difficulty and time required to do the PCB layout. The versatile TPS62130A is used as the example step-down converter, which can be used in each of the above applications. Figure 1 shows the completed schematic of a typical circuit.

Step #1. Place and route the input capacitor

The input capacitor is the single-most important component for reliable operation of any step-down converter. As such, it should be the first component placed in the layout after the IC. Route the capacitor to the IC immediately after it is placed, so that nothing else can be routed in its path. Extra parasitic inductance between the input capacitor's terminals, both power and ground, and the IC's PVIN and PGND terminals creates excessive voltage spikes due to the switching action from V = L × dI/dt. This can lead to IC failure.

Figure 2. Layout and routing of the IC and the input capacitor to reduce voltage spikes



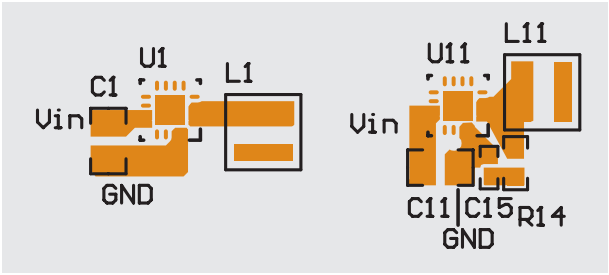
Place the input capacitor as close to the IC as allowed by manufacturing rules. Planes connect the input capacitor's terminals to the IC's. Making such a wide and short plane connection minimizes trace inductance. Add vias to connect to the system's input voltage and ground. These are added in Step #5 as they are less important. Figure 2 shows the correct placement and routing of the input capacitor and IC. Two circuits are shown due to two acceptable input-capacitor placements (C1 and C11) based on the TPS62130A's pinout (U1 and U11). Pin 1 of the IC is in the bottom right corner.

Step #2. Place and route the inductor and SW-node snubber

The second most important component to place and route is the inductor and SW-node snubber, if required. Snubber circuits are occasionally required to reduce the electromagnetic interference (EMI) of SMPSs by slowing down the rise and fall times of the SW node. Unfortunately, slowing down these timings reduces efficiency by increasing switching losses. Since the SW-node voltage swings from the input voltage to ground with very fast rise and fall times, it is the main generator of EMI in a SMPS. Modern SMPSs typically incorporate some EMI reduction techniques, which generally eliminate the need for a snubber. To be effective, add a resistor/capacitor (RC) snubber to the PCB layout at this step. This is where it has the shortest possible routing between the SW and PGND (GND) pins, minimizing its parasitic inductance.[1]

To reduce radiated EMI, place the inductor as close as possible to the IC with the area of the SW-node copper kept to a minimum. All copper connected to the SW node is one plate of a parasitic capacitor, whose other plate is each node in the circuit. This capacitor is a noise coupling path. By keeping the SW node small, the area of the capacitor plate is minimized and the coupling reduced. Rotate the inductor as needed in order to keep the SW node small and to make an easy connection to the output capacitor (Step #3). Figure 3 shows proper inductor placement (L1 and L11) with and without the RC snubber (R14 and C15) from SW to PGND (GND).

Figure 3. Layout and routing of the inductor and RC snubber to minimize EMI



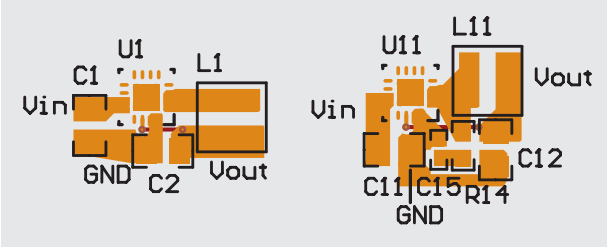
Step #3. Place and route the output capacitor and VOS pin

The output capacitor completes the routing of the power components (internal MOSFETs, input capacitor, output capacitor, inductor, and optional snubber). It is the final component connected to the power ground terminal in the system and is placed to minimize the distance from the inductor back to power ground. An improper output capacitor placement typically causes poor output voltage regulation.

Each power component is placed and routed to minimize the paths between them. Keeping these loop areas small enables the best operation of the SMPS. Finally, no vias should be used to route these components, because vias add significant inductance to the trace. In some specific cases, vias may be used on the SW-node connection. See the special considerations section at the end of this article.

The most critical small-signal connection is the VOS input pin. An improper or noisy VOS pin connection causes poor output voltage regulation, switching jitter, and in some cases, IC failure. Route the VOS pin now to ensure that it has priority over other signal routings. Make the VOS pin trace short and direct to the output capacitor. Due to the TPS62130A's pinout, route the VOS pin with two vias and a dedicated trace to the output capacitor. This gives priority to the power components in the circuit. To reduce noise pickup, isolate the two vias from all other connections except for the VOS pin and output voltage plane on the top layer. Do not route the TPS62130A's VOS pin directly on the top layer, as this breaks the PGND connection which is more important. Figure 4 shows proper placement and routing for C2 and C12 output capacitors and a good VOS-pin routing on the bottom layer.

Figure 4. PCB layout and routing of the output capacitor and the VOS pin for good regulation



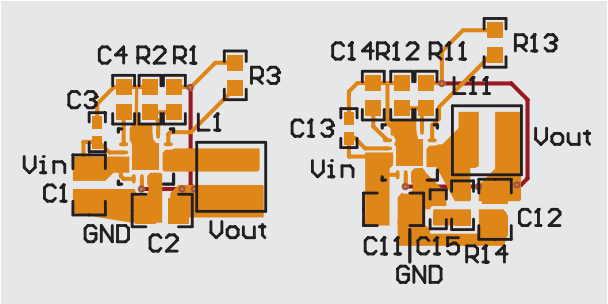
Step #4. Place and route the small-signal components

The small-signal components comprise all analog and digital components not directly related to the power conversion. These are components like the FB pin voltage divider, soft-start capacitor, and any small-value decoupling capacitors (0.1 µF for example). While the noisier power components and their nodes generate noise, the analog small-signal components are sensitive to noise. Place each of these components close to the IC with a short and direct routing to keep their noise sensitivity low. It is especially important to keep the FB node as small as possible to minimize noise pickup and provide good output voltage regulation. Use a common analog or quiet ground. Keep all components on a single side of the PCB for ease of routing. Common issues with poor placement and routing of small-signal components include poor output voltage regulation, erratic soft-start operation, and device operational problems.

Any digital signals, such as the EN and PG pin circuitry, are the least important to place and route, so do these last. Digital pins typically have a low impedance driving source. Any pull-up or pull-down resistors required

generally can be placed anywhere along the signal's path and do not need to be located close to the SMPS. Figure 5 shows proper placement and routing of the small-signal components: FB resistors (R1, R2 and R11, R12), SS/TR capacitor (C4 and C14), AVIN decoupling capacitor (C3 and C13), and PG pin pull-up resistor (R3 and R13).

Figure 5. Layout and routing of digital and small-signal components



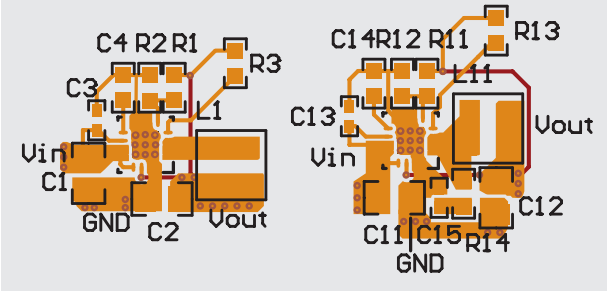
Step #5. Make a single-point ground and connect to the rest of the system

Always follow the datasheet's specific recommendations for grounding. Generally, this means keeping one ground for power components, which are noisy, and a separate ground for the small-signal components, which are quiet. By following the recommendations and steps given above, this is already done. Next, join these two grounds at a single point, typically the exposed thermal pad under the IC, which should also be connected to ground. Referring to Figure 5, the only edit needed to the grounds is to completely pour a copper plane between the PGND pins and the exposed thermal pad. The TPS62130A datasheet goes further to make this connection mandatory. Not making this connection might cause noise-related issues, such as poor output voltage regulation, or possibly improper logic levels for the digital input pins. This is due to voltage shifts between the grounds during operation. Properly connecting the grounds also provides the best thermal relief of the device.

With the grounding finished, it's time to connect this circuit to the rest of the system. This can be done with vias as the input voltage, output voltage, and ground are typically routed on planes on inner PCB layers to reach the various circuits. Starting with ground, vias are best placed directly under the IC so that the exposed thermal pad conducts its heat down into the PCB layers. This is required to achieve the IC's best thermal performance. Vias are also typically placed at the input- and output-capacitor's ground terminal. Placing vias into the system ground plane on the quiet grounded components is not generally recommended because this can couple noise from the ground plane into these nets. These grounds are best routed directly back to the AGND pin, where they make a single point connection to the exposed thermal pad.

Vias are also needed to connect the input and output voltages back into the system. It is best to place the vias outside the circuit, versus between the input capacitor and IC, for example, to not obstruct critical routings between components. A good rule of thumb for the number of vias necessary is to use one via per amp of current flowing. However, more is better if room allows. A finished layout is shown in Figure 6.

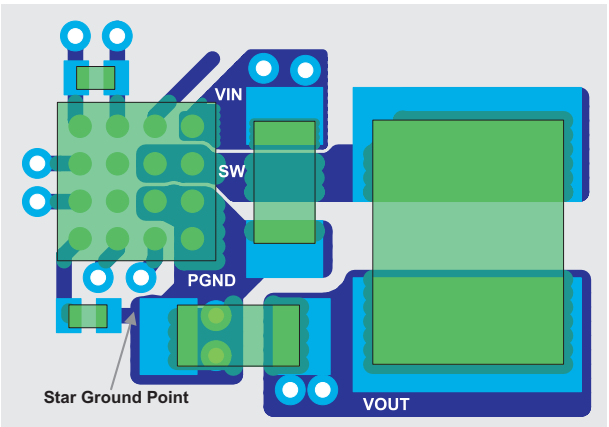
Figure 6. Finished PCB layout and routing with vias and single-point ground



Special considerations

Always consult the device's datasheet for specific layout recommendations and a recommended layout example. Directions and examples provided are sufficient for most devices' layouts. One type of layout that generates some confusion is commonly found on wafer chip-scale packages (WCSPs), such as the TPS62360. In many WCSP step-down converters, the IC's pinout places the SW pin between the VIN and PGND (GND) pins. If following Step #1, the input capacitor blocks access to the SW pin unless the SW pin is routed underneath the input capacitor. Some think this is undesirable because that trace must be rather thin to be routed between the terminals of a small component, such as the input capacitor. This then looks like Figure 7.

Figure 7. Recommended layout of the TPS62360 in a WCSP package[2]



The preferred PCB layout method is to route the SW pin underneath the input capacitor (Figure 7). While the SW trace is thin, it is also very short, which keeps the SW node small. This follows Step #2 to reduce EMI. If it is not possible to route such a trace, then use vias to connect the SW pin to the inductor. Vias in this connection merely create additional EMI by the longer routing. However, the added inductance of these vias is not critical as this parasitic inductance is in series with the inductor's inductance. Using vias in this path is a better choice than moving the input capacitor out of its ideal location.

Conclusion

When designing the PCB layout for a SMPS, always consult the device's datasheet and EVM for examples and specific recommendations. But for cases when it is not possible to exactly follow these, or in the rare case where these are not present, five simple steps allow for a good step-down converter layout:

1. Place and route the input capacitor.
2. Place and route the inductor and SW-node snubber.
3. Place and route the output capacitor and VOS pin.
4. Place and route the small-signal components.
5. Make a single-point ground and connect to the rest of the system.

Doing these steps will generate a robust design that gives good performance for servers, tablets, electronic point-of-sale machines, and any other system that uses step-down converters.

References

1. Jeff Falin, "Minimizing Ringing at the Switch Node of a Boost Converter," Application Note, Texas Instruments, September 2006. Available: **www.ti.com/1q15-slva255**
2. Layout example taken from the TPS62360 datasheet, figure 52, page 35. Available: **www.ti.com/lit/slvsau9**

Related Web sites

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