

PCB Layout for Low Distortion High-Speed ADC Drivers

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ABSTRACT

Once an analog-to-digital converter (ADC) and a driver/interface have been selected for a given application, the next step to achieving excellent performance is laying out the printed circuit board (PCB) that will support the application. This application report describes several techniques for optimizing a high-speed, 14-bit performance, differential driver PCB layout using a wideband operational amplifier.

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1 Introduction

Numerous techniques to apply wideband dual op amps to differential ADC drivers are presently available. After selecting the topology and amplifier based on the target specifications, PCB layout for even-order distortion suppression becomes the next design task.

In theory, a differential architecture allows the cancellation of 2nd-harmonic distortion, leaving the 3rd-harmonic as the dominant term. In practice, however, only a careful PCB layout results in effective 2nd-harmonic cancellation. The PCB layout techniques discussed in this report enable the combination of low distortion and high speed in an ADC driver.

NOTE: If you are reading this as a black-and-white document, please understand that the multiple layers shown in the example PCB diagrams are best displayed in color. Please see an on-line version of the document at the TI web site (www.ti.com) to view these layers more clearly.

2 Differential Layout Characteristics

As more and more ADCs are specified with differential inputs, a differential driver becomes necessary. Using a symmetrical design, the differential inverting configuration is preferred in order to obtain the best slew rate achievable by the amplifier. (See Figure 1.) In order to reap the full benefit of 2nd-harmonic cancellation that the differential architecture enables, PCB layout must be optimized. The number of board layers, characteristic impedance, component placement, ground planes, symmetry, and power supply decoupling are only a few of the many issues that need to be resolved when designing a PCB.

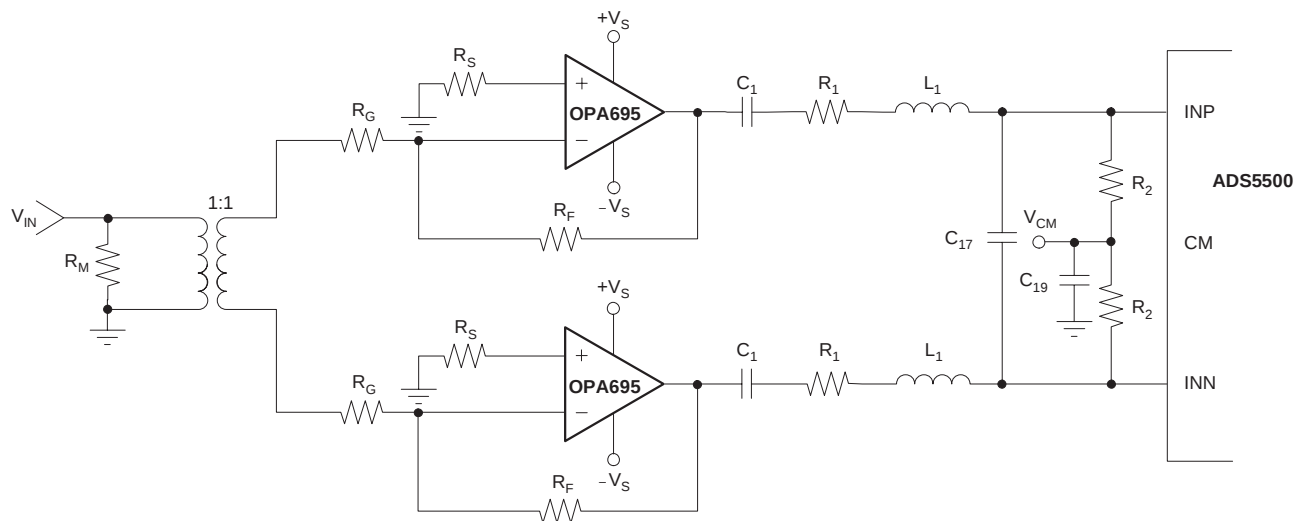


Figure 1. OPA695 Differential Interface to ADS5500

2.1 Symmetry

There are several different ways to explain symmetry. For the purposes of this application report, two definitions are of primary interest:

1. **component symmetry**, or when all board components are placed according to a certain pattern; and
2. **signal path symmetry**, where attention is given to the signal path instead of the component.

Figure 2 shows an example of component symmetry.

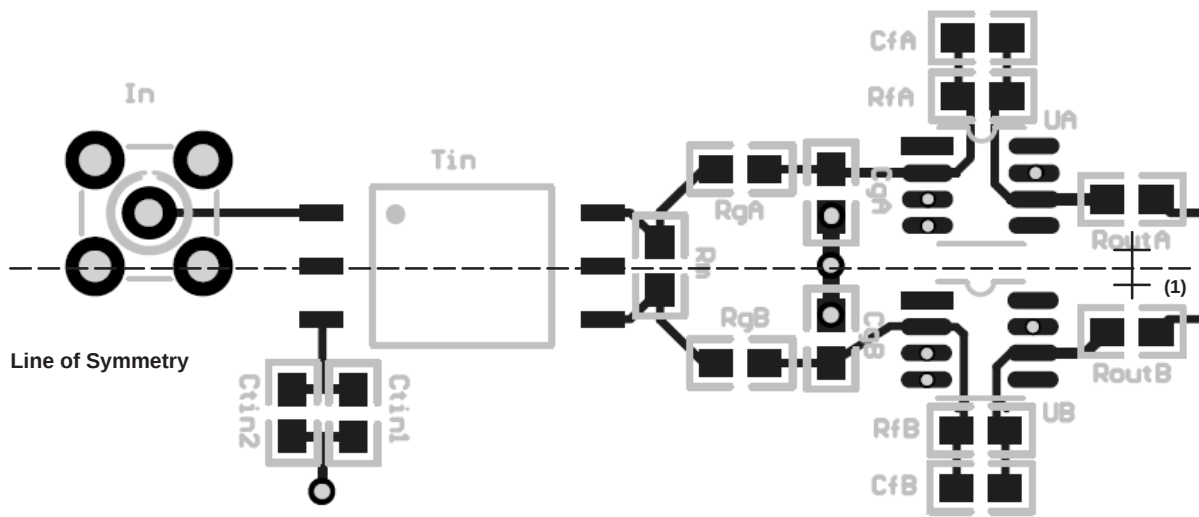


Figure 2. Component Symmetry Strategy, Line of Symmetry

In Figure 2, the example components have been placed according to a component symmetry strategy. The line of symmetry here is defined as passing through the middle of the transformer (T_{IN}). Consequently, the output resistors [R_{OUTA} , R_{OUTB} – see (1)] are equidistant from the line of symmetry. Although this approach is pleasing to the eye, there is still a difference in the signal path to accommodate the amplifier's pinout. In an SOIC-8 package, for example, the output pin is typically pin 6. Thus, the distance from pin 6 for UA to the center is different than the distance to the center from UB. This difference must be compensated for by the use of longer traces. Unmatched traces from path A and path B are shown in Figure 3.

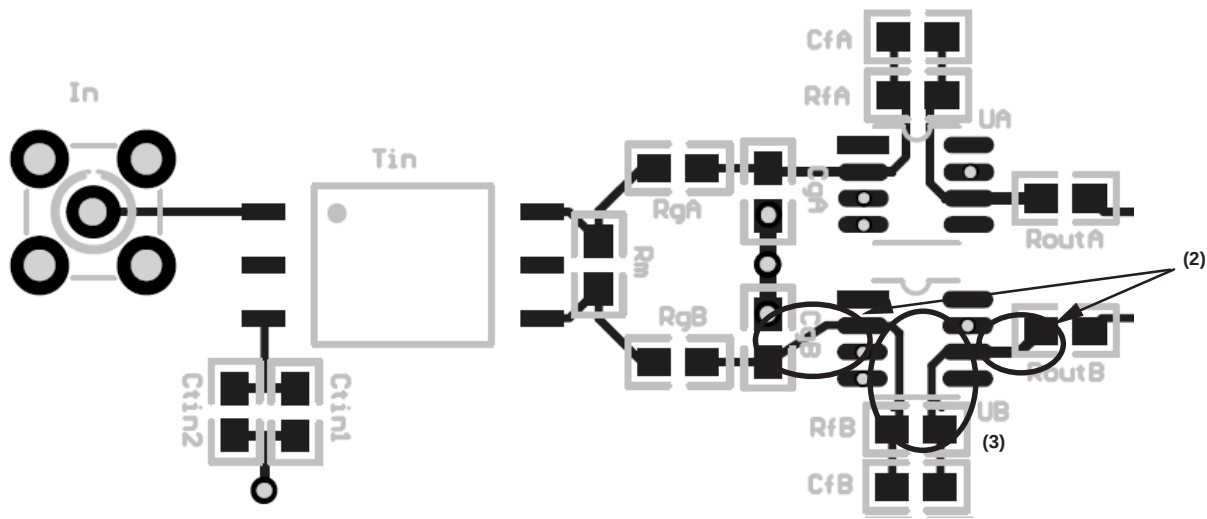


Figure 3. Component Symmetry Strategy, Unmatched Traces

Figure 4 shows a signal path symmetry strategy. Notice that trace length from pad to pad is the same for both the top path and the bottom path.

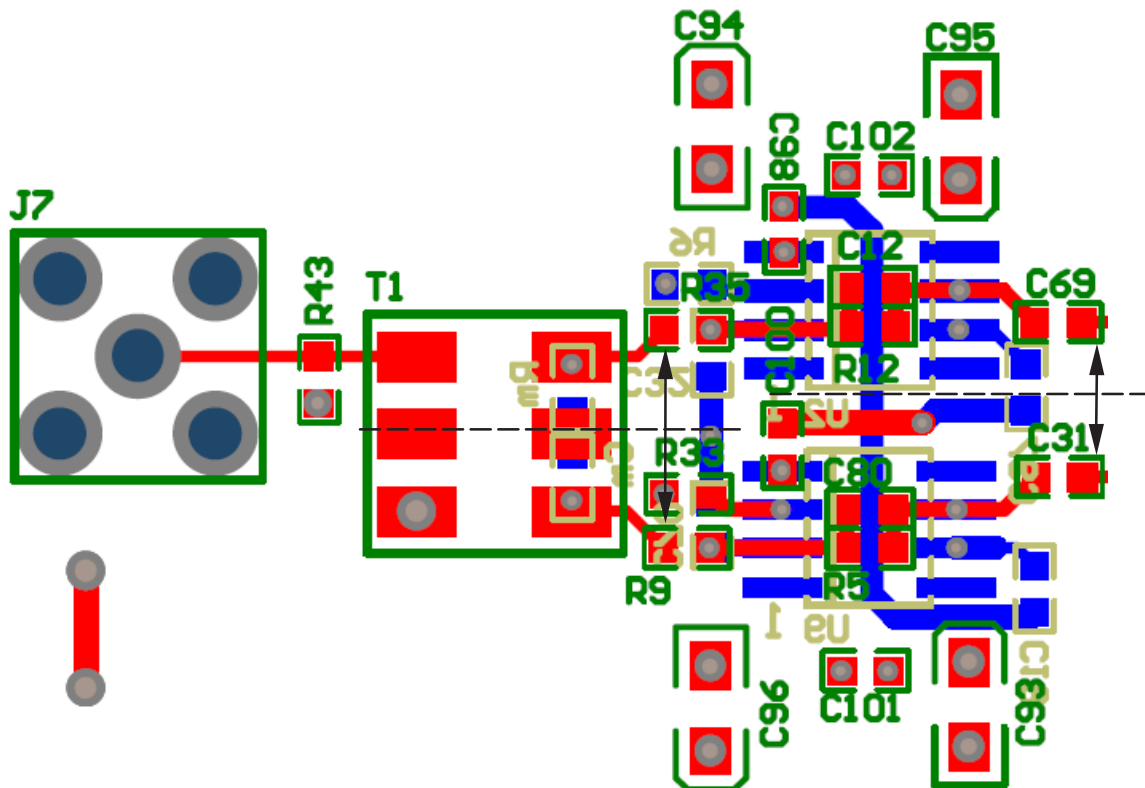


Figure 4. Signal Path Symmetry Strategy

There are also two distinct lines of symmetry: one on the driver input, and one on the driver output. The SOIC-8 footprints are symmetrical to the input line of symmetry. This characteristic eliminates the mismatch shown as (2) in Figure 3.

2.2 Choice of Footprint/Component Placement

The layout shown in Figure 4 is noticeably much more compact than that of Figure 2. This compact layout is a result of the choice of 0603-size components in place of 1206-size parts. Furthermore, using 0603-size components allowed the feedback components R_{FA} , C_{FA} , R_{FB} , and C_{FB} (renamed in the design shown in Figure 4 as R_{12} , C_{12} , R_5 , and C_{80} , respectively) to be placed on one side of the board with the op-amp directly on the other side, avoiding vias and parasitic coupling between the feedback component pads and the non-inverting input of the operational amplifier (pin 3 of the SOIC-8). This smaller size also minimized the output trace length back to the inverting input and eliminated the mismatch shown as (3) in Figure 3.

2.3 Power-Supply Decoupling

As with most active integrated circuits, operational amplifiers require good power-supply decoupling. Literature on this subject typically recommends two capacitors on each supply: one high-frequency capacitor ($0.1\mu\text{F}$), directly connected (or less than $0.25''$ from the power supply pin); and one larger ($2.2\mu\text{F}$ to $6.8\mu\text{F}$) decoupling capacitor, effective at lower frequencies. The second capacitor can be placed somewhat further from the device. Note that it can be shared among several devices in the same area of the PCB. In addition to these capacitors, a third smaller capacitor (10nF) can also be added between the supplies. This extra capacitor usually helps reduce 2nd-harmonic distortion.

Figure 5 shows specific capacitor locations. Larger capacitors are shown as C93, C94, C95 and C96. High-frequency capacitors are labeled as C18, C97, C98 and C100. C101 and C102 are the smaller capacitors between the supplies.

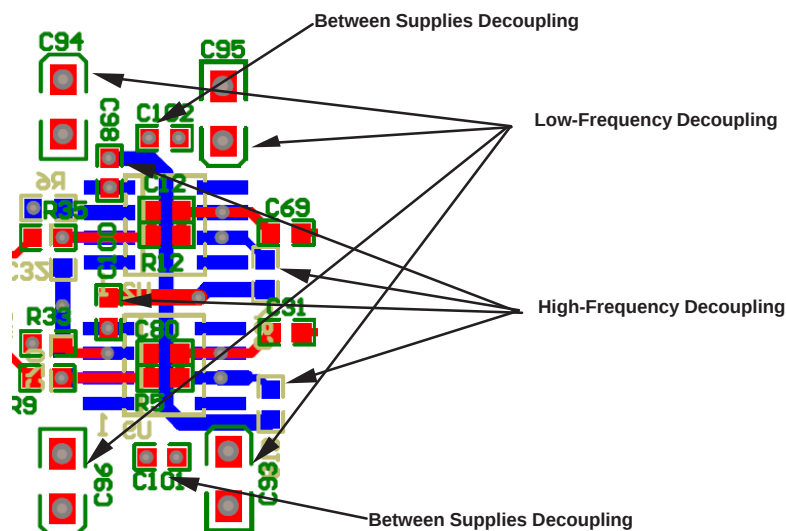


Figure 5. Power Supply Decoupling

One additional detail is the star connection for the ground connection of C97, C98, C18 and C100. This connection allows the cancellation of some distortion generated by the amplifier before it propagates to the common ground. Figure 6 shows the return paths of the high-frequency bypass capacitor to ground.

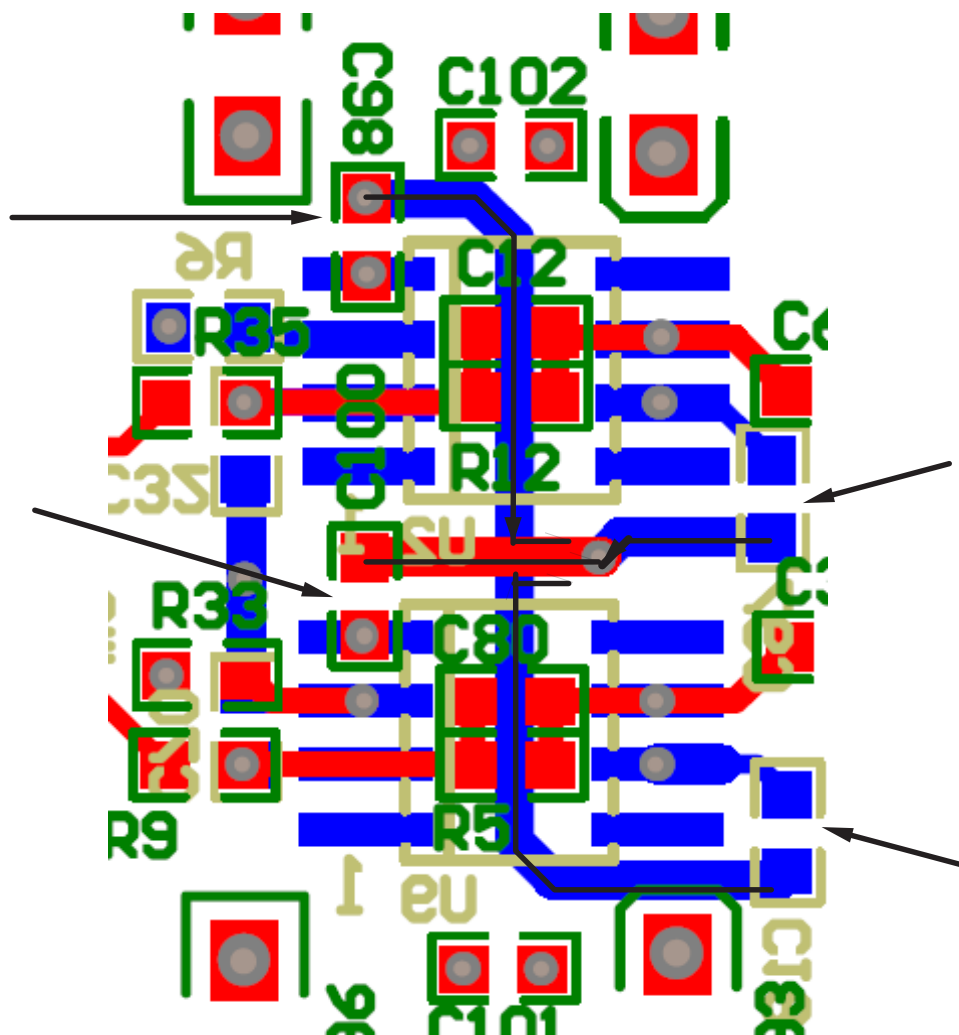


Figure 6. High Frequency Bypass Capacitor Star Connection

2.4 Ground Planes

The importance of not generating distortion, or keeping distortion away from the ground planes, cannot be emphasized enough. However, at one point or another, some distortion will most likely reach the ground plane, and will then propagate across the board possibly degrading distortion.

Having only one ground plane on the board is ideal, although this goal cannot always be attained. When additional ground planes are necessary, the use of a *quiet ground* is recommended. This design uses one ground plane as a reference, and connects all other planes that need to be connected to ground to it through one (and only one) connection.

Figure 7 represents a four-layer board, where the top and bottom layers are used for signal and the two inner layers are used for ground. It illustrates the quiet ground concept used in conjunction with a single ground plane.

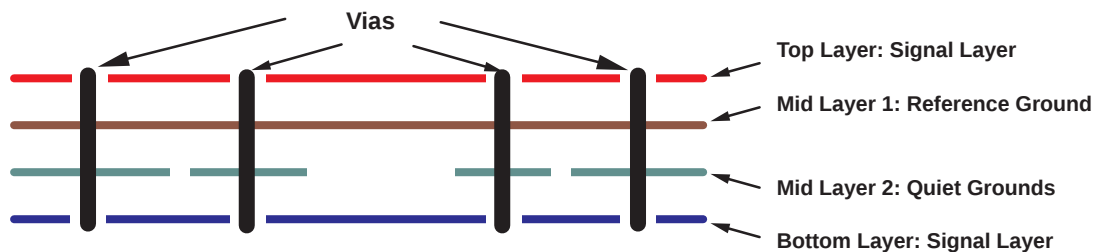


Figure 7. Ground Plane and Quiet Ground

Opening the ground planes as well as power planes under the device avoids parasitic capacitive coupling that may feed back undesirable signal to the noninverting input. Figure 8 shows the ground plane open under both operational amplifiers.

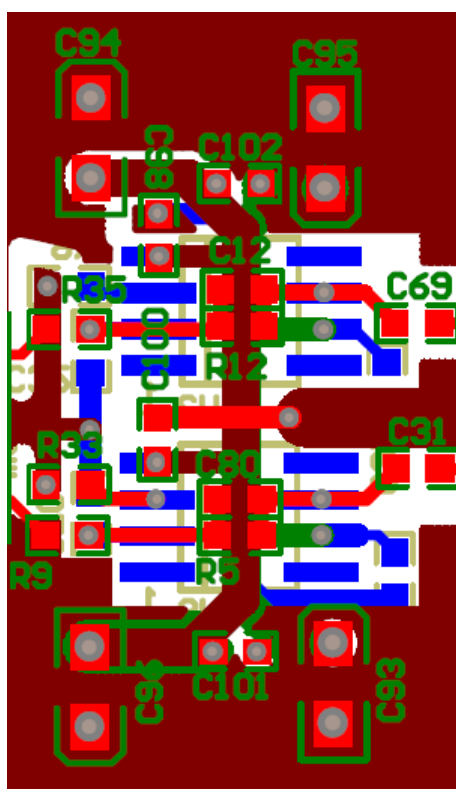


Figure 8. Ground Plane

Note that not only the ground plane has been opened under the operational amplifiers, the opening has been extended in order to enclose *all pads directly connected* to the operational amplifiers. Additionally, whenever a trace is necessary or desirable for connecting a pad to ground, its width is greater than 50 mils (0.050in), thus minimizing trace parasitic inductance and resistance.

2.5 Power Supplies Traces

Powering both amplifiers without crossing any signal traces has been accomplished by running the positive and negative supply traces on the inner layers on top of one another, underneath the SO-8 packages. Both traces are shown in black in Figure 9a and Figure 9b. Figure 9a and Figure 9b are both top views of the board. (Figure 9b shows the inverted order of the layers of Figure 9a.)

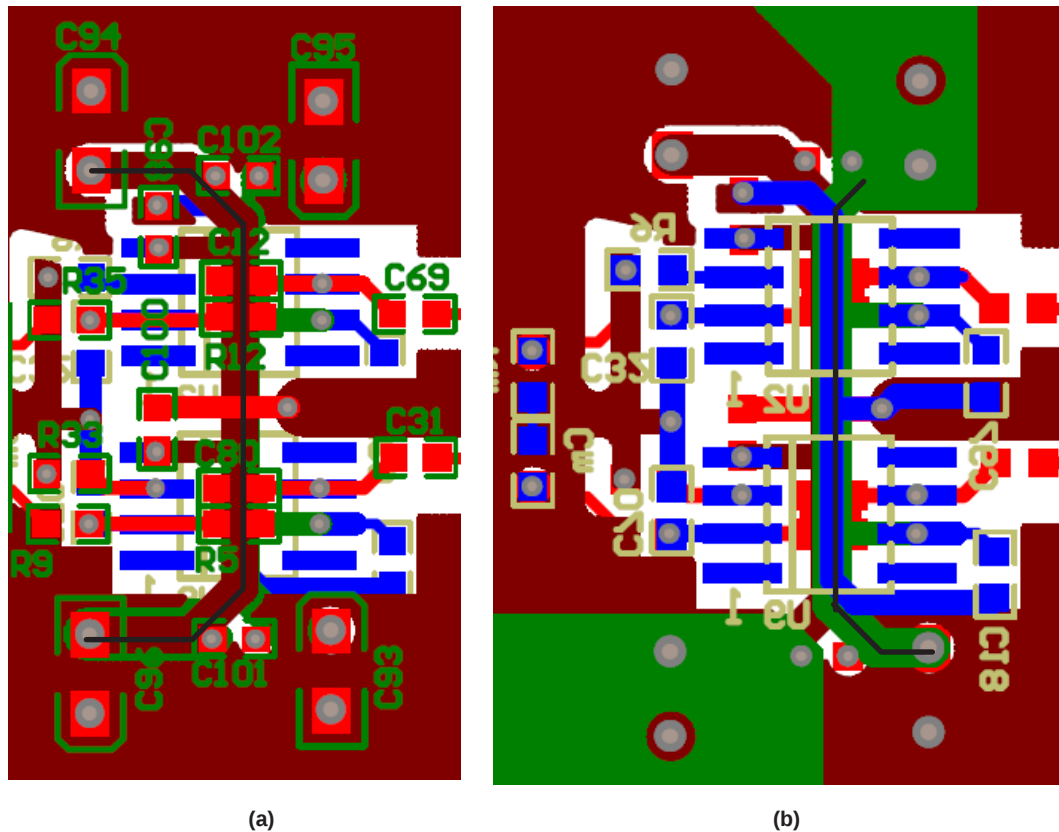


Figure 9. (a) Top View (Layer Order: Top Layer, Ground, Power, Bottom Layer)
(b) Top View (Layer Order: Bottom Layer, Power, Ground, Top Layer)

This configuration reduces the number of layers on the PCB to four.

3 Differential Layout Performance

Testing the differential layout discussed in this report using the ADS5500 (125MSPS, 14-bit ADC converter) and the OPA695 (Ultra-Wideband, Current-Feedback Operational Amplifier with Disable) shows that 2nd-harmonic distortion appears to be completely cancelled; see Figure 10. The 2nd-harmonic at 20MHz shows a -98dB level as a result of the converter alone. The configuration shown in Figure 1 was used to achieve this result.

The ADS5500 running at 122MSPS has a 10MHz SFDR of 87dB and an SNR of 72dB when driven through a transformer. The use of the OPA695, which drives it with a differential inverting circuit, achieves an SNR of 69.8dB and 87.1dBFS SFDR. From the plot below, neither the 2nd- nor 3rd-order terms are dominant for the converter in this test.

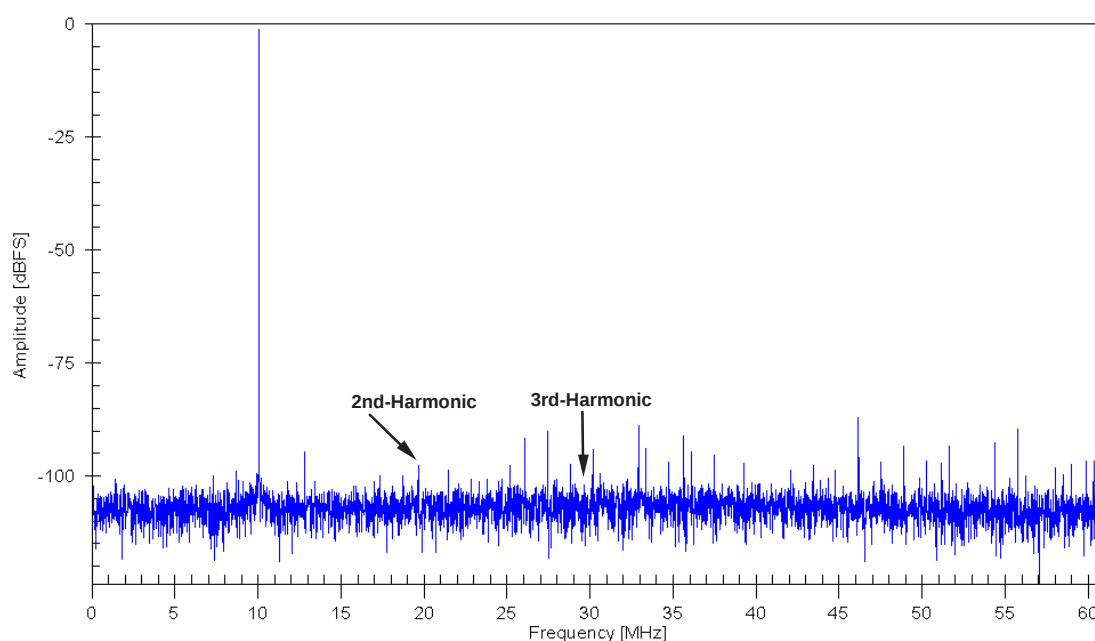


Figure 10. OPA695 Differential Driver Circuit Driving ADS5500

Table 1 gives 2nd-harmonic, 3rd-harmonic, SFDR and SNR results for the OPA695 driving the ADS5500 over frequency. Conditions for the test are:

- $F_S = 122\text{MSPS}$ for the ADS5500
- $F_{-3\text{dB}} = 54\text{MHz}$ for the RLC filter
- OPA695 in a differential configuration, as shown in Figure 1
- Layout discussed in this application note

Table 1. Tested Results for Figure 1 Layout

Frequency (MHz)	HD2 (dBFS)	HD3 (dBFS)	SFDR (dBFS)	SNR (dB)
10	98.0	102.0	87.1	69.9
12.5	92.0	88.2	88.2	69.7
15	92.0	89.0	88.1	69.7
20	83.9	88.0	83.9	69.6
30	81.1	94.0	81.1	69.3
40	86.0	82.4	82.4	68.9

For the OPA695 in a single-ended configuration ($1V_{PP}$), the second harmonic is -74dBc at 10MHz. Here at 10MHz, the 2nd-harmonic distortion ($1V_{PP}$ on each amplifier) is -98dBc , or a 24dB improvement over the single-ended configuration. Over frequency, the 2nd-harmonic in the differential configuration stays below the 80dB level. Note that at higher frequencies, the filter starts providing some attenuation. The 3rd-harmonic distortion is not increasing rapidly, as a result of the 2nd-order filter.

For a more complete discussion of RLC filters, please refer to application report SBAA108, *RLC Filter Design for ADC Interface Applications*.

References

Steffes, M. RLC Filter Design for ADC Interface Applications. Application Note. (SBAA108)

OPA695 Datasheet (SBOS293)

ADS5500 Datasheet (SBAS303)

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