Application Report
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Low Power Input and Reference Driver Circuit for ADS8318 and ADS8319

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ABSTRACT

The *one size fits all* approach to operational amplifiers (op amps) is not effective. Every application has its own specific requirements that must be fulfilled. Appropriate selection of the op amp that drives an analog-to-digital converter (ADC) in a low-power application is a critical step. Most available low-power op amps trade off low-power features with other parameters such as bandwidth, settling time, slew rate, or amplifier noise, and typically, these trade-off areas play a crucial role in data conversion applications. This report specifically addresses the matching of the THS4281 (a very low power, high-speed op amp) with the ADS8318 and the ADS8319, two 16-bit, 500-kSPS, low-power, serial, successive approximation register (SAR) ADCs.

The discussion starts with a short introduction to the ADS8318, ADS8319, and THS4281, followed by the driver circuits for the ADS8318 (for both differential and single-ended input configurations) and the ADS8319. Then, circuit performance is demonstrated through test results and several recommendations are presented regarding op amp selection for both the ADS8318 and ADS8319.

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1 Introduction

The ADS8318 and ADS8319 are two 16-bit, 500-kSPS SAR ADCs available from Texas Instruments. The ADS8318 receives a unipolar differential input while the ADS8319 receives a unipolar single-ended input. Both devices are optimized for very low power operation (typically, 18 mW at a speed of 500 kSPS and 5-V supply voltage), and overall power consumption directly scales with speed. This feature makes it attractive for a wide range of low-power applications.

The low-power feature of the ADS8318 and ADS8319 becomes even more attractive if the ADC is matched with low-power op amps for driving its inputs and reference. The THS4281 meets these demands by offering a very low quiescent current (less than 1 mA) across supply voltage and temperature. It also has a high bandwidth (40 MHz, specified at gain of 2) and settles quickly.

Figure 1 illustrates the open-loop gain versus frequency response of a generic op amp. This response shows a dominant pole frequency (f_{P1}), a crossover frequency (f_X) and a higher-order pole (f_{P2}). The crossover frequency, f_X, is the point at which $a\beta = 1$; *a* is the open-loop gain of the op amp and β is the feedback factor.

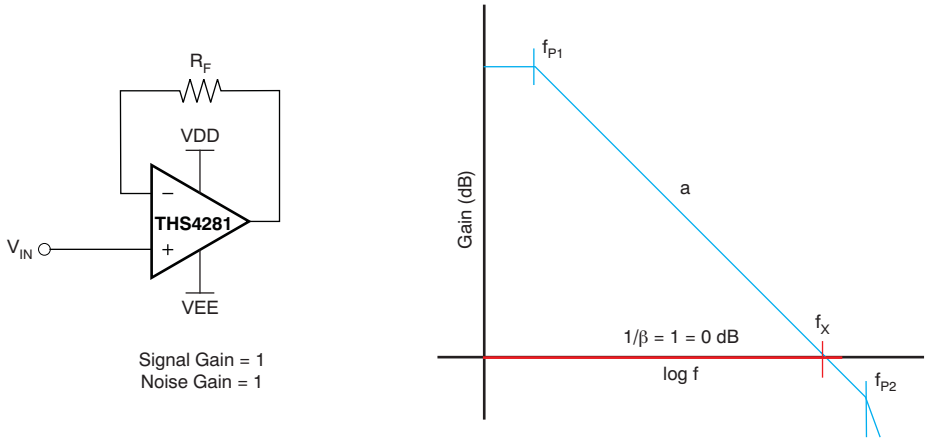

Figure 1. Open-Loop Gain vs Frequency (Generic Op Amp Response)

When f_X and any higher-order poles (f_{P2}, f_{P3} … etc.) are far from each other (say, $f_{P2} > 10f_X$), then the closed-loop unity gain frequency response of the op amp is flat. But, when f_X and f_{P2} are very close, peaking is seen in the closed-loop unity gain response of the op amp because of the reduced phase margin, which may lead to oscillations. As expected, the THS4281 shows peaking in its closed-loop unity gain frequency response.

The closed-loop frequency response of the op amp can be improved by pushing the aβ = 1 point (that is, the crossover frequency) towards the low frequency end, where phase margin is higher. This effect can be achieved by reducing β (or increasing 1/β), as shown in Figure 2. However, reduction in β is usually achieved at a cost of increased noise gain ($1 + R_F/R_1$, in Figure 2). This trade-off causes signal-to-noise ratio (SNR) degradation of the ADC. Note that the circuit shown in Figure 2 maintains its unity gain configuration without loading the source or the op amp output.

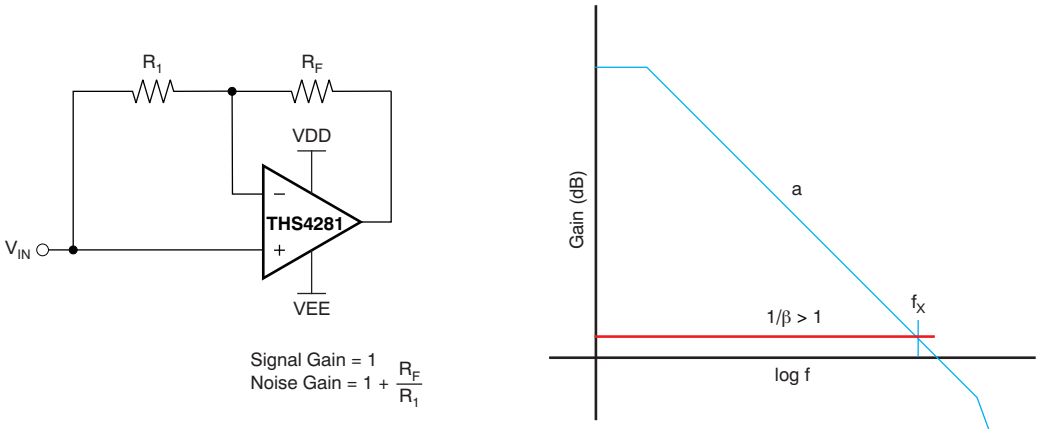

Figure 2. Reduced Feedback Factor Reduces Peaking

The feedback network can be made to be frequency-dependent. For example, at low frequencies where 1/f noise dominates and noise spectral density is high, the noise gain is maintained as unity. At a crossover frequency f_X (where aβ =1), 1/β is maintained sufficiently high to provide compensation for a peaked closed-loop response (as Figure 3 illustrates). For the THS4281, $\beta = R_1/(R_1 + R_F)$ of –3 dB to –6 dB is found to be sufficient to flatten the unity-gain frequency response.

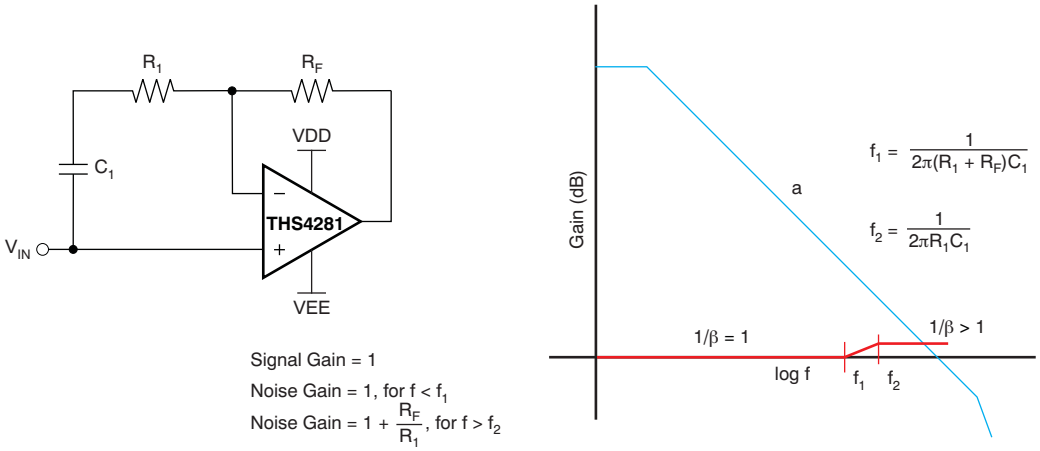

Figure 3. Noise Reduction Effect

2 ADS8318 Driver Circuits

Figure 4 and Figure 5 illustrate two driver circuits for the ADS8318, using the THS4281 as an input driver and reference buffer. Figure 4 illustrates the circuit configuration for a unipolar differential input, and Figure 5 shows the configuration for a unipolar single-ended input.

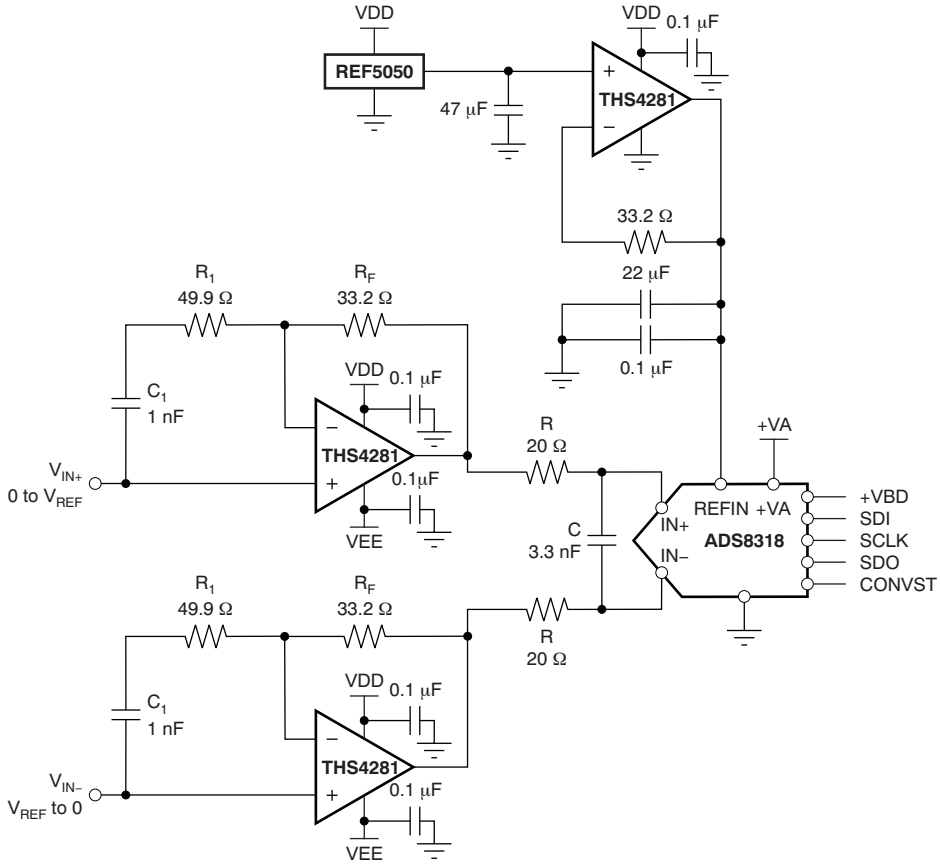

Figure 4. ADS8318: Driver Configuration for Unipolar Differential Input

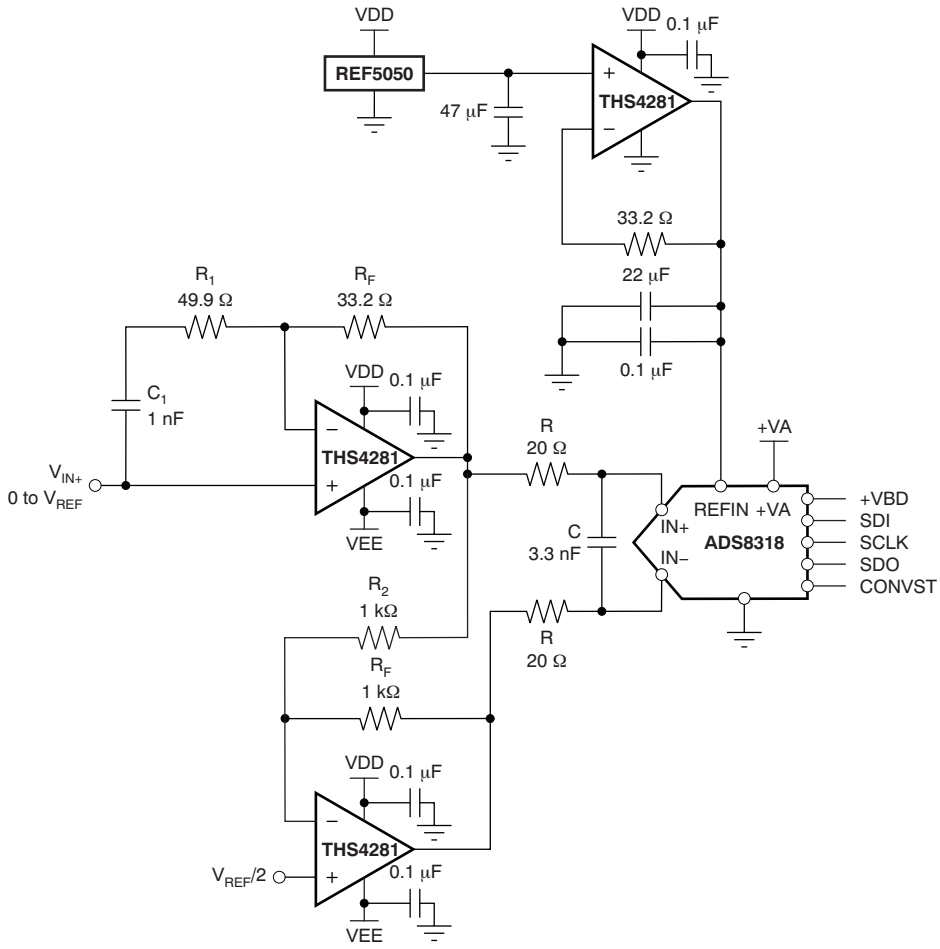

Figure 5. ADS8318: Driver Configuration for Unipolar Single-Ended Input

These circuits are configured with these design parameters:

- V_{REF} = Reference voltage applied to the ADC
- VDD = Positive analog power supply (VDD > 0)
- VEE = Negative power supply to the op amp (VEE < 0)
- VDD > V_{REF} + 1.5 V (to accommodate an input offset voltage shift with the common-mode input voltage for the THS4281)
- (VDD – VEE) < 16.5 V

None of the THS4281 input pins are left floating when it is powered.

From Figure 4:

- 2RC time constant = $2 \times 20 \times 3.3$ nF = 132 ns
- Corresponding –3-dB frequency = 1.2 MHz
- THS4281 input voltage noise = 12.5 nV/$\sqrt{\text{Hz}}$
- Noise contribution from one THS4281 = 12.5 nV/$\sqrt{\text{Hz}} \times \sqrt{1.2\ \text{MHz}}$ = 13.7 μV
- V_{REF} = 5.0 V
- RMS signal voltage = 5.0 V/$2\sqrt{2}$ = 1.767 V
- Quantization noise = 5.0 V/($2^{16} \times \sqrt{12}$) = 22.0 μV
- Total RMS noise (quantization noise and noise of two THS4281s):

$$\sqrt{13.7^2 + 13.7^2 + 22.0^2} = 29.13\ \mu\text{V}$$

- SNR = 20log(1.767 V / 29.31 μV) = 95.6 dB

The *2RC* time constant applied in Figure 4 is 132 ns. For a full-scale step input to settle to 18-bit accuracy at the ADC input, the 2RC time constant should be less than:

$$\frac{600\ \text{ns}}{[\ (N + 2) \times \ln 2\ ]} = 48\ \text{ns}$$

where:

- 600 ns is the acquisition time
- N = 16 is the resolution of the ADC

Because the THS4281 is slightly noisy, a higher time constant is required to band-limit the noise within the acceptable specification range.

3 ADS8319 Driver Circuit

Figure 6 illustrates a driver circuit for the ADS8319, also using the THS4281 as an input driver and reference buffer.

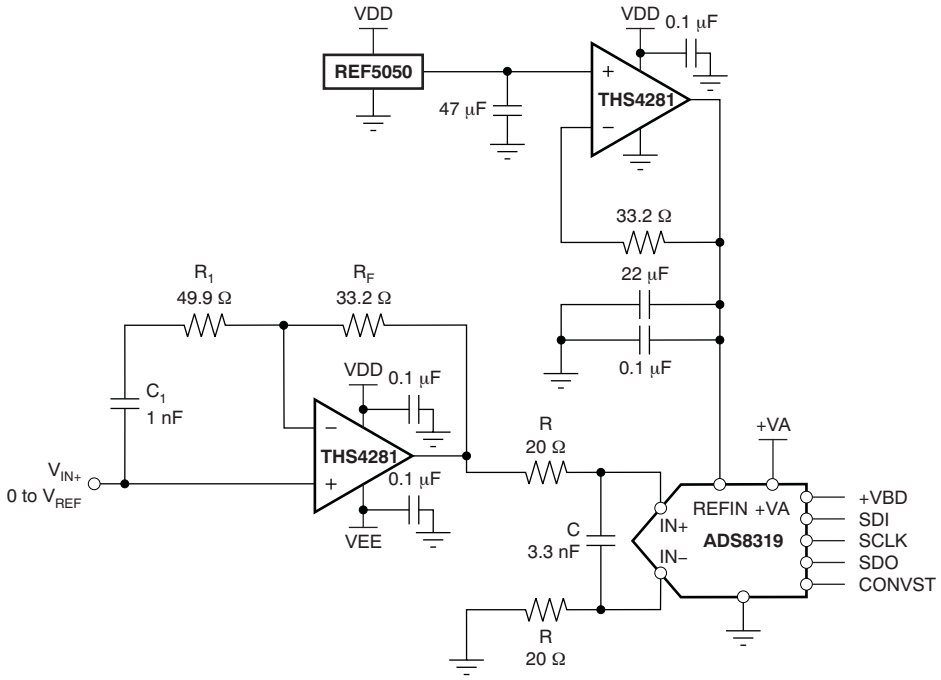

Figure 6. ADS8319: Driver Configuration

4 Performance Results

This section presents the performance results obtained on several devices for the driver configurations discussed earlier. The results are then compared with the benchmark results obtained for these circuits with the THS4031 as the driving op amp. The THS4031 is very high-performance op amp, but it has very high quiescent current.

Figure 7 illustrates a typical power spectrum for the circuits shown in Section 2 and Section 3. Figure 8, Figure 9, and Figure 10 show typical linearity plots for these same circuits. To compare these results with the graphs obtained using the THS4031 as the driving op amp, refer to the ADS8318 and ADS8319 product data sheets (available for download at www.ti.com).

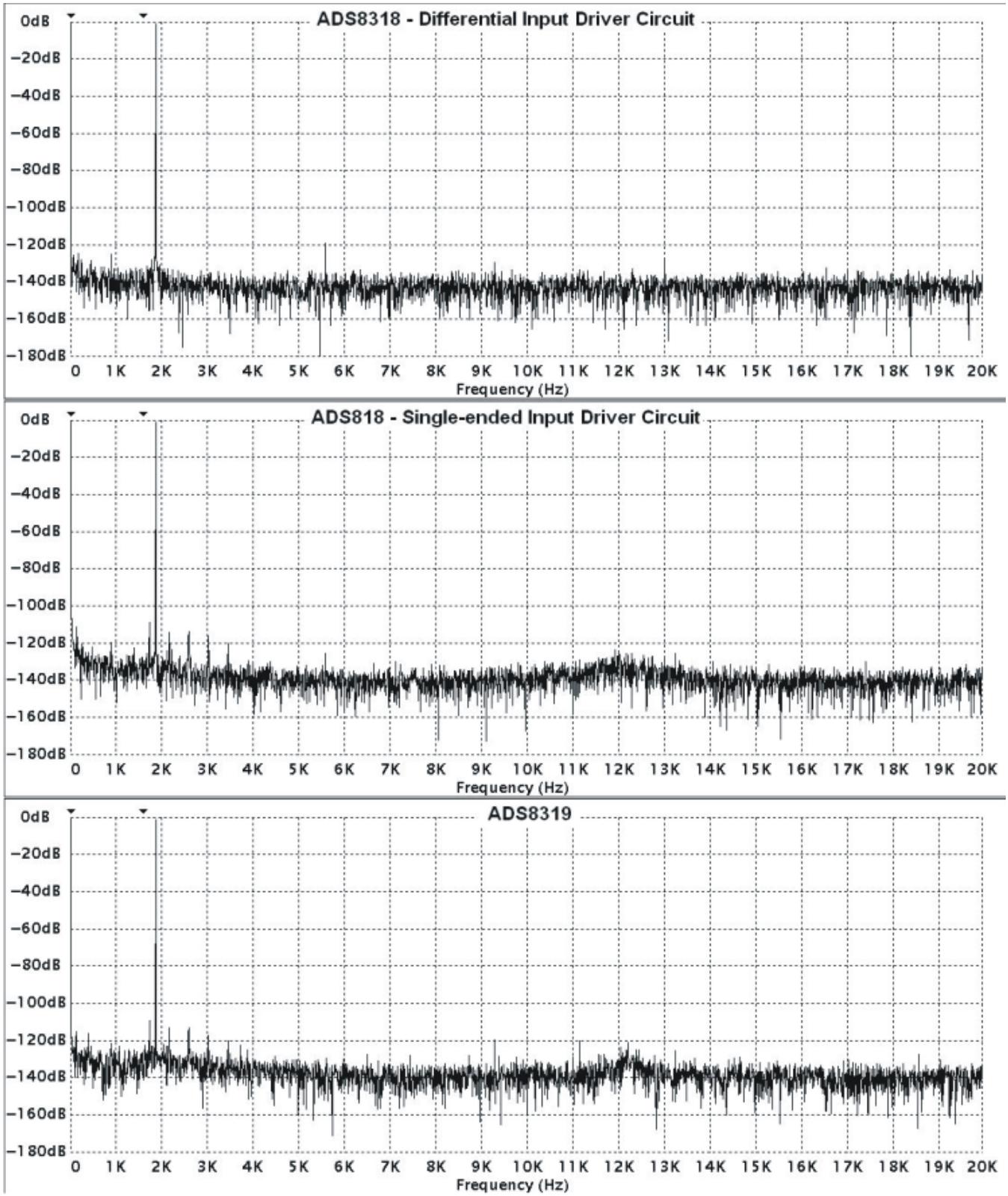

Figure 7. Power Spectrum Comparison

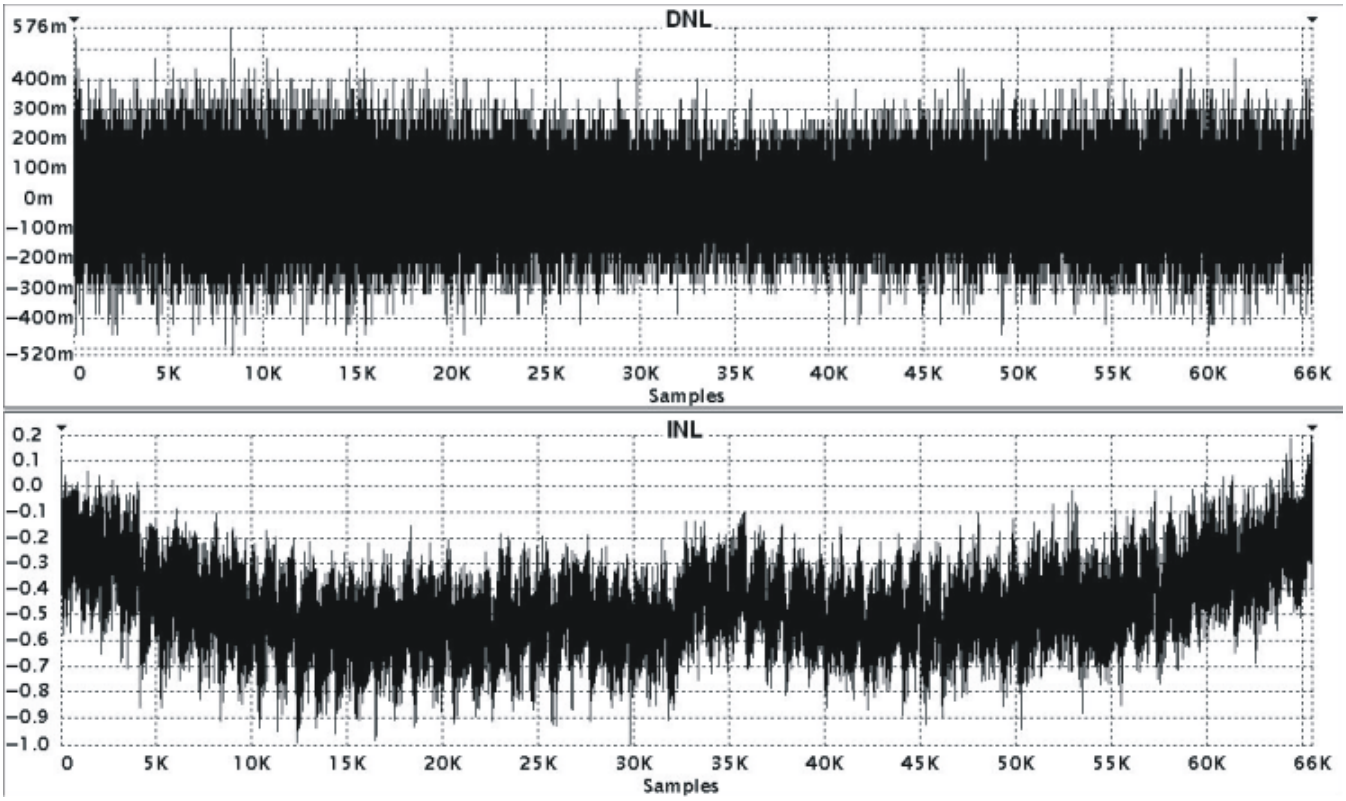

Figure 8. ADS8318: Typical Linearity Graphs (Differential Configuration)

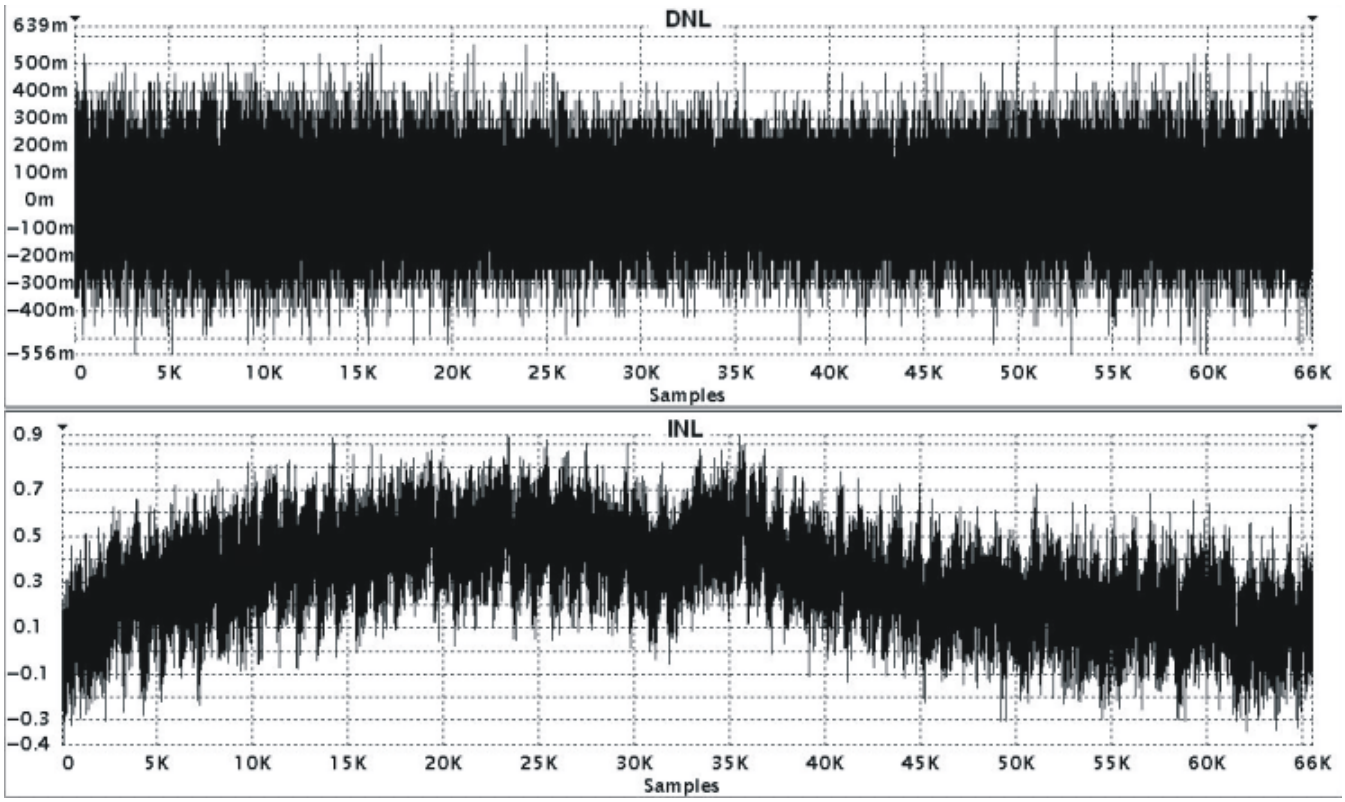

Figure 9. ADS8318: Typical Linearity Graphs (Single-Ended Configuration)

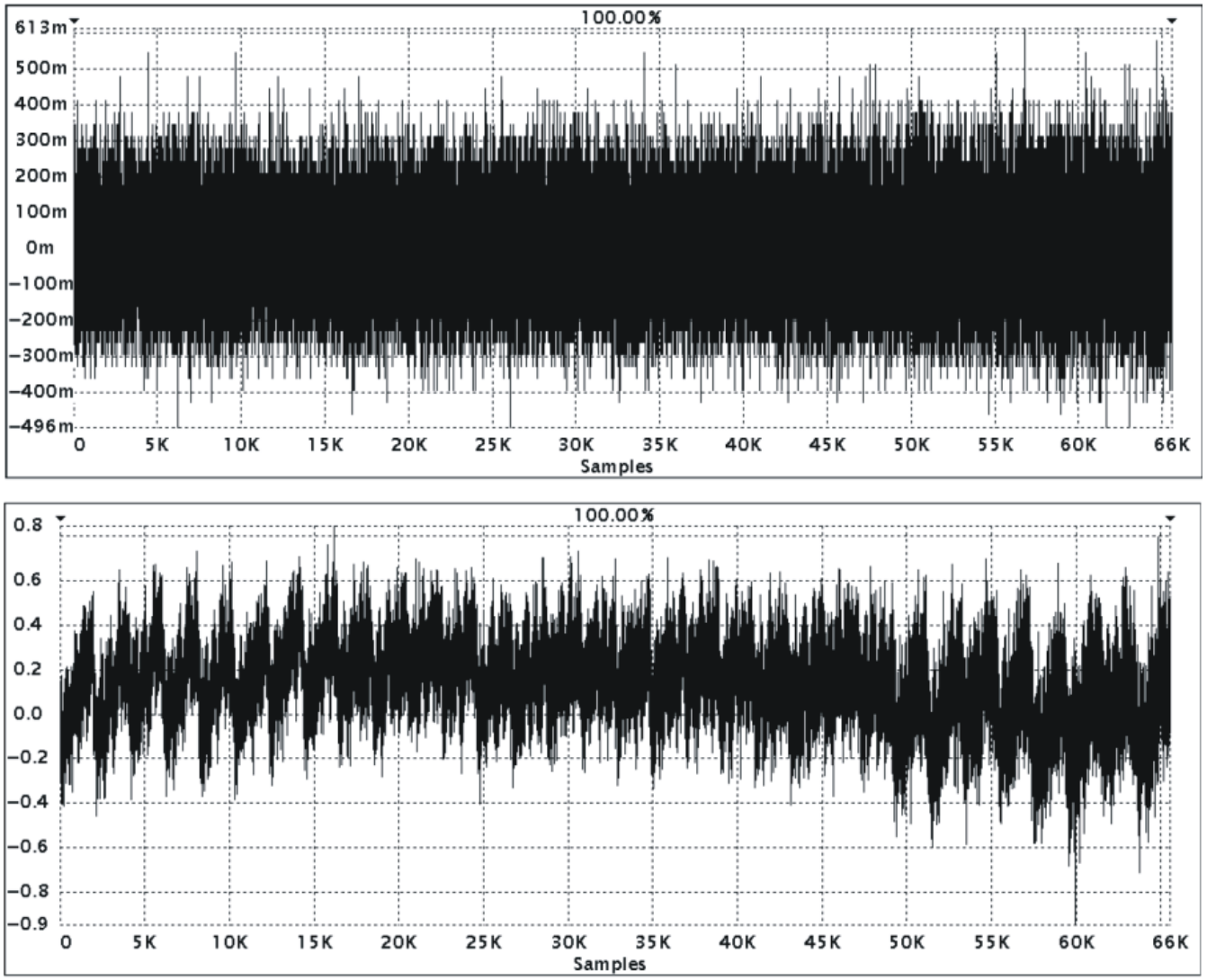

Figure 10. ADS8319: Typical Linearity Graphs

Table 1 describes the typical average power contribution from the various components used in the circuits shown in Figure 4 and Figure 6.

Table 1. Typical Average Power Numbers

Circuit	ADC	Input Driver Op Amps (THS4281)	REF5050	Reference Buffer (THS4281)	Total Power
ADS8318 Differential (Figure 4)	20 mW	2 × 0.8 mA × 7.3 V = 11.68 mW	0.8 mA × 7 V = 5.6 mW	1 mA × 7 V = 7 mW	44.28 mW
ADS8319 (Figure 6)	20 mW	0.8 mA × 7.3 V = 5.84 mW	0.8 mA × 7 V = 5.6 mW	1 mA × 7 V = 7mW	38.44 mW

Test Conditions: ADC: +VA = 5 V, +VBD = 5 V, V_{REF} = 5 V, Throughput = 500 kSPS, T = 300 kelvin, and input signal frequency = 1.9 kHz.

Op Amp: VDD = 7 V, VEE = –0.3 V

Table 2 summarizes the results obtained for a differential circuit configuration (see Figure 4), and Table 3 shows the results obtained for single-ended circuits (see Figure 5 and Figure 6).

Table 2. Performance Results for Differential Circuit Configuration (Figure 4)

Parameter	Datasheet Limits	ADS8318 with THS4031	ADS8318 with THS4281
DNL_{MAX}	< 1	0.33	0.47
DNL_{MIN}	> –1	–0.34	–0.52
INL_{MAX}	< 1.5	0.35	0.33
INL_{MIN}	> –1.5	–0.59	–0.68
SNR	> 95. 5dB	96.0 dB	95.5 dB
THD	–114 dB (typ)	–118 dB	–114 dB
SFDR	116 dB (typ)	121 dB	117 dB
SINAD	96 dB (typ)	96.0 dB	95.4 dB
Circuit power consumption	—	315.6 mW (for Figure 4)	44.28 mW (for Figure 4)

Table 3. Performance Results for Single-Ended Circuit Configuration (Figure 5 and Figure 6)

Parameter	Datasheet Limits	ADS8319 with THS4031	ADS8318 with THS4281	ADS8319 with THS4281
DNL_{MAX}	< 1.5	0.54	0.64	0.65
DNL_{MIN}	> –1	–0.5	–0.56	–0.53
INL_{MAX}	< 2.5	0.62	0.94	0.83
INL_{MIN}	> –2.5	–0.95	–0.4	–0.65
SNR	> 92 dB	93.9 dB	92.5 dB	92.5 dB
THD	–111 dB (typ)	–113 dB	–113 dB	–113 dB
SFDR	113 dB (typ)	115 dB	115 dB	115 dB
SINAD	93.8 dB (typ)	93.8 dB	92.4 dB	92.4 dB
Circuit power consumption	—	205.6 mW (for Figure 6)	55 mW (for Figure 5)	38.44 mW (for Figure 6)

5 Step-Input Settling

For applications where multiple signal channels must be sampled (such as those with a multiplexed input), the step response of the circuit is important. The response of the circuit shown in Figure 6 was studied for a 5-V step-input.

Simulation results are shown in Figure 11. Because of the presence of capacitance C1 (1 nF) in the feedback path, the THS4281 output shows an overshoot. The THS4281 output then settles to 18-bit accuracy (within 20 μV, for a 5-V reference) within 0.54 μs. The voltage at the IN+ pin of the ADS8319 settles to 18-bit accuracy within 1.57 μs.

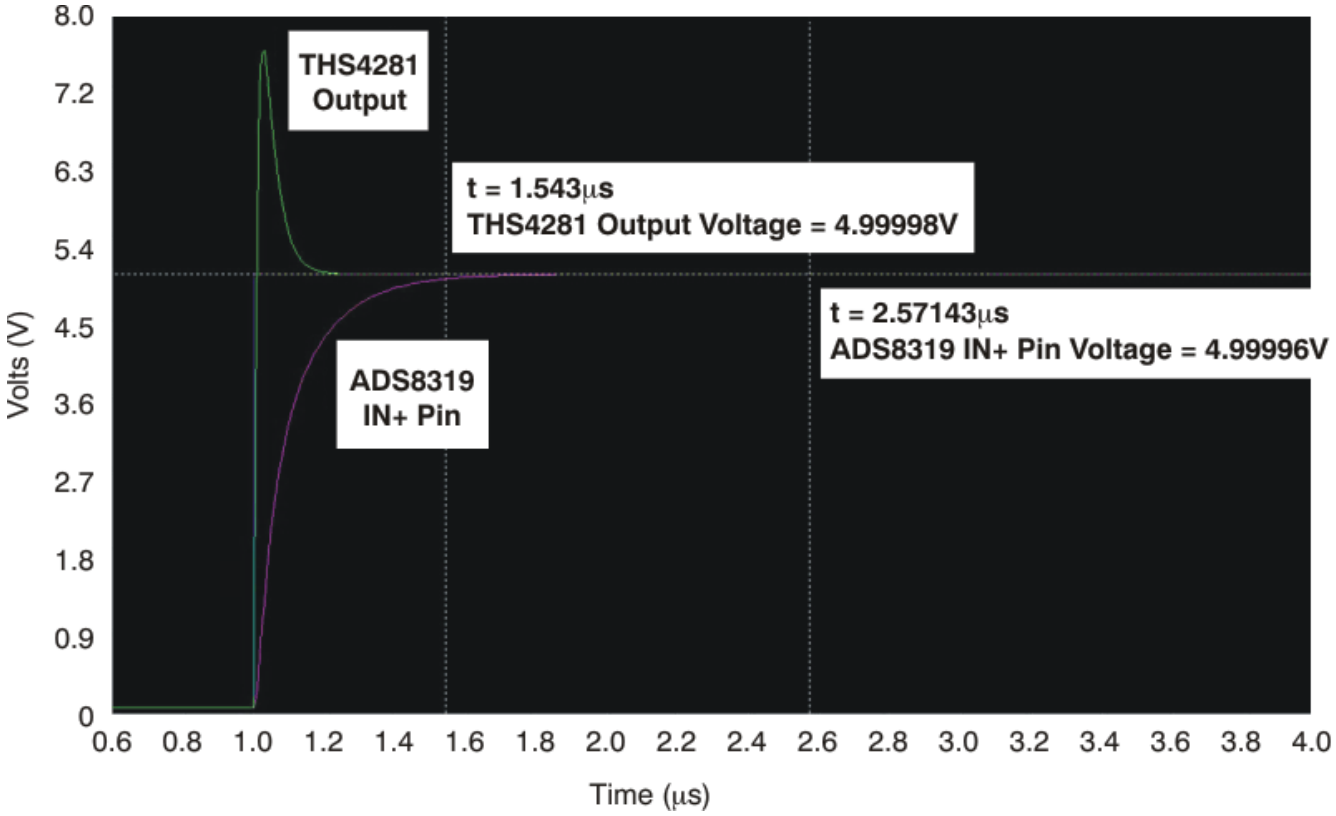

Figure 11. Step-Input Response for Circuit Shown in Figure 6

From the transfer function of the input drive circuit (see Figure 6):

- Natural frequency of oscillation (ω_n) = 47.55×10^6 rad/s
- Damping ratio (ζ) = 0.521
- Settling time (for 18-bit accuracy, output of THS4281) = 0.51 μs
- Settling time required for voltage at IN+ pin of ADS8319 to 18-bit accuracy = $12.5 \times (2 \times 20\Omega) \times 3.3$ nF =1.65 μs

Thus, the numbers obtained from the simulation and the calculated numbers are reasonably consistent. The voltage at the IN+ pin of the ADS8319 should not take more than 1.65 μs to settle to 18-bit accuracy. In a worst-case scenario, if the step-input changes at the end of conversion time (1.4 μs), the total ADC cycle time will be 1.4 μs + 1.65 μs = 3.05 μs. 3.05 μs corresponds to a throughput of 333 kSPS. Thus, the circuit illustrated in Figure 6 (as well as those shown in Figure 4 and Figure 5) can operate with step-inputs only up to 333 kSPS speed.

6 Quick Op Amp Selection Guide

Figure 12 shows the operating region of the THS4281, where the op amp performs very well with ADS8318 and ADS8319. For operation of these ADCs at more than 300-kSPS throughput (with step-inputs), however, we must use an OPA365 or THS4031. This configuration comes with a penalty, though, in the form of the power dissipation required to achieve the desired performance. Figure 12 also illustrates the power dissipation of the OPA365 and THS4031 compared to the THS4281.

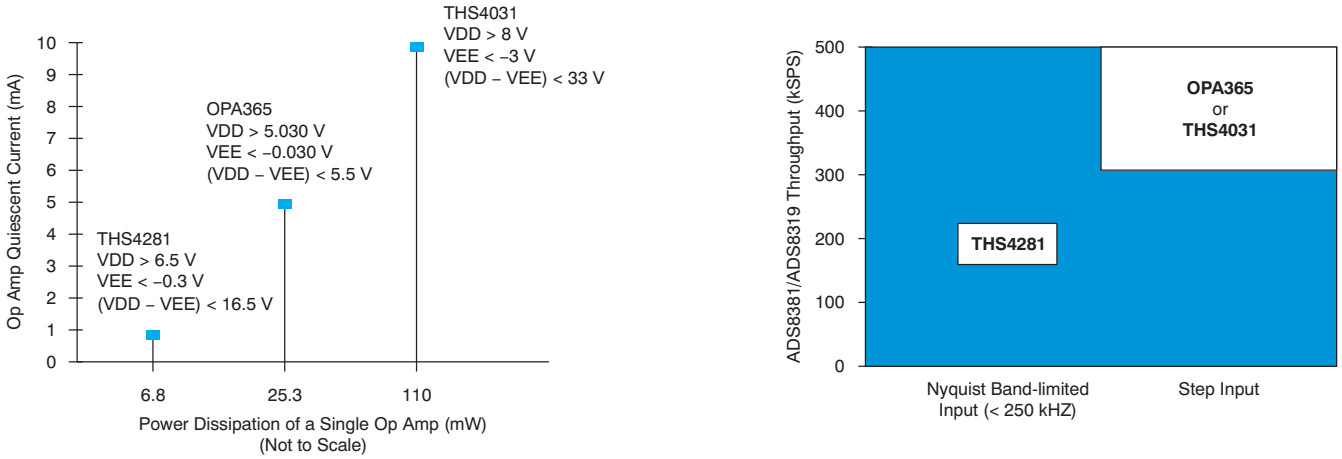

Figure 12. THS4281 Operating Region and Power Dissipation Comparison

When either the OPA365 or the THS4031 is used as an input driver in the circuits discussed earlier (see Figure 4, Figure 5, and Figure 6), some changes should be made to the component values used in the circuit. These changes are summarized in Table 4.

Table 4. Changes Required When THS4031 or OPA365 is Used as Input Driver

Component	THS4281	THS4031	OPA365
R_1	49.9 Ω	Not installed	Not installed
C_1	1 nF	Not installed	Not installed
C	3.3 nF	1 nF	1 nF
Minimum VDD	6.5 V	8 V	5.030 V
Maximum VEE	–0.3 V	–3 V	–0.030 V
Maximum allowed (VDD – VEE)	16.5 V	33 V	5.5 V

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