POWERLINK on TI Sitara™ Processors

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Overview

POWERLINK is a real-time Ethernet fieldbus system based on Ethernet standard IEEE 802.3. It was initially developed by B&R and was introduced in 2001. Since 2003, further development is driven by the Ethernet POWERLINK Standardization Group (EPSG), an independent user organization. The EPSG cooperates with other relevant standardization and user organizations such as CiA or IEC. Free open-source versions of POWERLINK have been available since 2008.

POWERLINK supports Ethernet standard features such as cross-traffic, hot-plugging and different types of network configurations such as star, ring and mixed topologies.

The communication profile of Ethernet POWERLINK is based on CANopen. Process data object (PDO) for process variables and service data objects (SDO) for configuration and remote objects are re-used.

For safety applications POWERLINK can be used with the openSAFETY stack which is also available as open source.

Technology

Introduction

A POWERLINK system consists of a bus master (Managed Node or MN) and several slaves (Controlled Node or CN). The MN controls the bus and defines the timing and polls each CN cyclically during the isochronous phase. During that time, real-time critical data (PDO) will be transferred. The start of the isochronous phase is indicated by an SoC message that is also used to synchronize all slaves. The isochronous phase is followed by an asynchronous phase where all non-real-time critical data such as TCP/IP traffic will happen. This phased approach ensures determinism on the communication bus. Ethernet POWERLINK (EPL) systems can be linked to standard Ethernet networks using gateways.

Be sure to check out the K2E Clock Generation Reference Design

The basic idea is to have strict timing management during a POWERLINK cycle. The managing node starts the synchronous cycle, polls the nodes and finally starts the asynchronous cycle.

- Start of cycle

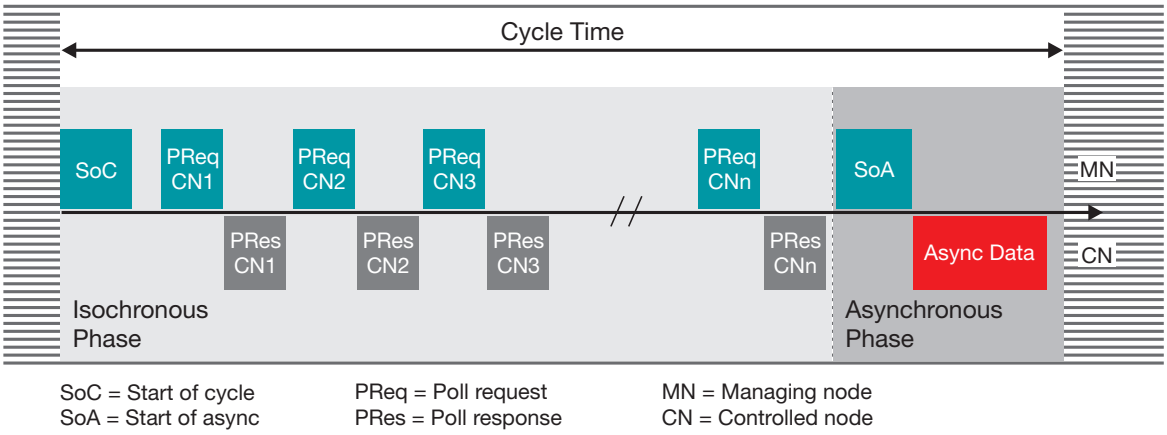


Figure 1: *POWERLINK communication scheme.*

- Poll request
- Poll response by the CN
- Start of asynchronous phase
- Asynchronous data

POWERLINK operates at 100 Mbit half duplex only – the half-duplex mode enables POWERLINK to use repeaters (hubs). The Ethernet hubs used in POWERLINK networks are low-latency class II hubs, introducing less than 460-ns delay. Half duplex comes with the advantage of using low-latency hubs but with the disadvantage of unpredictable collisions (if two nodes access the network in a close timely manner). However the POWERLINK communication scheme eliminates collisions during runtime. Contrary to a switch, a hub can forward an Ethernet frame with an extremely short delay. Combining half-duplex operation with POWERLINK's strict communication scheme provides an extreme low-latency and fully predictable network infrastructure.

In order to support POWERLINK requirements in terms of performance, determinism and low jitter it is required that the underlying media access controller (MAC) supports an auto-reply feature. Processing a poll request in a standard way by going through several levels of software on the Arm® core would introduce unpredictable delays and therefore jitter on the network. As such, the auto-reply feature is required in POWERLINK systems which allows the stack to setup pre-defined answers in registers. Any poll response can then be answered at the lowest level in the system with a minimum delay and jitter. Such a feature is ideally suited to be implemented on members of the Sitara™ processor family containing a programmable real-time unit industrial communication subsystem (PRU-ICSS).

Each EPL device has a unique MAC ID (conforming to 802.3) and a node ID. Node IDs are usually assigned on the device level through switches or dials. Devices implementing a TCP/IP stack on top of POWERLINK also get an IP address consisting of a combination of a defined IP range and their node ID.

POWERLINK solution with Sitara MPU from Texas Instruments

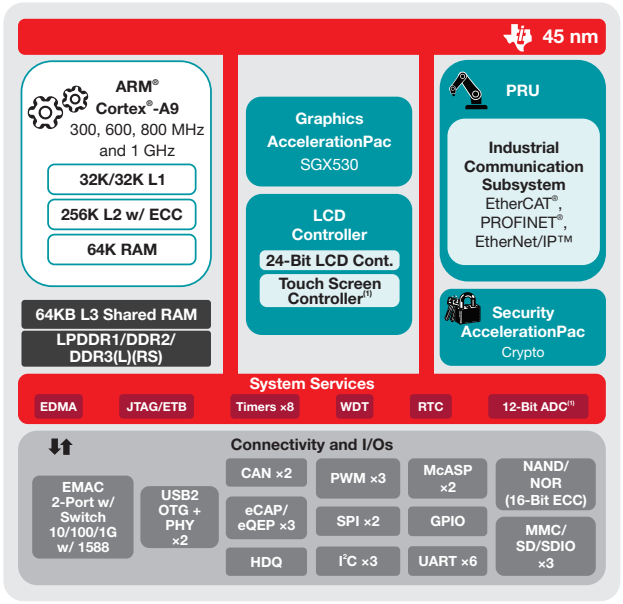
The Sitara processors - including the AMIC110, AM335x, AM437x, and AM57x - are low-power with an Arm Cortex®-A and a broad range of integrated industrial peripherals (**Figures 2-5**). The Sitara family provides scalability to help enable a wide range of applications with a performance range from 300 MHz Cortex-A8 to dual-core 1.5 GHz Cortex-A15.

The AMIC110 and AM335x devices contain one instance of the PRU-ICSS, while the AM437x and AM57x contain two instances. The PRU-ICSS has two dedicated processing cores (Programmable Real-time Units or PRUs) and industrial communication interfaces such as universal asynchronous receiver/transmitter, media independent interface (MII) and management data input/output (MDIO). The two PRU-MII interfaces directly connect to two Ethernet PHY devices and their ports on the board. Now software can be used to implement any kind of Ethernet Media Access Control (MAC) implementation to serve different industrial protocol implementations.

For POWERLINK, TI implemented the openMAC module which is a standard Ethernet MAC with extensions for POWERLINK (e.g., auto-reply and time triggered send functions). Using openMAC on PRU-ICSS and a POWERLINK stack running on an Arm host inside the Sitara processors, it is now

possible to implement an integrated POWERLINK CN or MN. The main features of the TI openMAC implementation are:

- Compliant to openMAC specification
- Two MII interfaces with 100-Mbps full-duplex and half-duplex support
- Three-port hub implementation
- 16 Rx filters
- Ability to filter up to first 31 bytes of Rx packet
- Auto-response feature
- Time stamping of Tx and Rx packets, IRQ generation to host processor
- OS independent driver/Hardware Abstraction Layer (HAL) code



* 800 MHz/1 GHz only available on 15×15 package. 13×13 supports up to 600 MHz.
(1) Use of TSC will limit available ADC channels.

Figure 2: *AM335x SoC block diagram.*

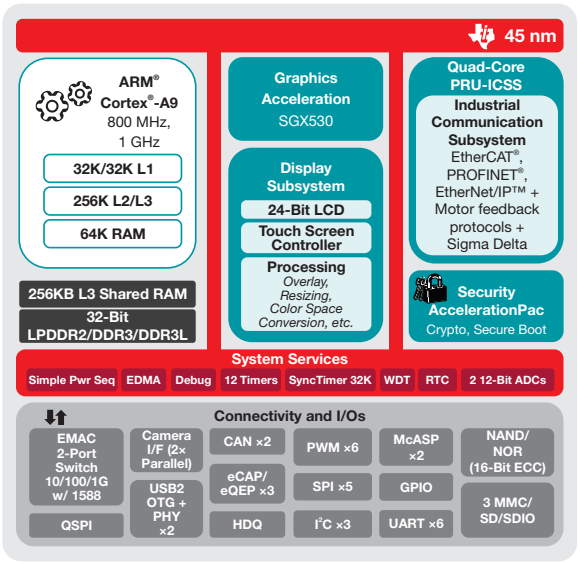


Figure 3. *AM437x Sitara processor block diagram.*

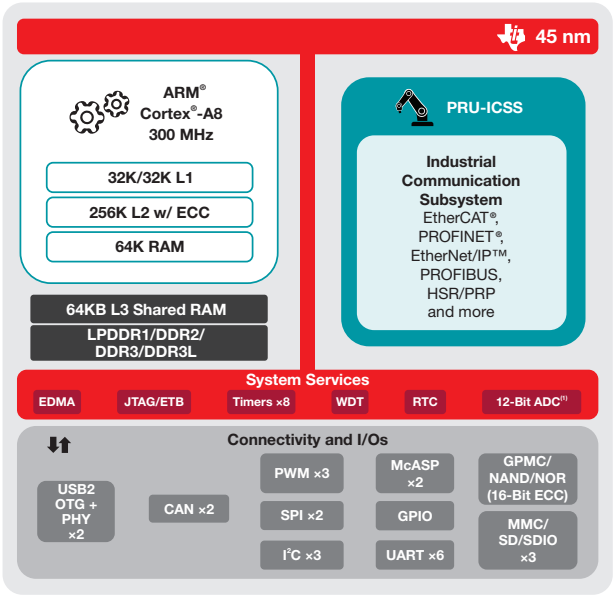


Figure 4. *AMIC110 block diagram.*

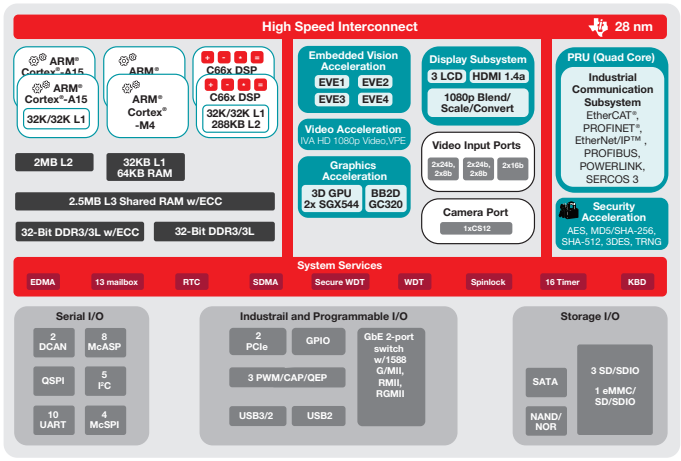


Figure 5. *AM57x block diagram.*

Figure 6 shows an example usage scenario for openMAC. It implements the lower layer of an Ethernet hub that is capable to be used with a POWERLINK stack. Customers can then implement POWERLINK MN on CN solutions on top.

A third-party protocol is available from Port GmbH, Halle, Germany. Port uses its own POWERLINK stack and tools that support customers in creating the required device description files and application code. The solution from port running on TI development boards was officially certified by EPSG.

Port has created a driver to interface with TI POWERLINK PRU firmware and offers features for POWERLINK products according to **Table 1**.

This solution is supported by Port's POWERLINK Design Tool (**Figure 7)** to manage complex object dictionaries.

The design tool:

- **Manages** object dictionary (dynamically or statically)
- **Configures** the POWERLINK stack accordingly
- **Creates the XDD** device description file
- **Creates the application stubs** for the customer's application
- Provides a **documentation** of the object dictionary
- Provides an **automatic, error-free and reproducible measure** to create the configuration

The design tool expands the POWERLINK offering from a simple protocol stack offering to a POWERLINK solution chain.

Development tools

TI also provides low-cost development boards for industrial communication solution. The Industrial Communication Engines (ICEs, see **Figure 8** for an example showing the AM3359 ICE board and Industrial Development Kits) are based on a Sitara

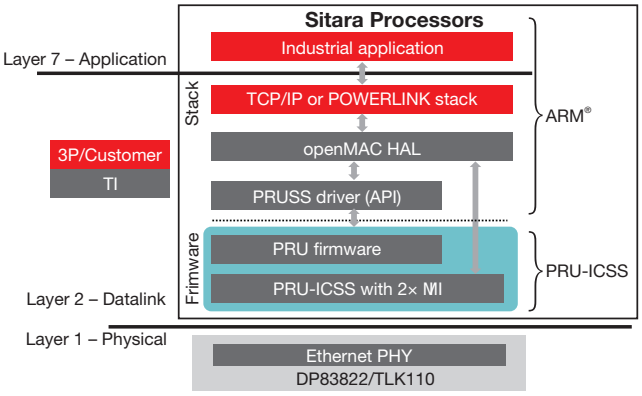


***Figure 6**. openMAC usage example.*

devices. They use many of the SoC peripherals such as SPI, I²C, UARTs and GPIO to drive LEDs, a display and other components such as the TLK110 or DP83822 Ethernet PHY devices on the board. For Ethernet connectivity they support two Ethernet ports that are connected to PRU-MIIs. ICE boards are equipped with SPI- and NOR-based Flash as

Feature	Support
Controlled node functionality	yes
Managing node functionality	–
Isochronous controlled node	yes
Async-only controlled node	yes
PDO producer	yes
PDO consumer	yes
Number of supported transmit-PDOs	1
Number of supported receive-PDOs	1 – 254
Dynamic PDO mapping	yes
Static PDO mapping	yes
IP support	yes
SDO-server	yes
SDO-client	yes
SDO over UDP	yes
SDO over ASnd	yes
SDO over PDO	-
SDO expedited transfer	yes
SDO segmented transfer	yes
Number of supported lines	1
Multiplexing	yes
Usage of nonvolatile memory	yes
CN NMT state machine	yes
Object dictionary	yes
Extended data types	yes
Usage of CANopen profiles	yes
CiA-401 framework support	yes
Frame autoreply support	yes

***Table 1:** Stack features*

well as an SD card interface for permanent storage Port provides an evaluation software package that can directly be applied on the boards. The supplied

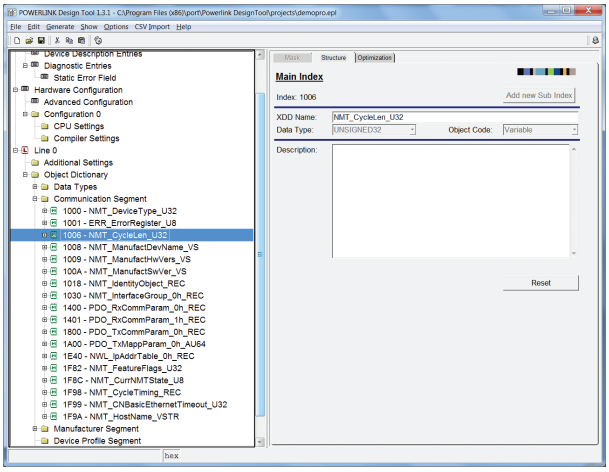


Figure 7: *Port design tool.*

binary application program needs to be copied onto a microSD card. Once inserted, the board can boot from an SDcard and run the POWERLINK CN implementation. Now the associated device description file may be imported into a PLC system with POWERLINK master (MN) functionality. Using the defined input and output data fields, data transfers between MN and CN can be implemented.

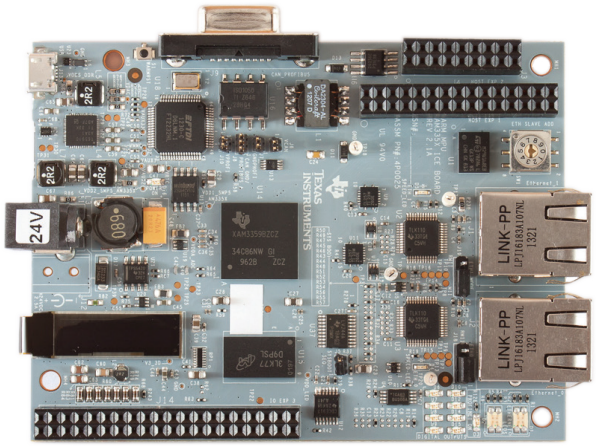


Figure 8: *TMDSICE3359 Industrial Communication Engine (ICE) board.*

The CN output data is associated in the example application with eight LEDs on the board. Data sent from the MN is directly visualized on the board.

The example application based on TI openMAC and Port POWERLINK CN stack currently supports features according to **Table 2**.

Feature	Description
POWERLINK cycle time	200 µs – 10000 µs
Multiplexing	Yes
Async MTU size	300–1500 bytes
Basic Ethernet mode	Yes
SDO	Using ASnd and UDP
Conformance	POWERLINK conformance test version 1.1.0
Ports	2 external Ethernet ports, internal hub

Table 2: *Stack features.*

Further software development can be done using the Processor Software Development Kit (Processor SDK) and protocol-specific software available on the PRU-ICSS industrial software page, which combines SYS/BIOS™ [real-time operating system (RTOS) from TI] and example projects using industrial Ethernet protocols.

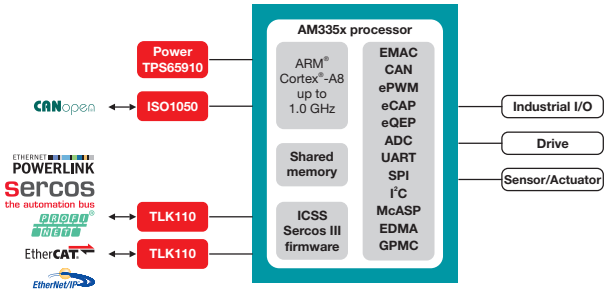


Figure 9: *TMDSICE3359 Industrial Communication Engine (ICE) board system block diagram.*

Summary

The PRU-ICSS inside TI's Sitara family of processors allows implementing real-time critical Ethernet protocols in software. As such, it allows implementation of a variety of industrial communications protocols which otherwise would require an additional external FPGA or ASIC. Working with the third-party Port, TI provides a certified solution for POWERLINK CN implementations on a single System-on-Chip (SoC). Evaluation boards and related software development kits are available for customers to start their own application development. Future Sitara devices will incorporate PRU-ICSS subsystems, too, and therefore provide a scalable environment for all industrial communications needs based on a common system architecture model. Many of the available software components will be directly reusable to allow a fast and seamless transition.

Links and resources

- EPSG: **www.ethernet-powerlink.org**
- TIDEP0028 POWERLINK CN solution: www.ti.com/tool/TIDEP0028
- Sitara processor family: www.ti.com/sitara
- PRU-ICSS industrial software: www.ti.com/tool/PRU-ICSS-INDUSTRIAL-SW
- Port solution on AM335x SoC: www.port.de/en/products/applications/am335x.html

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