Application Report
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Migrating from TMS320DM642/3/1/0 to the TMS320DM648/7 Device

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ABSTRACT

This application report describes issues of interest related to migration from the TMS320DM642/3/1/0 to the TMS320DM648/7 device. The objective of this document is to indicate differences between the two device portfolios. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, see the TMS320DM642, TMS320DM643, or TMS320DM641/0 Fixed-Point Digital Media Processors data manuals [1] [2] [3]; the TMS320DM648/7 Digital Media Processors (DMP) data manual [4]; the TMS320C6000 Peripherals Reference Guide [5] and any associated manual update sheets [6].

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Trademarks

C64x is a trademark of Texas Instruments.

1 Introduction

Migration issues from the DM642/3/1/0 to DM648/7 are indicated with the following symbols:

- S Software modification is required
- H Hardware modification is required
- D The DM642/3/1/0 and DM648/7 devices are different (usually due to added features or enhancements on the DM648/7 device), modifications may be necessary for migration (i.e., different but compatible).

These symbols are included at the beginning of each section.

DM642/3/1/0:

Throughout the rest of this document DM642 refers to all subset devices, including DM642, DM643, DM641 and DM640. Unless otherwise noted, the information contained in the DM642 data manual(s) (see Section 9) should be considered Production Data defined as follows:

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

DM648/7:

Throughout the rest of this document, unless specifically noted, DM648 refers to both DM648 and DM647. Unless otherwise noted, the information contained in the DM648 data sheet(s) (see Section 9) should be considered Production Preview defined as follows:

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

2 DSP Core Differences [S D]

The DM648 family achieves higher performance through an enhanced DSP central processing unit (CPU). The C64x+ architecture adds several new instructions, giving you improved performance for operations used in video applications and other general purpose algorithms.

The C64x+ DSP core is based on the C64x™ DSP core and most C64x software should run without problems after being recompiled for the new core and after being adjusted for memory map differences. The *TMS320C64x to TMS320C64x+ CPU Migration Guide* [7] should reference more information on the DSP core differences. For detailed information, see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* [8] and the device-specific data manual. Changes exist in the following areas that can affect existing code:

- Instruction set
- Registers
- Interrupts
- Enhanced direct-memory access (EDMA) operations
- Timing changes
- Circular addressing

The following new enhancements should be closely monitored to realize performance improvements on the new C64x+ architecture:

- New instructions support increased code efficiency and speed
- New 16-bit compact instructions support increased code compactness
- New SLOOP facility provides improved code compactness and interruptibility for pipelined loops
- Changes to internal memory increases the flexibility of internal memory usage
- New privilege modes support secure operating systems
- New support for exceptions provides new error handling capabilities

3 Peripheral Differences [H D]

Table 1 shows the peripheral differences between the DM648, DM647, and DM642 devices.

Table 1. Peripheral Differences

Peripheral	DM648	DM647	DM642
CPU	C64x+	C64x+	C64x
L1D/L1P	32/32 KB (Configurable as SRAM)	32/32 KB (Configurable as SRAM)	16/16 KB (Cache Only)
L2 RAM	512 KB	256 KB	256 KB
DMA	EDMA3.0	EDMA3.0	EDMA2.0
Timers	4- 32b	4- 32b	3- 32b
Host Ports	32b PCI 66/33 MHz 32b HPI	32b PCI 66/33 MHz 32b HPI	32b PCI 66/33 MHz 32b HPI
Ethernet	2x SGMII (10/100/1000)	1x SGMII (10/100/1000)	1x MII (10/100)
VLYNQ	YES	YES	NO
External Memory Interface	DDR2-532 32b 266 MHz Clock	DDR2-532 32b 266 MHz Clock	SDRAM-133 64b 133 MHz Clock
EMIFA 16 Bit	YES	YES	NO
Video Port	5- 16b	5- 16b	3- 20b
VIC	YES	YES	YES
McASP	10 Channels	10 Channels	8 Channels
McBSP	NO	NO	2x
UART	YES	YES	NO
SPI	YES	YES	NO
I2C	YES	YES	YES
Video Imaging Co-Processor	YES	YES	NO

3.1 Ethernet Subsystem [H]

The Ethernet subsystem on the DM648 utilizes SerDes technology to reduce pin count and improve performance. The SerDes Gigabit Media Independent Interface (SGMII) communicates with a PHY to achieve 10/100/1000 Ethernet rates. The DM648 has two SGMII ports with an internal switch to allow packets to be received and processed or passed from one port to the next. This improvement allows high speed communication between devices, as well as a standard interface for commonly used Ethernet protocols.

The Ethernet subsystem is a stand-alone peripheral and is not multiplexed with any other peripherals.

In addition, the DM648 can boot over the Ethernet subsystem. For more details, see Section 8, Resetting and Booting [D] of this document.

3.2 External Memory Interface [H]

3.2.1 System Memory

The DM648 utilizes standard DDR2-SDRAM as its main system memory. The DDR2 memory controller interface can be clocked up to 266 MHz, yielding a data rate of 533 MHz. The interface bus is 32-bits wide, providing a theoretical data rate of 2132 Mbps. This data rate achieves more than 2x the performance provided by the DM642 external memory interface (EMIFA). Another advantage of this improved interface is that it is dedicated; there is a second memory interface that allows connectivity to both synchronous and asynchronous interfaces.

To help get to market faster, a DDR2 reference design application report is provided and gives you an understanding of what tolerances must be adhered to in order to assure correct DDR2 operation.

3.2.2 Secondary Memory [D]

The DM648 provides a secondary external memory interface (EMIFA) which can be operated either synchronously or asynchronously, allowing connectivity to various devices such as NOR flash, FGPAs, CPLDs, or other such devices. The interface is 16-bits wide and can be clocked up to 100 MHz, providing a theoretical throughput of 200 Mbps.

The secondary interface is used for booting NOR flash. For more details, see Section 8, Resetting and Booting [D] of this document.

3.3 Video Ports and VIC [H]

The video port architecture is the same between the DM648 and DM642 device families. There are five 16-bit video ports on the DM648 device, compared to three 20-bit video ports on the DM642 device. The video port modes supported for each device are compared in Table 2.

Table 2. Video Port Modes Comparison

Video Port Modes	Maximum Frequency (MHz)	DM648	DM642
Capture			
8b - Single Channel	80	X	X
10b - Single Channel	80		X
16b - Dual Channel	80	X	X
20b - Dual Channel	80		X
8b - Y/C Capture	80	X	X
10b - Y/C Capture	80		X
8b - RAW Capture	80	X	X
10b - RAW Capture	80		X
16b - RAW Capture	80	X	X
20b - RAW Capture	80		X
8b - TSI Capture	27	X	X
Display			
8b - Single Channel	110	X	X
10b - Single Channel	110		X
8b - Y/C	110	X	X
10b - Y/C	110		X
8b - RAW	110	X	X
10b - RAW	110		X
16b - RAW	110	X	X
20b - RAW	110		X
8b - Dual Sync	110	X	X
10b - Dual Sync	110		
VIC	27 MHz ±10%	X	X

3.4 McASP [D]

The multi-channel audio serial port (McASP) is similar on both the DM648 and the DM642 devices. The DM648 McASP provides two additional data pins to increase the channel quantity to 10 channels.

3.5 McBSP [H]

The DM642 contained 2 multi-channel buffered serial port (McBSP) peripherals which could be used for standard serial port communications and other time division multiplexed streams. The DM648 McASP can be used to interface to Audio Codecs.

3.6 UART [H]

A universal asynchronous receiver/transmitter (UART) peripheral has been added to the DM648 device. The UART can be used for general-purpose communications and control in various applications. On the DM648 device, this peripheral is multiplexed with the serial peripheral interface (SPI) peripheral.

It is possible to boot the DM648 over the UART peripheral. For more details, see Section 8, Resetting and Booting [D] of this document.

3.7 SPI [H]

An SPI peripheral has been added to the DM648 device. The SPI can be used for general-purpose communications, control, and storage via a serial electrically erasable programmable read-only memory (EEPROM). The SPI peripheral is multiplexed with the DART peripheral.

It is possible to boot the DM648 over the SPI peripheral. For more details, see Section 8, Resetting and Booting [D] of this document.

3.8 Video and Imaging Co-Processor (VICP) [D]

The video and imaging co-processor (VICP), is new to the DM648 device. The VICP is targeted toward complex algorithms (i.e., motion estimation) but, can be used for pre- and post-processing algorithms such as color-space conversion, resizing, and filtering.

The DM648 VICP is similar to the VICP in the DM6446 system-on-chip (SoC). The VICP is unique on the DM648 device in that, by default, it operates at a CPU/2 or CPU/3 clock frequency, depending on what the CPU speed is. When the CPU speed is greater than 720 MHz, the VICP must run at a CPU/3 clock frequency.

4 Power Supply Differences [H]

The core voltage of the DM648 is 1.2 V with ±5% tolerance; reduced from 1.4 V with ±5% tolerance on the DM642. Table 3 shows the relationship between operating voltages, frequencies, and CV_{DD} tolerances supported on the DM648 device. The DV_{DD} (I/O voltage) is unchanged (3.3 V ± 5% tolerance). The DDR and SGMII peripherals require an additional supply rail (1.8 V ± 5% tolerance).

Table 3. Power Supplies for DM648

CV_{DD}	DV_{DD}	1.8 V	Maximum Frequency
1.2 V ± 5%	3.3 V ± 5%	1.8 V ± 5%	720 MHz
1.2 V ± 5%	3.3 V ± 5%	1.8 V ± 5%	900 MHz

The power consumption for the DM648 device increased due to the higher performance and memory sizing discussed in previous sections. In systems where the DM648 replaces the DM642, the power supply circuit on the board must be modified to support this change.

5 Device Identification [D]

The DM648 device is a new product. The JTAG (BSDL) ID and Silicon revision ID are different than the DM642 device. Table 4 identifies the JTAG (BSDL) ID differences between the DM642 and the DM648.

Table 4. JTAG (BSDL) ID for DM648

Device	JTAG (BSDL) ID				
	Memory Address	Variant	Part Number	Manufacturer	LSB
DM648	0×0204 9018	0000	1011 0111 0111 1010	0000 0010 111	1
DM642	0×01B3 F008	0000	0000 0000 0111 1001	0000 0010 111	1

The silicon revision ID differences between the DM642 and DM648 can be found in the device-specific data manual.

6 Package and Pins [H D]

The DM648 and the DM642 devices use different mechanical packages. The physical dimensions and pin out of the packages are also different. Table 5 lists the variations between the DM648 and the DM642 devices.

Table 5. Package Differences Between DM648 and DM642

Device	Package Characteristics			
	Size (mm)	Pitch (mm)	No. of Pins	Package Designator
DM648	19×19	0.8	529	ZUT
DM642	23×23, 27×27	0.8, 1.0	548	ZDK, ZNZ

7 PLL/CPU Clock [H]

The phase-locked loop (PLL) on the DM648 device is improved from the DM642. The DM648 has two internal PLLs, one dedicated to the DDR interface, and the other for the CPU and remaining peripherals. The DM642 PLL only supported two multiply modes, x6 and x12.

While the DM642 required external pins to configure the PLL-multiply modes, the DM648 PLL multiply modes are programmed through register accesses.

Available clock frequencies for the DM648 range from 400 MHz – 900 MHz, depending on the silicon speed grade.

8 Resetting and Booting [D]

The reset controller for DM648 has several enhancements that allow the application to control peripherals on an individual basis. Once the DSP comes out of Master Reset, the individual peripherals must be enabled through the reset controller. I2C, SPI, UART, and EMIFA FASTBOOT require data for boot to be stored in an application image script (AIS) format. AIS is a Texas Instruments, Inc. proprietary format for boot images.

The DM648 has additional bootmodes that are not available on the DM642. Table 6 lists the available bootmodes and their associated description.

Table 6. Description of Available Bootmodes on DM648 and DM642

Device		Boot Type	Description
DM642	DM648		
X	X	Emulation	DSP starts execution at pre-defined start address: • DM648 → 0x00100000 • DM642 → 0x00000000
X	X	Host Port	This mode allows booting the device over the Host port. Depending on configuration, this can be either PCI or HPI.
X	X	EMIF	Allows booting over the asynchronous interface. DSP pulls data from a memory device such as a NOR flash.
	X	I2C	This mode starts downloading code from an I2C EEPROM of address 0x50. The code must be stored in an AIS format.
	X	SPI	This mode starts downloading code from an SPI EEPROM on CS0. The code must be stored in an AIS format.
	X	UART	This mode must be booted using a 27-MHz clock. This forces the baud rate to 115200. The UART sends a *BOOTME* request to the UART peripheral and waits for a response along with code from a host processor.
	X	Ethernet	This mode allows booting over the Ethernet. The Ethernet port starts out by sending a BOOTP request. Once acknowledged by a BOOTP server, the DSP can be booted.

9 References

1. *TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor Data Manual* (SPRS200)
2. *TMS320DM643 Video/Imaging Fixed-Point Digital Signal Processor Data Manual*(SPRS269)
3. *TMS320DM641/TMS320DM640 Video/Imaging Fixed-Point Digital Signal Processors Data Manual*(SPRS222)
4. *TMS320DM647/TMS320DM648 Digital Media Processors* (SPRS372)
5. *TMS320C6000 DSP Peripherals Overview Reference Guide* (SPRU190)
6. *TMS320C6000 Peripherals Reference Guide – Manual Update Sheet for SPRU190D* (SPRZ122)
7. *TMS320C64x to TMS320C64x+ CPU Migration Guide* (SPRAA84)
8. *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732)

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