Technical White Paper

Space Power Supply for the STAR-Tiger SpaceFibre Routing Switch

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ABSTRACT

Modern space-rated Field Programmable Gate Arrays (FPGAs) have enabled entirely new system architectures and increased data throughput. These advances in FPGAs require technology to be able to support data-handling applications at high data rates. SpaceFibre is a high-performance, high-availability datalink and network technology specifically designed for spaceflight applications, where the technology is used to transfer data from instruments to processing and storage elements onboard the spacecraft, and to the downlink transmitter that sends data to ground. STAR-Tiger is a ten-port SpaceFibre routing switch with a bisectional bandwidth of 100 Gbit/s developed by STAR-Dundee. This paper discusses in detail the power-supply design for the STAR-Tiger SpaceFibre routing switch.

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1 SpaceFibre and STAR-Tiger

SpaceFibre is the latest generation of SpaceWire network technology for spacecraft onboard data-handling applications. SpaceFibre runs over electrical or fiber-optic cables, operates at very high data rates, and provides built-in quality of service (QoS), and fault detection, isolation and recovery (FDIR) capabilities. SpaceFibre provides high-performance, high-reliability, and high availability, making it an excellent choice for many demanding network applications, including spacecraft payload data-handling. A SpaceFibre network is made up of links, endpoints and routing switches. Links connect endpoints and routing switches together to form a SpaceFibre network.

Figure 1-1 shows the STAR-Tiger SpaceFibre routing switch which is used for transferring data at high data-rates between instruments, mass-memory, data compressor, data processors, and downlink transmitters. The switch is also used to provide the control network used by the control computer to manage both the network and the equipment attached to the network. The STAR-Tiger routing switch is a high-performance SpaceFibre routing switch implemented using STAR-Dundee SpaceFibre IP.

Figure 1-1. STAR-Tiger SpaceFibre Routing Switch

As Figure 1-2 shows, STAR-Tiger comprises three circuit boards:

1. A power-supply board (bottom) which has nominal and redundant power input selection and delivers the five main power rails to the FPGA. Other power rails are supplied by regulators on the other two boards. Texas Instruments space-rated power-supply components are used.
2. An FPGA board (middle) containing the Xilinx® KU060 FPGA. The PCB footprint accommodates either the commercial part, industrial part or the radiation-tolerant part. An industrial grade FPGA was used. The FPGA is surrounded by six Elara connectors which carry the SpaceFibre electrical signals. Each connector provides four lanes of SpaceFibre. Two connectors each carry one quad-lane port and the other four connectors each carry two dual-lane ports.
3. A configuration and scrubbing board (top) which is used to configure and monitor the KU060 FPGA. Configuration is from EEPROM or via a SpaceWire interface. The EEPROM can be programmed over SpaceWire.

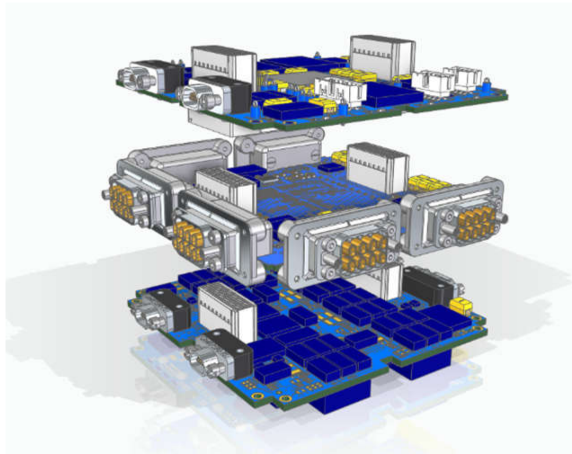

Figure 1-2. STAR-Tiger Routing Switch Board Arrangement

These three boards are shown in Figure 1-3 through Figure 1-5 in various stages of integration with the STAR-Tiger housing.

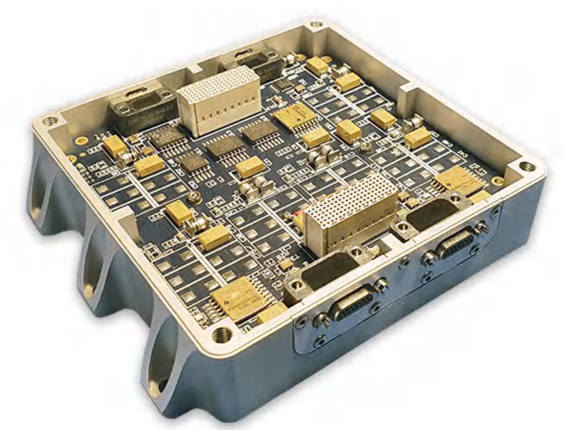

Figure 1-3. STAR-Tiger Power-Supply Board

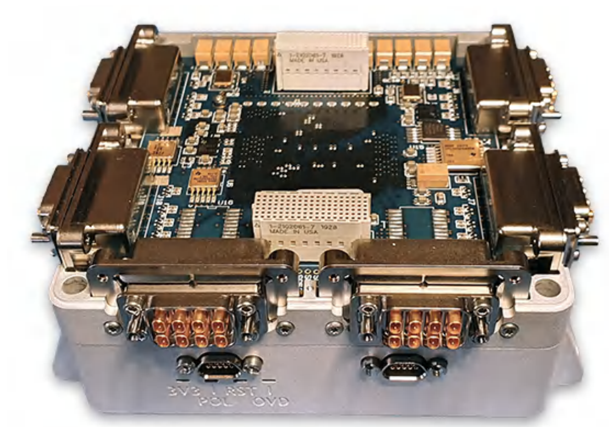

Figure 1-4. STAR-Tiger FPGA

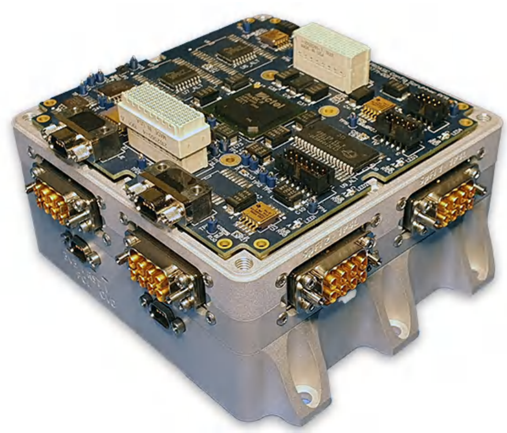

Figure 1-5. STAR-Tiger Configuration Board in Housing

The STAR-Tiger SpaceFibre routing switch forms the heart of the SpaceFibre network that connects the instruments, data-handling, and downlink telemetry elements together. STAR-Tiger is capable of data rates up to 19Gbps on the quad-lane ports and 9.6Gbps on the dual-lane ports, with an aggregate throughput (all ports in both directions) of around 200Gbps. The SpaceFibre routing switch is a spaceflight Technology Readiness Level (TRL) 5-6 level design.

2 STAR-Tiger Power-Supply Design

The power-supply board in the STAR-Tiger unit provides the primary power rails to the Xilinx KU060 FPGA being used to implement the routing switch. The STAR-Tiger power-supply design is shown in Figure 2-1, along with a photograph of the board in Figure 2-2. The STAR-Tiger power-supply board uses the following space-rated power-supply devices from Texas Instruments: TPS7H2201-SP, TPS50601A-SP, TPS7H4001-SP, TPS7H1101A-SP, and the TPS7A4501-SP. All these devices are class V devices and qualified up to Total Ionizing Dose (TID) = 100 krad(Si) and LET = 75 MeV-cm^2/mg.

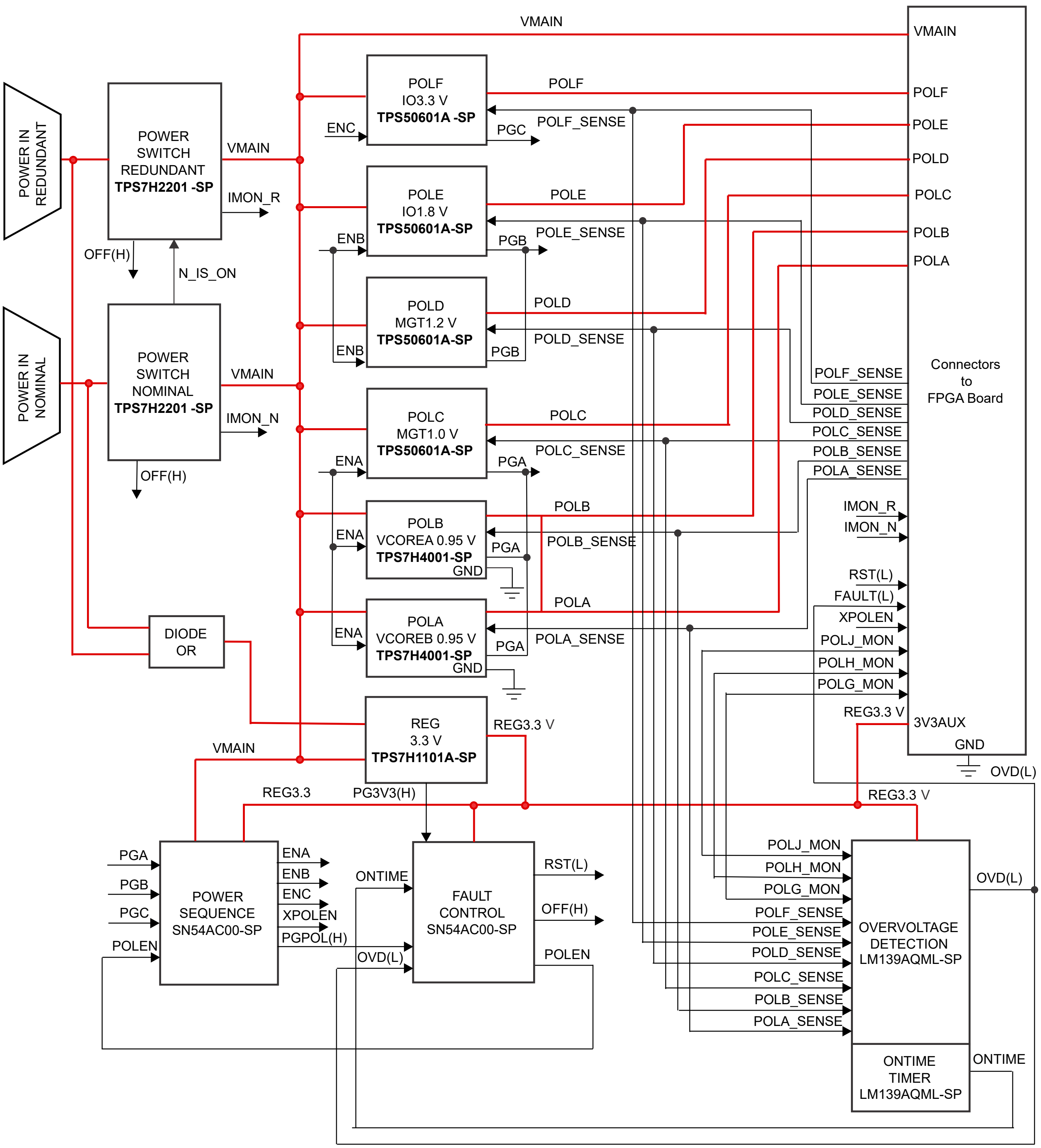

Figure 2-1. STAR-Tiger Power-Supply Block Diagram

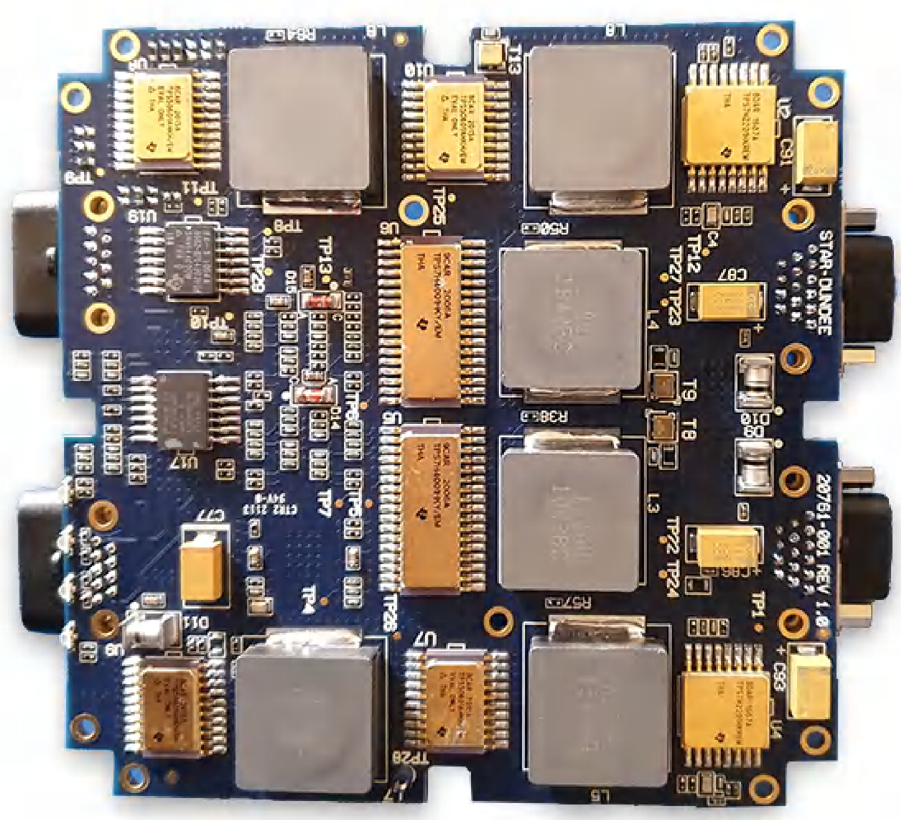

Figure 2-2. STAR-Tiger Power-Supply Board

2.1 Power Inputs

There are two power inputs to the power-supply board, PWR-N and PWR-R (nominal and redundant, respectively). The power input is nominally 5 V ±5% and up to 12 A. Each power input goes to the TPS7H2201-SP device, a power switch that is used to switch power from either the nominal or the redundant power input to an array of point-of-load (POL) converters. The power switches are controlled by a fault detection circuit using the OFF(H) signal which, when asserted, switches off the power switches. During normal operation only one power switch is provided with power.

When power is applied to the nominal power input, the nominal power switch is turned on and the redundant one turned off. When power is applied to only the redundant power input, the nominal power switch is turned off and the redundant one turned on. When power is applied to both nominal and redundant power inputs, the nominal power switch is turned on and the redundant one turned off, so that power is drawn from the nominal power input only.

The power switches protect the SpaceFibre routing switch from reverse polarity and overvoltage up to 7 V. The switched 5-V rail provides the main supply voltage (Vmain) to several POL DC-DC converters and to a linear regulator. Each of these devices can operate with an input voltage of up to 7 V. The power switches provide overvoltage protection which switches off the Vmain power if the input voltage exceeds the maximum power input voltage.

The power switches have overcurrent and overtemperature protection and also a current sense output. The overcurrent limit is set to 17.6 A maximum, which considers the normal maximum current, current inrush during power up, and 20% tolerance on the overcurrent limit setting. Power is switched off when the overcurrent condition has been present for around 1 ms. There are two current sense outputs, IMON, one on each power switch device.

2.2 KU060 Power Rails

Vmain from the power switches is used to drive the POL converters which provide the POLA, POLB, POLC, POLD, POLE, and POLF output voltage to the KU060. For a Xilinx KU060 FPGA, these correspond to VCOREA0.95V, VCOREB0.95V, MGT1.0V, MGT1.2V, IO1.8V, and IO3.3V power rails respectively. Two TPS7H4001-SP regulators provide the core rail supply (POLA, POLB), and four TPS50601A-SP regulators are used for POLC, POLD, POLE, and POLF. The output from each POL converter is passed to the connector on the power-supply board, which is used to provide power to the FPGA and other boards. VCOREA0.95V and VCOREB0.95V are connected together for the Xilinx KU060 FPGA used in STAR-Tiger.

A voltage sense signal is also provided for each POL converter on another connector. Each sense signal is connected close to the load on the FPGA board and senses the voltage at the load, so that each POL can adjust the voltage to the required level.

Each POL converter has an output undervoltage and overvoltage detection circuit which checks that the output voltage is within 94 – 106% (typical), 97 – 103% (worst-case) of the nominal value. If this voltage goes outside 91 – 109% (typical), 90 – 110% (worst-case) of the nominal value, the power good (PG) pin of that device is de-asserted pulling the corresponding PGx signal low which propagates through a chain of POL converters causing PGPOLx(H) to be de-asserted. A separate overvoltage detection circuit is used to improve accuracy of the overvoltage threshold.

Each POL converter is enabled by an EN input and indicates when the output has reached, or is close to, the required output voltage by asserting an open-drain power good signal. The POL converters are grouped into three groups:

- POLA, POLB, and POLC (KU060 VCOREA0.95V, VCOREB0.95V, and MGT1.0V, respectively)
- POLD and POLE (KU060 MGT1.2V and IO1.8V, respectively)
- POLF (KU060 IO3.3V)

POLs in a group are enabled by the same enable signal and generate PG only when all the POLs in the group have reached close to their nominal output voltage. The groups are arranged as follows:

- Group A enabled by ENA, generating PGA: POLA, POLB, and POLC
- Group B enabled by ENB, generating PGB: POLD, POLE
- Group C enabled by ENC, generating PGC: POLF

Table 2-1 shows a summary of the KU060 power rails used in the SpaceFibre switch, the maximum current capability, dynamic load, and voltage transient for which the rails were designed.

Table 2-1. KU060 Power Rails in the SpaceFibre Routing Switch

DC/DC Converter	KU060 Rail	Output Voltage (V)	Current Capability (A)	Maximum Dynamic Load (A)	Voltage Transient Under Maximum Dynamic Load (mV)
TPS7H4001-SP (POLA, POLB)	VCCINT VCCINTIO VCCBRAM	0.950	36	8	±27
TPS50601A-SP (POLC)	VMGTAVCC	1.000	6	2	±10
TPS50601A-SP (POLD)	VMGTAVTT VMGTAVTTRCAL	1.200	6	2	±10
TPS50601A-SP (POLE)	VCCAUX VCCAUXIO SYSMON1.8V VCCO1.8V	1.800	6	2	±12
TPS50601A-SP (POLF)	VCCO3.3V	3.218	6	4	±23

POLF was configured to 3.218 V (instead of 3.3 V) to allow sufficient margin between the operating maximum voltage and the absolute maximum voltage rating of the KU060. The operating maximum voltage includes regulation and overvoltage detection requirements across all conditions.

2.3 Power Sequence

A power sequencing circuit is used to determine the order of powering each group. For the KU060 FPGA, the following sequence is followed:

- Group A, POLA, POLB, and POLC (VCORE0.95 V and MGT1.0 V), enabled when Vmain > a threshold voltage
- Group B, POLD and POLE (MGT1.2 V and IO1.8 V), enabled when PGA is asserted, that is, POLA, POLB, and POLC have all reached close to their nominal voltage
- Group C, POLF(IO3.3 V), enabled when PGB is asserted, that is, POLD and POLE have both reached close to their nominal voltage
- A PGPOLx(H) signal is asserted by the power sequencing circuit when PGC is asserted, that is, when all the POL converters have reached and remain at close to their nominal voltages, the PGPOLx(H) signal is asserted.

2.4 Fault Protection

To make sure that all the POL converters are switched off in the event of one of them failing, those upstream on the EN chain are disabled by a fault control circuit.

The Xilinx KU060 FPGA has tight tolerances on the supply rails and overvoltage limits which are close to the operating voltage. This means that it was not possible to use the power good signals from the POL converters for overvoltage detection. A separate overvoltage detection circuit was used. This comprises a voltage reference (LM4050QML-SP) and set of comparators (LM139AQML-SP), one for each POL converter, which compares the sensed voltage against the maximum permitted value. If an overvoltage is detected, the overvoltage detection circuit asserts the OVD(L) signal. In addition, there are three additional overvoltage detection circuits on the power-supply board that can be used to monitor voltages on other boards in the STAR-Tiger unit and switch off the unit if a potentially damaging fault occurs. Additional POL converters on other boards are monitored by overvoltage circuitry on those boards. If an overvoltage is detected, a FAULTx(L) signal is asserted which drives the OVD(L) signal on the power-supply board, disabling power.

An additional POL enable signal, XPOLEN, is provided for the external POL converters on the other boards in the STAR-Tiger unit. When XPOLEN is asserted the external POL converters are enabled.

The fault control circuit comprises a reset timer, ONTIME, (LM139AQML-SP), and some logic gates (SN54AC00-SP) which are powered by a 3.3-V regulator, the TPS7H1101A-SP, that is powered by Vmain. When the input power switch turns on, the timer is powered by the regulator and the output remains asserted for a power-on timeout period. This power-on timeout is set to be longer than the maximum expected time for the POL converters to all power up and for PGC to be asserted. No faults can be detected during this initial power-up interval. The power-on timeout is also used to provide a system reset signal. The following faults can be detected:

- The POL converters have not reached their power good state in the expected time period. This condition is detected by PGPOLx(H) not being asserted before the power-on timeout timer expires. The POL converters on the other boards are linear regulators and do not have power good outputs.
- One or more POL converters becoming overvoltage, undervoltage, or overtemperature. This condition is detected by the POL converter with the fault de-asserting the power good signal which propagates along the POL power-good and power-enable chain resulting in PGPOLx(H) being de-asserted. The fault is detected when PGPOLx(H) is de-asserted at any time after the power-on timer has expired.
- The overvoltage detection circuit detects that one of the sensed voltages has exceeded a set threshold value and is in danger of damaging the FPGA. When this condition is detected on any of the sensed voltages, the OVD(L) signal is asserted.
- There are also two linear regulators on the FPGA board. POLH is a TPS7H1101A-SP LDO regulator providing 1.2-V VMGTAVTTRCAL and POLJ is a TPS7A4501-SP linear regulator providing 3.3 V for the SpaceWire transceivers on the FPGA board. POLH and POLJ are also monitored by the overvoltage detection circuit on the power-supply board.

- POLH and POLJ are monitored by overvoltage detectors on the power-supply board using the signals POLH_MON and POLJ_MON. POLG_MON is used to monitor the MGTVCCAUX rail on the FPGA board.
- There are three further TPS7A4501-SP linear regulators on the configuration and scrubbing board which are monitored by local overvoltage comparators. When an overvoltage fault is detected, the FAULTx(L) signal is brought low. FAULTx(L) on the FPGA and other boards is connected to OVD(L) on the PSU board, so when FAULTx(L) is brought low, the power switches are turned off and the POL converters disabled.
- Overtemperature of the FPGA or the FPGA board is detected by a TMP461-SP temperature sensor. This sensor is located on the FPGA board which monitors local (board) or remote (FPGA) temperature and which asserts the FAULTx(L) output when an overtemperature condition occurs.

When a fault occurs, the fault control circuit disables the POL converters and asserts the OFF(H) signal, switching off the two power switches. The fault control circuit and comparators are powered from the 3.3-V regulator (REG_3V3), which is powered directly from the 5-V nominal or redundant inputs. Diode ORing is used to combine these two power sources together for the REG_3V3 supply because the load is low. Since the fault control circuitry is not switched off by the power switches, the power switches remain disabled once a fault has occurred. To recover from this fault condition, power-down both the nominal and redundant 5-V inputs and to then turn one on again.

The REG_3V3 supply also provides the 3V3AUX supply to other boards which is used to power the overvoltage detection circuits on those boards.

3 Conclusion

The need to support data-handling applications at high data rates in satellites has increased significantly with modern FPGAs. The STAR-Tiger routing switch, using the SpaceFibre network protocol implementation from STAR-Dundee, successfully demonstrates data transfer supporting these high demands. A space-rated power design for this SpaceFibre routing switch was discussed in detail. The power design includes redundant power inputs, sequencing, and fault protection to provide a robust and reliable system-level design in satellite applications.

4 Acknowledgment

The STAR-Tiger SpaceFibre routing switch was the primary element of the payload data-handling network for the European Union Hi-SIDE project. The Hi-SIDE project received funding from the European Union’s Horizon 2020 research and innovation program under grant agreement No 776151.

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