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The old analog power meters that were used to measure commercial and residential power usage are being replaced with more intelligent electronic meters (eMeters). These eMeters communicate either through wired or wireless communication to the power company. These meters are designed for single, dual, and/or three phase operation and use a 2-W to 7-W offline buck or flyback converter for the power supply. [Figure 1](#) shows a functional block diagram of a two phase eMeter. This application note reviews design considerations for eMeter applications using the [UCC28722](#) primary-side regulation (PSR) controller. This information is supplemental to the [UCC28722/20](#) Design Example/Application Note ([UCC28722 Data Sheet SLUSBL7](#) and [UCC28722/UCC28720 5W Design Example SLAU700](#)).

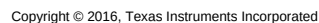


Figure 1. Functional Block Diagram of a 2-Phase eMeter

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eMeters are used universally and are designed for a wide variety of input voltage ranges. For single phase applications the input voltages generally range from 85 V AC to 265 V AC. One eMeter design for India, however, has input specifications of 48 V AC to 270 V AC. Some design requirements may require the eMeter bias supply to work with a single phase or multi-phase systems, where the input range is 85 V AC to 480 V AC.

At 480-V AC input, the eMeter's internal bias supply could see a peak-input voltage of roughly 679-V peak (VIN). To reduce the voltage stress on the input bulk capacitor (CIN), designers have used two 400-V capacitors in series, which requires each capacitor to have twice the capacitance needed for input ripple voltage and holdup requirements. To reduce the voltage stress on the eMeter's step down converter's main switch (Q2), some designers use a simple series pass regulator (R1, D1 and Q1). Refer to Figure 2 for a functional schematic.

NOTE: Even though the series pass regulator reduces the voltage stress on the eMeter's bias supply switch (Q2), this circuitry will hurt the bias supply's overall efficiency.

Due to this reduction in system efficiency, it is not recommended to use a series pass regulator before the eMeter's bias supply. It would be better to find a higher voltage rated FET, or even better, a power supply controller that can drive a bipolar junction transistor (BJT) for the switch.

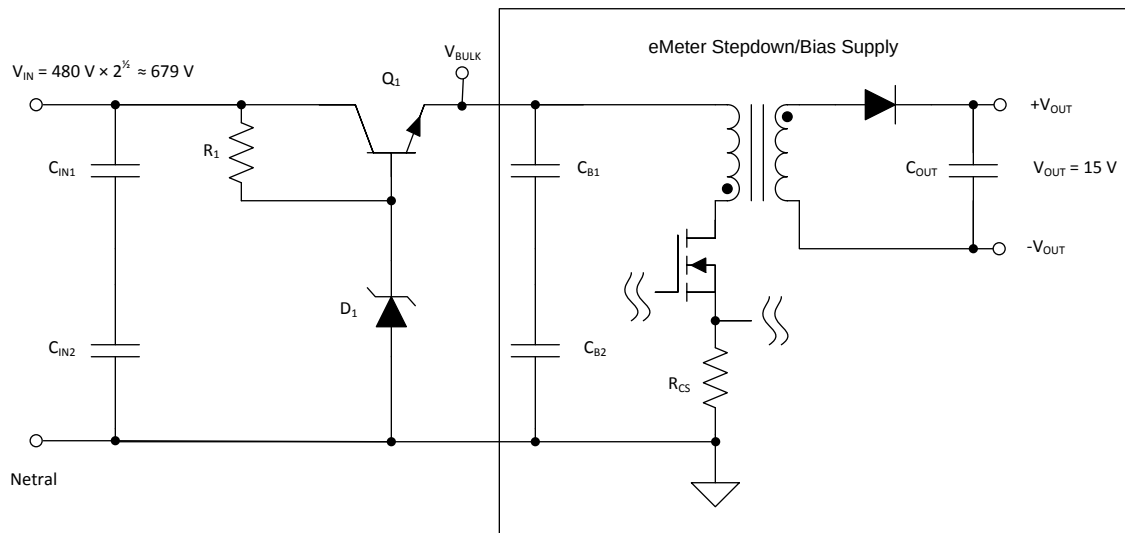


Figure 2. Schematic of eMeter Bias Supply with Series Pass Pre-regulator (R1, D1, Q1)

Both the offline flyback converter and offline buck converter use a bridge rectifier to convert the AC line voltage to a DC voltage. These converters typically have a power factor (PF) of 0.45. There is an ANSI standard that requires the input power of an eMeter to be less than 20 VA. To meet this standard, it is required that the load of the bias supply be much less than 20 VA. If an eMeter's output power requirement (POUT) is 6 W, the converter needs to be designed for greater than 67% efficiency (η) at full load based on the ANSI standard and the PF of the offline step-down converter. To make it easier to meet this efficiency requirement it is advisable to not use the series-pass regulator circuit as presented in Figure 2.

$$PF = \frac{\eta}{20VA} = 0.45 \quad \eta \geq \frac{P_{OUT} \times 100}{PF \times 20VA} \approx 67\% \quad (1)$$

To keep the bias supply design cost effective, green, and efficient, it is ideal to use TI's [UCC28722](#) primary-side regulated (PSR) controller. One reason for using this controller is that it uses the auxiliary to secondary-side transformer turns ratio to sense the output voltage. This removes the need of an opto-isolator feedback in the design, which improves the reliability of the system, and reduces standby power. Removing the opto-isolator feedback network also reduces the design's List of Materials component count and total design cost. Also, the [UCC28722](#) is designed to drive bipolar junction transistors which are easier to find with high-voltage ratings and are less expensive than FETs for the same power rating, which makes it an ideal choice for eMeter applications. Refer to [Figure 3](#) for a functional schematic.

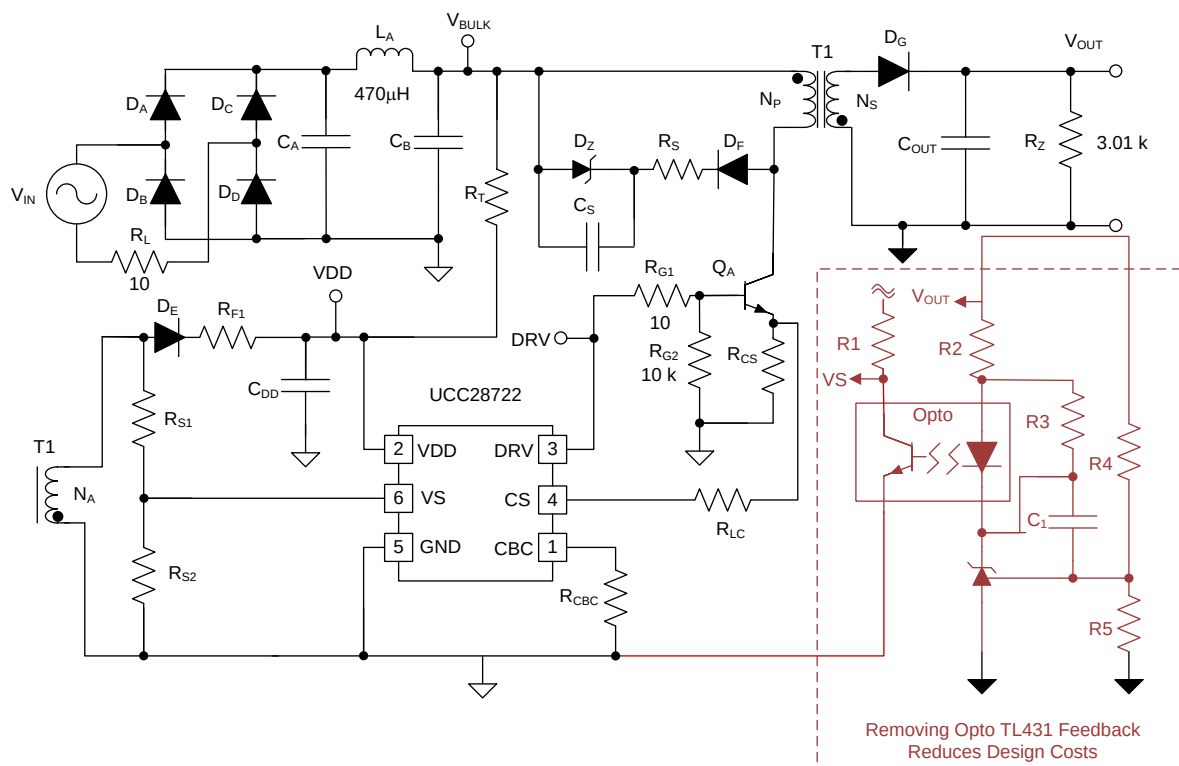


Figure 3. Offline Flyback Converter with [UCC28722](#) PSR Controller

The [UCC28722](#) is designed for discontinuous conduction mode Flyback converters. The power supply controller uses an FM/AM/FM modulation scheme to control duty cycle and improve overall efficiency; as well as reduce standby power. Please refer to [Figure 4](#) for the [UCC28722](#)'s internal control feedback block diagram.

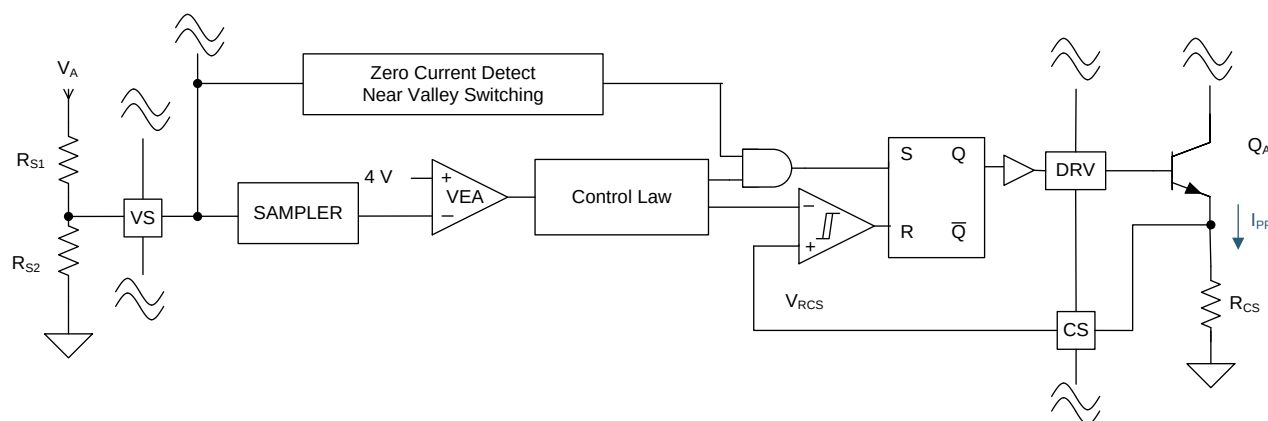


Figure 4. [UCC28722](#) Control Block Diagram

Figure 5 show the UCC28722 control law profile and shows the converter frequency (f_{SW}) and primary peak current (IPP) is modulated based on the UCC28722's error amplifier (E/A) output voltage. Please refer to the UCC28722's data sheet for more detailed information.

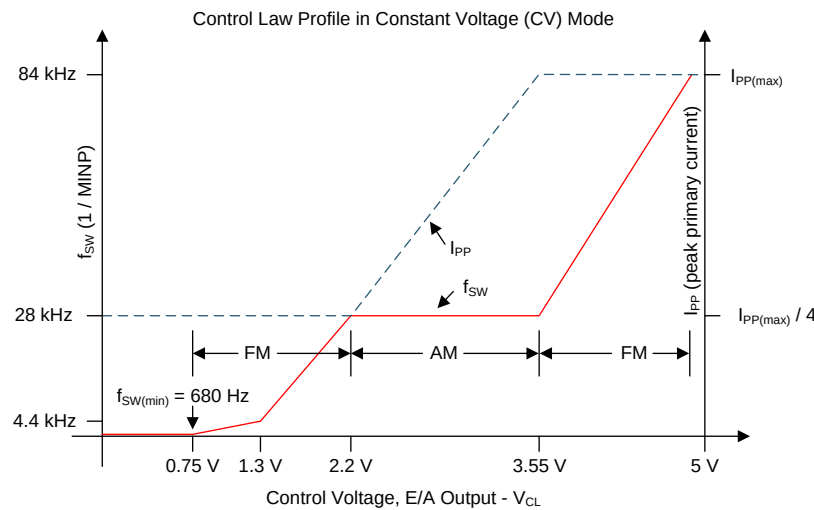


Figure 5. UCC28722 Control Law Profile

Previously it was mentioned that different eMeters have different input voltage ranges that vary from 48 V AC to 270 V AC, 85 V AC to 265 V AC, and 85 V AC to 480 V AC. These input ranges are extremely wide and it is not recommended to design one eMeter bias supply to meet every condition. For example designing for 48 V AC to 480 V AC input range is not feasible by using UCC28722. In this example the minimum input where the bias supply would have to operate is about 66% of the minimum peak input voltage, which is about 45 V. The maximum peak input voltage would be roughly 679 V. The bias supply would have to operate with an input range of 15:1, which PWM controllers cannot handle due to limitations in duty cycle. The UCC28722 can be designed for a wide input range 9.8:1 down to 4.9:1 but this range varies with the maximum switching frequency ($f_{SW(max)}$) chosen for the design, as well as with the switch-node resonant-ringing frequency (f_{LC}).

f_{LC} is determined by the magnetizing inductance (L_M) and the switch node capacitance (C_{SW}). For this evaluation we estimate the resonant frequency to be 500 kHz.

NOTE: Frequency varies based on power level, layout and semiconductors chosen, etc. for the design.

$$f_{LC} = \frac{1}{2 \times \pi \sqrt{L_M \times C_{SW}}} \approx 500 \text{ kHz} \quad (2)$$

The maximum duty cycle (D_{MAX}) of the converter happens at the minimum input voltage and full load condition. It is limited by the resonant frequency (f_{LC}), maximum allowable switching frequency ($f_{SW(max)}$) and allowing the flyback rectifier diode to conduct for at least 42.5% of the switching period during D_{MAX} .

NOTE: the UCC28722 control law limits the output rectifier conduction time to less than 42.5% of the switching period.

$$D_{MAX}(f_{SWMAX}) = 1 - 0.425 - \frac{f_{SWMAX}}{2 \times f_{LC}} \quad (3)$$

The primary magnetizing inductance (L_{PM}) of the transformer in Figure 3 sets the converter's maximum switching ($f_{SW(max)}$) and is selected based on estimated/actual systems efficiency (η), output power, the transformer primary peak current (I_{PPK}), and the converter's minimum input bulk voltage.

NOTE: Due to limitations imposed by EMI jitter and absolute maximum frequency ratings of the device it is recommended that the converter be designed for $f_{SW(max)}$ between 38 kHz and 72 kHz.

This is within the 28-kHz to 80-kHz range for the upper FM region in the control law presented in [Figure 5](#).

$$38 \text{ kHz} \leq f_{SWMAX} \leq 72 \text{ kHz} \quad (4)$$

$$I_{PPK} = \frac{2 \times P_{OUT}}{\eta \times D_{MAX} \times V_{BULK(MIN)}} \quad (5)$$

$$L_M = \frac{\frac{2 \times P_{OUT}}{\eta}}{(I_{PPK})^2 \times f_{SWMAX}} \quad (6)$$

NOTE: For the controller to operate correctly over the entire load range at maximum input voltage, the minimum duty cycle at maximum load and maximum switching frequency ($D_{MIN@f_{SW(max)}}(f_{SW(max)})$) needs to be 4 times greater than the UCC28722 current sense leading edge blanking timer (T_{CSLEB}) times the maximum switching frequency.

This ensures the converter operates in the AM range allowing the peak primary current (I_{PPK}) to be modulated from its maximum value down to its minimum value of $I_{PPK}/4$. This in turn limits the input voltage range ($\text{Range}(f_{SW(max)})$) the converter can be designed for.

$$T_{CSLEB} = 355 \text{ ns} \quad (7)$$

$$D_{MIN@f_{swmax}}(f_{SWMAX}) = 4.05 \times T_{CSLEB} \times f_{SWMAX} \quad (8)$$

In this equation $D_{MIN@f_{SW(max)}}(f_{SW(max)})$ is the primary-side switch duty cycle at maximum input voltage and full-load condition.

In the following equation, $V_{BULK(max)}$ is the maximum input voltage and $V_{BULK(min)}$ is the minimum input voltage to the eMeter bias supply.

$$\text{Range}(f_{SWMAX}) = \frac{V_{BULK(MAX)}}{V_{BULK(MIN)}} = \frac{D_{MAX}(f_{SWMAX})}{D_{MIN@f_{swmax}}(f_{SWMAX})} \quad (9)$$

With the equation for $\text{Range}(f_{SW(max)})$, the input range was plotted versus frequency in [Figure 6](#).

NOTE: This is based on an estimated f_{LC} and varies with actual magnetizing inductance and switch node capacitance.

From [Figure 6](#) it can be observed that, for the $f_{SW(max)}$ chosen for the design, the maximum input voltage range can vary from 9.8:1 down to 4.8:1.

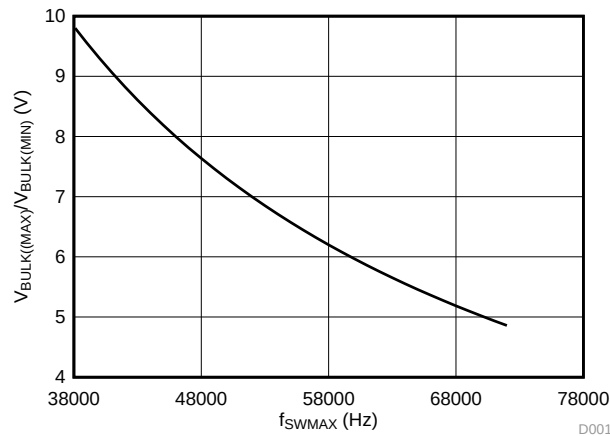


Figure 6. Input Range vs. Frequency

An eMeter bias supply using the UCC28722 flyback PSR controller will be evaluated to determine if it can be used for an aggressive input voltage range (V_{IN}) of 85 V_{RMS} to 480 V_{RMS}. For this design, the minimum bulk voltage ($V_{BULK(MIN)}$) is limited to 72 V and the maximum input voltage ($V_{BULK(MAX)}$) is the peak of highline operation which is roughly 679 V. This requires an input range of roughly 9.4 to 1.

$$Range = \frac{V_{BULK(MAX)}}{V_{BULK(MIN)}} = \frac{679V}{72V} = 9.4 \quad (10)$$

By evaluating the graph in Figure 6 and the equation for Range($f_{SW(max)}$) it can be observed that a 9.4:1 input range is obtainable at a switching frequency of 39.5 kHz.

NOTE: The allowable input range will not just vary based on $f_{SW(max)}$, it also varies based on C_{SW} and L_M .

For this reason it is a good idea to leave some margin and not design for the maximum input range that is possible (9.8:1).

$$Range(39.5kHz) = \frac{V_{IN(MAX)}}{V_{BULK(MIN)}} = \frac{D_{MAX}(39.5kHz)}{4.05 \times T_{CSLEB} \times 39.5kHz} = 9.4 \quad (11)$$

Once the maximum frequency is determined, the primary magnetizing inductance (L_M) of the transformer in Figure 3 can be calculated, based on an estimated efficiency of the design. For these high input voltage range eMeter designs, I have observed the efficiency at the peak of line to be roughly 70%. For this design we selected the maximum switching frequency to be 39 kHz and estimated the efficiency to be 70%, which gave us an L_M of roughly 2.7 mH. For a 5-W, 15-V design:

$$I_{PPK} = \frac{2 \times P_{OUT}}{\eta \times D_{MAX}(39kHz) \times V_{BULK(MIN)}} = \frac{2 \times 5W}{0.7 \times 0.54 \times 0.72} \approx 0.36A \quad (12)$$

$$L_M = \frac{\frac{2 \times P_{OUT}}{\eta}}{(I_{PPK})^2 \times f_{SWMAX}} = \frac{\frac{2 \times 5W}{0.7}}{(0.367A)^2 \times 39kHz} \approx 2.7mH \quad (13)$$

The transformer primary-to-secondary turns (N_{PS}) is calculated based on volt-second balance.

NOTE: In the equation for N_{PS} , variable $V_{QA(sat)}$ is the bipolar transistor saturation and V_{RCS} is the peak voltage drop across the current sense resistor.

V_{DG} is the voltage drop across the output rectifier diode (D_G) of the flyback converter in Figure 3.

$$N_{PS} \leq \frac{N_P}{N_S} = \frac{D_{MAX} (f_{SWMAX}) \times (V_{BULK(MIN)} - V_{QA(SAT)} - V_{RCS})}{0.425 \times (V_{OUT} + V_{DG})} \quad (14)$$

$$N_{PS} \leq \frac{N_P}{N_S} = \frac{D_{MAX} (39kHz) \times (72V - 0.6V - 0.75V)}{0.425 \times (15V + 0.6V)} = 5.7$$

where

- $N_{PS} = 5$, turns ratio was rounded down to a whole number. (15)

The primary-to-auxiliary turns ratio (N_{PA}) can be calculated based on the minimum input bulk voltage and the [UCC28722](#) UVLO turn on voltage ($V_{DD(on)}$).

NOTE: This turns ratio is set higher to combat magnetic tampering by means of VDD over voltage shutdown protection, as discussed later in the application note.

$$N_{PA} = \frac{N_P}{N_A} = \frac{V_{BULK(MIN)}}{V_{DD(on)}} = \frac{72V}{21V} \approx 3.6 \quad (16)$$

For this design example we set N_{PA} to 3.5.

$$N_{PA} = \frac{N_P}{N_A} = 3.5 \quad (17)$$

The output capacitor is selected based on holdup requirement.

$$C_{OUT} \geq \frac{2ms \times \frac{P_{OUT}}{V_{OUT}}}{V_{OUT} - V_{OUT} \times 0.8} = \frac{2ms \times \frac{5W}{15V}}{15V - 15V \times 0.8} = 222\mu F$$

where

- $C_{OUT} = 270 \mu F$, standard output capacitance was chosen for the design. (18)

There is one social issue with eMeter usage and that is with magnetic tampering to interfere with metering. If a strong magnet is applied near the flyback transformer it saturates the transformer causing sampling errors in the output voltage sensing. This causes the [UCC28722](#) controller to demand more duty cycle than it should, which causes the output voltage to increase because of the incorrect output voltage sampling and most likely would damage the eMeter bias supply. The inexpensive, simple circuitry presented in [Figure 7](#) can be used to disable the [UCC28722](#) BJT driver output if such an event should occur.

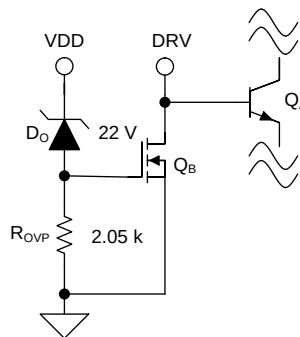


Figure 7. VDD Over Voltage Protection (OVP)

The VDD voltage tracks the output voltage through the auxiliary-to-secondary transformer turns ratio (N_{AS}). The circuitry in [Figure 7](#) is just a V_{DD}/V_{OUT} over-voltage protection circuit. The V_{DD} over voltage threshold $V_{DD}(OVP)$ will be FET QB's gate-to-source threshold ($V_{GS(th)}$) plus diode DO's zener voltage. In this example, if a logic level FET of with a $V_{GS(th)}$ of 2 V was used with a VDO of 22 V, FET QB will turn on, stealing the base drive current from Q_A , preventing the PSR flyback converter from switching. This also triggers a current sense short circuit fault, which disables driver switching and discharges the VDD capacitor to the UVLO turn-off voltage and initiates a restart after the VDD capacitor has been charged up with a trickle charge resistor to the UVLO turn on voltage.

$$V_{VDD(OVP)} = V_{gs(th)} + V_{DO} \approx 2V + 22V \approx 24V \quad (19)$$

NOTE: The VDD(OVP) threshold varies with changes in $V_{GS(th)}$ and variations in zener diode voltages. In this example, the VDD over voltage trip point would be between 23 V and 25 V.

$$V_{VDD(OVP)} = 23V \text{ to } 25V \quad (20)$$

The [UCC28722](#) BJT driver (DRV) is current limited ($I_{DRS(max)}$) to 42 mA. To ensure that the BJT does not start switching in case of an over voltage event, it is recommended to select a FET for QB with resistance ($R_{DS(on)}$) that is low enough to prevent BJT Q_A from turning on.

$$R_{ds(on)} \leq \frac{0.3V}{I_{DRS(max)}} = \frac{0.3V}{42mA} \approx 7\Omega \quad (21)$$

NOTE: The information in this application note reviews special considerations and techniques for designing the [UCC28722](#) into an eMeter bias supply.

This includes tips for designing for large input voltage ranges, as well as magnetic tampering protection circuitry. However, this is supplemental information and should be used in conjunction with the [UCC28722/UCC28720 5-W design example/application note \(SLUA700\)](#) to complete the eMeter bias supply design.

2 Reference Material

1. [UCC28722 Data Sheet](http://www.ti.com/lit/gpn/ucc28722), <http://www.ti.com/lit/gpn/ucc28722>
2. [UCC28722/UCC28720 5W Design Example](http://www.ti.com/lit/pdf/sluc700), <http://www.ti.com/lit/pdf/sluc700>
3. [UCC28722 MathCAD Flyback Design Tool](http://www.ti.com/lit/zip/sluc528), <http://www.ti.com/lit/zip/sluc528>
4. [UCC28722 Excel Design Tool](http://www.ti.com/lit/zip/sluc529), <http://www.ti.com/lit/zip/sluc529>
5. [Universal AC Input 7.5W Adapter \(flyback\), TI Reference Design](http://www.ti.com/tool/PMP4391), <http://www.ti.com/tool/PMP4391>
6. [Wide Input 2W Bias Power Supply \(Buck\), TI Reference Design](http://www.ti.com/tool/PMP7668), <http://www.ti.com/tool/PMP7668>

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