EVM User's Guide: DAC39RF12EVM

DAC39RF12EVM Evaluation Module

Description

The DAC39RF12EVM is an evaluation board for evaluating the DAC39RF10/DAC39RF12 family of digital-to-analog converters (DAC) from Texas Instruments. The DAC39RF10/DAC39RF12 is a family of single and dual channel DACs with 16-bit resolution. The devices can be used in non-interpolation modes (real) as well as interpolation modes (complex IQ). The maximum input rate is 24GSPS in a dual edge sampling mode with 8 bits of DAC resolution. 12GSPS real data is also supported with a single channel DAC. This evaluation board also includes the following features.

Features

- Two balun-coupled output networks per DAC output allowing singled ended signal evaluation.
- A 3MHz to 6GHz low band balun for 1st Nyquist evaluation.
- A 1.8GHz to 18GHz high band balun for 2nd/3rd Nyquist evaluation.
- A LMK04828 clock distribution chip for distributing FPGA reference clocks as well as SYSREF for subclass 1 operation.
- A balun-coupled clock input network to test the DAC performance with an external low-noise clock source.
- An FMC+ with High-speed serial data connections for full JESD204C testing of all 16 lanes.
- A USB to serial chip to allow programming of the DAC/LMK with a simple USB connection.
- The ability to program the DAC/LMK from an FPGA using the FMC+ connector.[1]
- Device register programming through USB connector and FTDI USB-to-SPI bus translator with option to program from FGPA using SPI through FMC+ connector

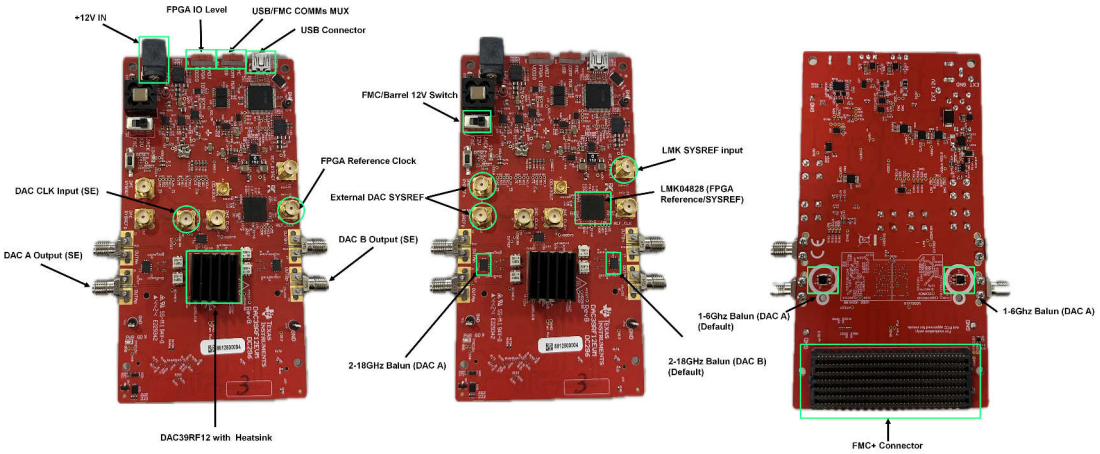


Figure 1-1. DAC39RF12EVM Key Components

The DAC39RF12EVM is paired with the TSW14J59EVM data capture and pattern generator card.[2]

[1] To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in Section 2.3).

[2] If the DAC39RF12EVM is only used in DDS mode, then data capture EVM is not required.

1 Evaluation Module Overview

1.1 Introduction

The following user guide gives an in depth overview on using the DAC39RF12EVM evaluation board hardware as well as the software GUIs that are associated with the EVM to change, configure and evaluate the DAC in the various modes and features.

1.2 Kit Contents (Required Equipment)

The following equipment and documents are included in the DAC39RF12EVM kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable

The following equipments are **not** included in the DAC39RF12EVM kit, but are required for evaluation of this product:

- TSW14J59EVM data capture board and related items
- PC computer running Microsoft® Windows® 10 or higher
- Low phase-noise signal generator for DEVCLK (Sampling clock).
- Additional signal generator for FPGA reference clock generation.
  - Both signal generators need to be 10MHz reference locked.
- Two low noise power supplies: 12V/5V (TSW14J59EVM) and 12V/3A (DAC39RF12EVM)
- Three SMA type low loss cables

2 Hardware

2.1 Setup Procedure

This section describes how to setup the DAC and TSW14J59 EVMs on the bench with the proper equipment to evaluate the performance of the DAC device.

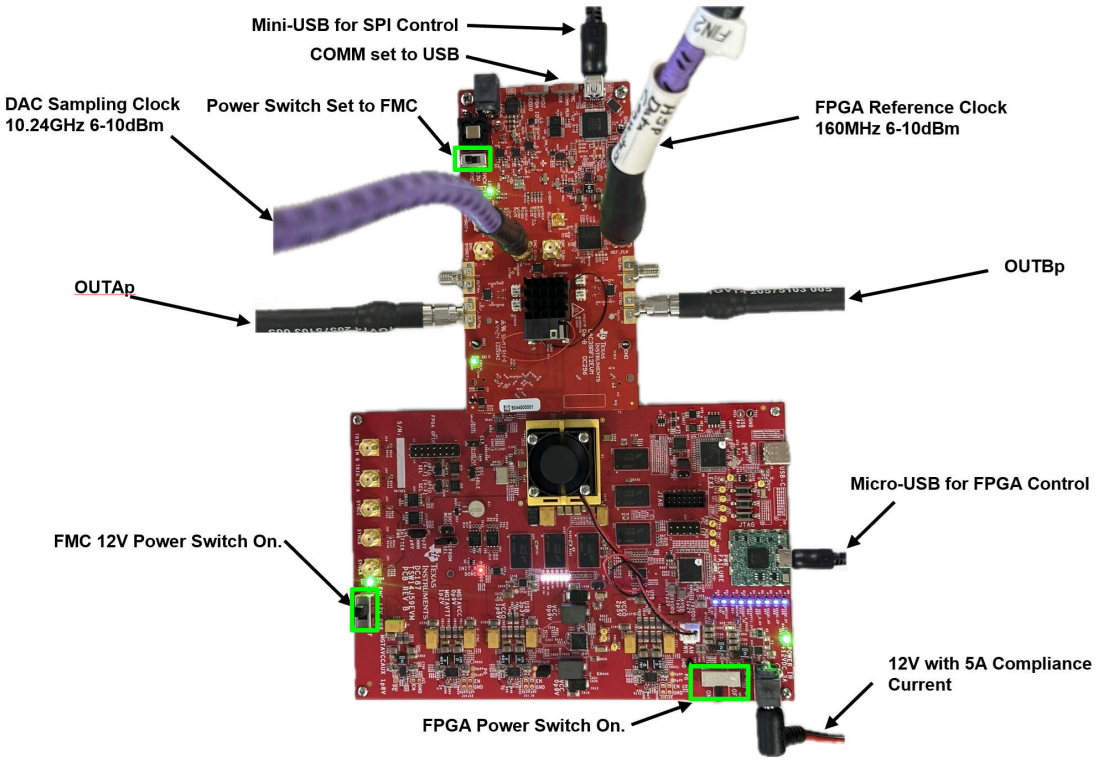


Figure 2-1. DAC39RF12EVM Test Setup

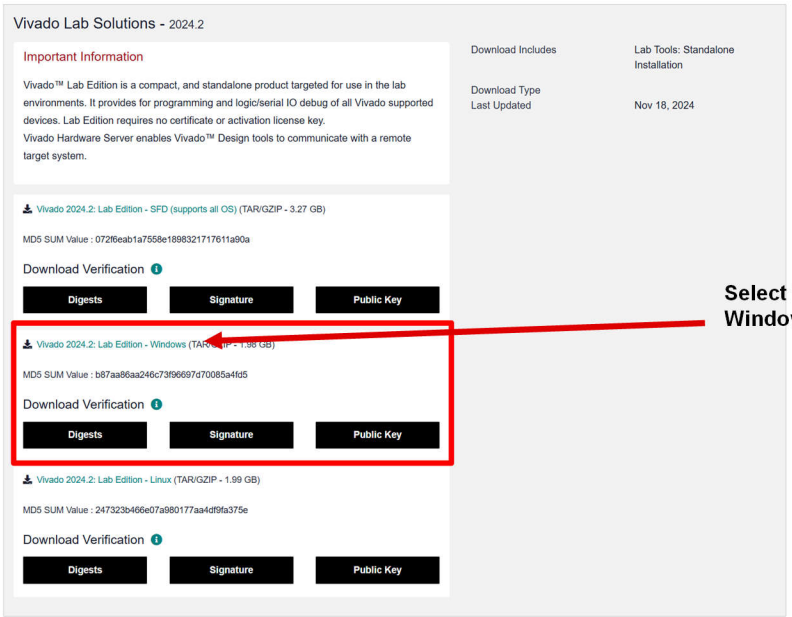
2.1.1 Installing the DAC39RF12EVM Configuration GUI Software

1. Download the DAC39RF12EVM Configuration GUI software from the EVM tool folder at DAC39RF12EVM GUI.
   a. NOTE: The GUI download includes the following:
      i. DAC39RF12 EVM GUI
      ii. J59 Commander
         1. DAC WaveGen
      iii. J59 Server
2. Run the executable file (DAC39RF12EVM_SW_Package_v3.1.2.exe).
3. Install Vivado Lab Tools: https://www.xilinx.com/support/download.html
   a. Follow the next section for instructions on how to install the Xilinx tools and add environment variables path to the desktop PC.

2.1.1.1 Installing & Setting Up Vivado Lab Tools

For the DAC39RF12EVM, Vivado Lab Tools will need to be installed. Please follow the steps outlined in this section.

1. Create a User account for AMD and sign in.
   a. Fill out the appropriate information before downloading.
   b. When complete, press the download button.
2. The download file type will be a .tar file. In Windows you can open the .tar file and explore it.
3. Next, look inside the Vivado_Lab_Win_2024.2_1113_1001 folder for <xsetup.exe>
   a. Right click and execute it, windows will ask you to “Extract All”.
4. Once the files are extracted, open the folder and find “xsetup.exe”.
   a. Right click on this file and install it. Windows may ask for permissions.
5. Follow the sequence of steps in the figures outlined below in order to finis the Xilinx Lab Tools installation.



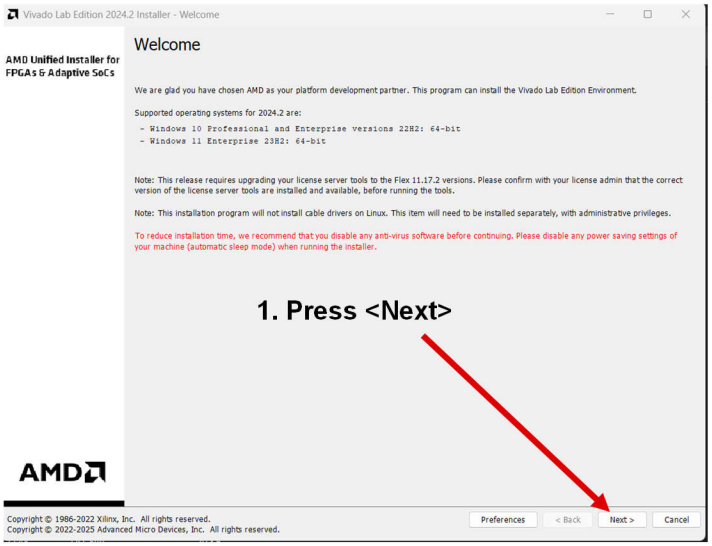
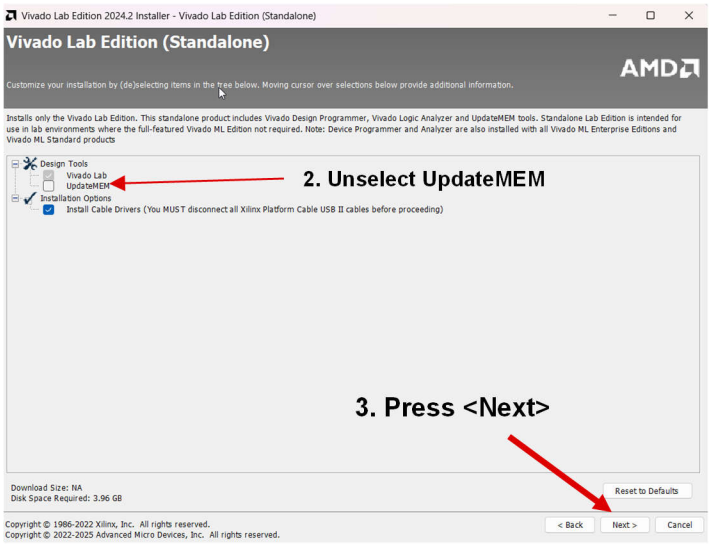
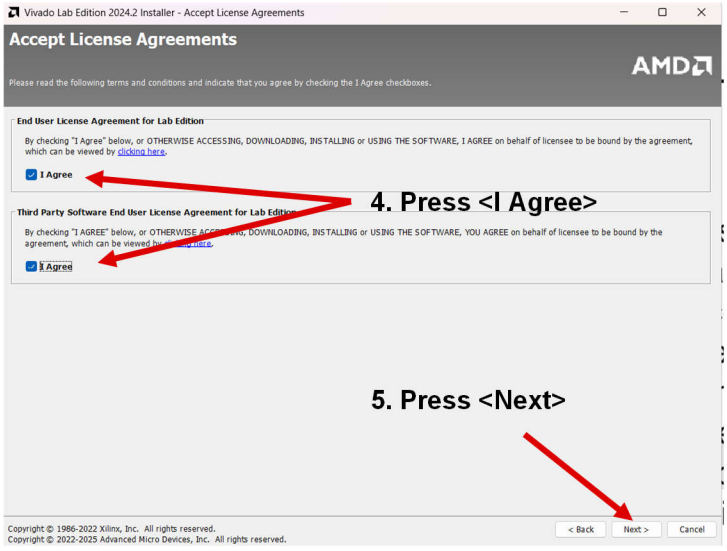
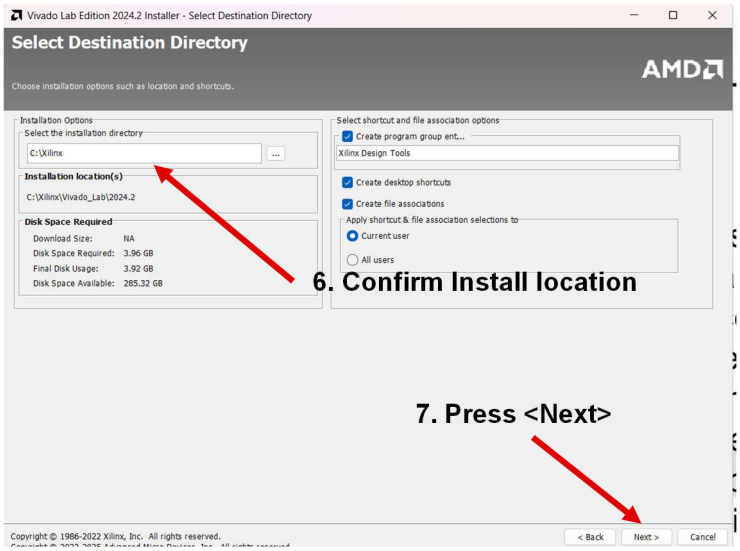
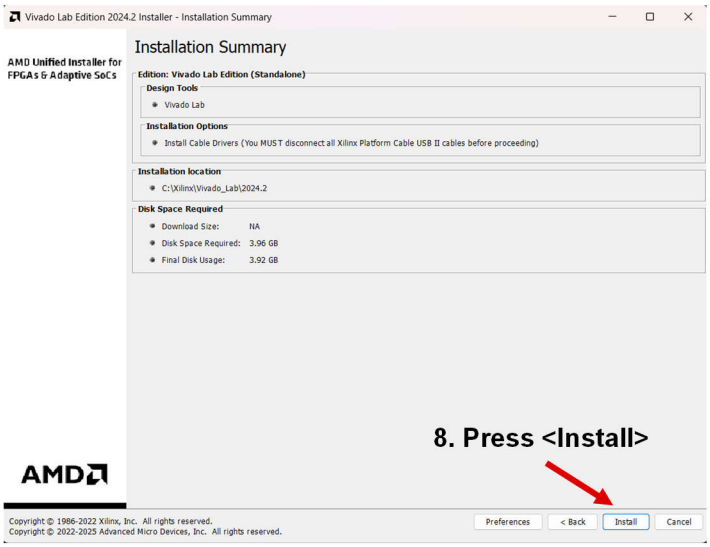


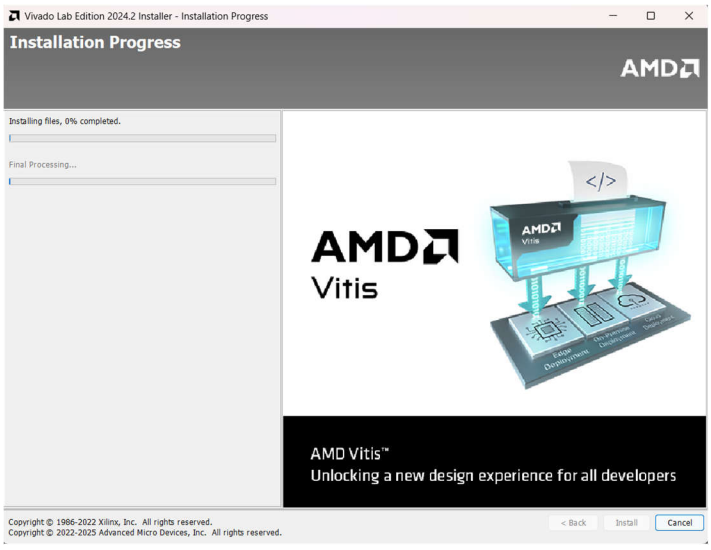
Figure 2-2. Installing Vivado Lab Tools

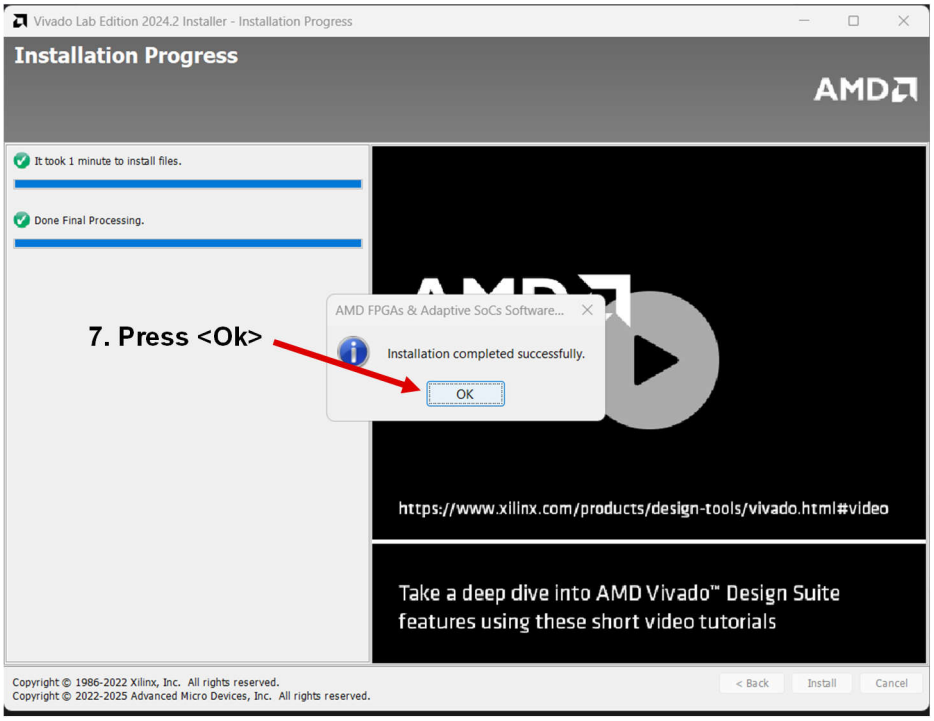












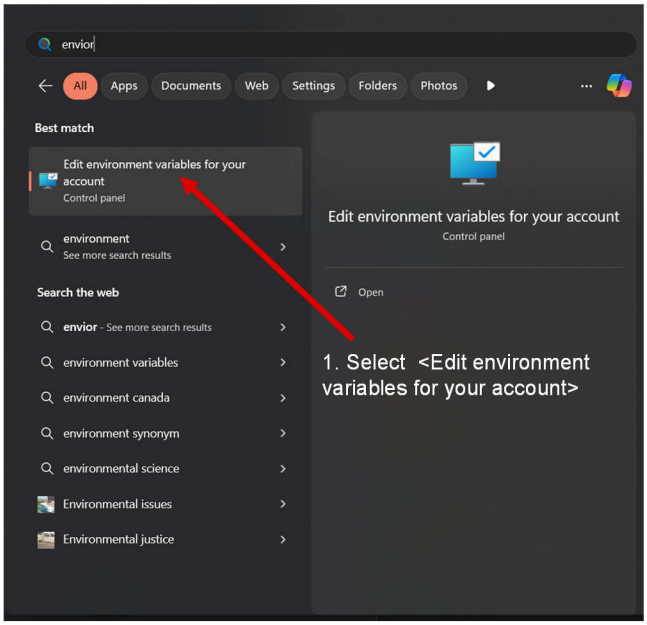
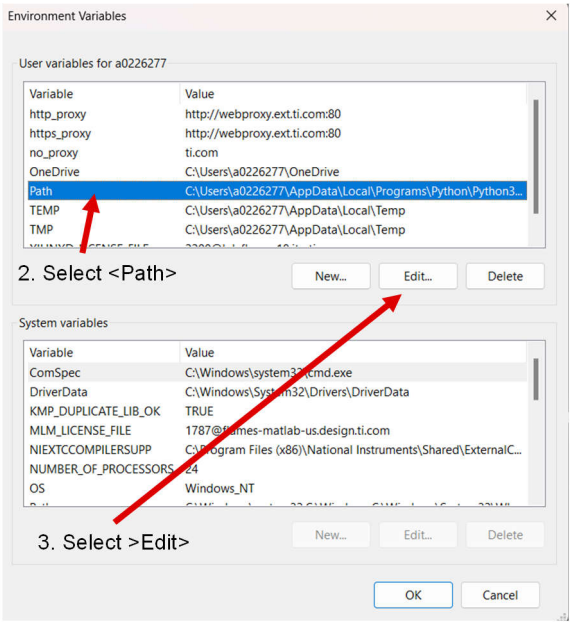
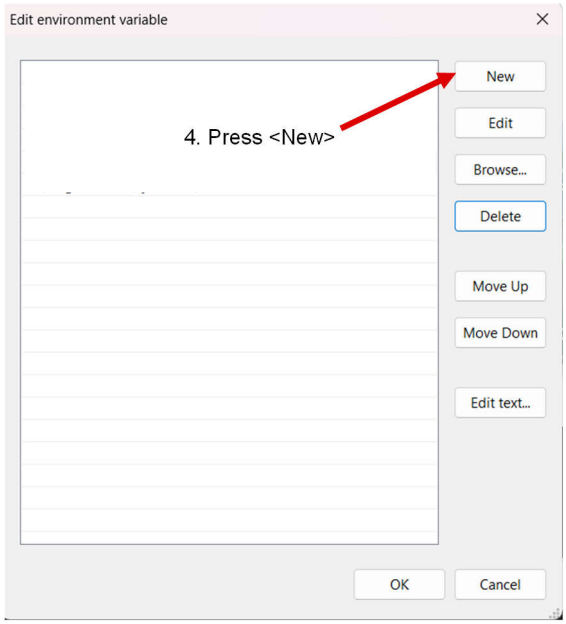
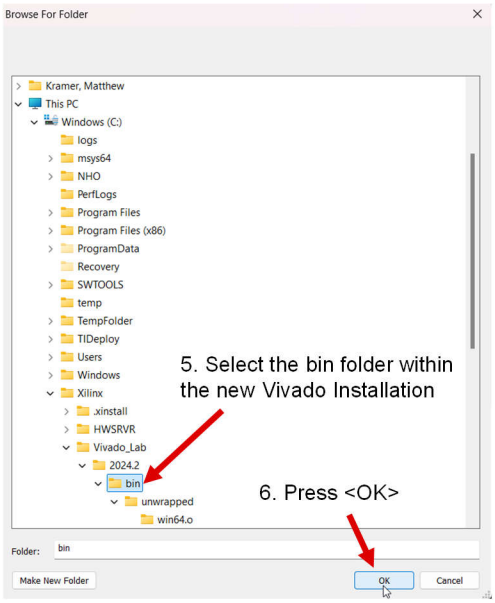
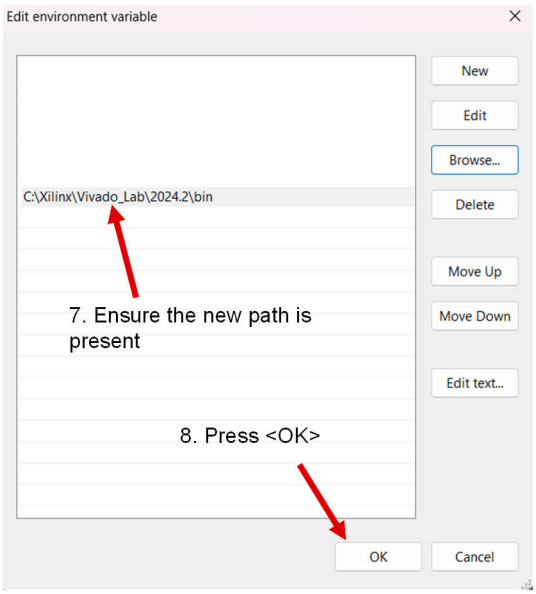


Figure 2-3. Adding Vivado Lab Tools to the Windows PATH









Once this is complete, the J59_Server can be run.

2.1.2 Connect the DAC39RF12EVM and TSW14J59EVM

1. With the power off, connect the DAC39RF12EVM to the TSW14J59EVM through the FMC+ connector as shown in DAC39RF12EVM Test Setup.

2.1.3 Connect the Power Supplies to the Boards (Power Off)

1. Confirm the power switch on the TSW14J59EVM is in off position. Connect the power cable to a 12V DC (minimum 5A) power supply. Make sure the proper supply polarity by confirming the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the TSW14J59EVM power connector.
2. DAC39RF12EVM can be powered with 12V DC (minimum 3A) though the connector jack(J5) on the DAC39RF12EVM, or the EVM can be powered from the TSW14J59EVM via FMC+ connector. There is a switch (SW1) which can be used to select power from the barrel jack on the DAC EVM, or from TSW14J59EVM through FMC+ connector. Confirm that the power switch for the DAC39RF12EVM power supply is set to the opposite position (Jack) from which it should be drawing power. If using barrel jack option, connect the power cable to a 12V DC (minimum 3A) power supply. Make sure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the EVM power connector. Table 2-1 is used as a reference to power the DAC EVM.

Table 2-1. Powering the DAC39RF12EVM

DAC39RF12 Powered from	DAC39RF12 Power Switch position	TSW14J59EVM FMC switch position	Power supply needed
TSW14J59EVM via FMC+ connector	FMC	ON	12V 5A for TSW14J59EVM
External Supply with jack on DAC39RF12EVM	JACK	OFF	12V 3A for TSW14J59 and 12V 3A for DAC39RF12EVM

CAUTION

Make sure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage. Leave the power switches in the off position until directed later.

2.1.4 Connect the Spectrum Analyzer to the EVM

Connect a spectrum analyzer to the Aoutp (J1) SMA connector of the DAC39RF12EVM .

Note

1. The FPGA REF clock frequency can be obtained from the DAC39RF12EVM GUI once the DAC39RF12EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown in Figure 1-1.
2. Make sure that the DEVCLK and Reference clock sources are frequency-locked using a common 10MHz reference to for functionality.
3. Do not turn on the RF output of any signal generator at this time.
4. In all of these examples the FPGA REF clock = 160MHz, the DAC sampling clock = 10.24GHz.

2.1.5 Turn On the TSW14J59EVM Power and Connect to the PC

1. Turn on the power switch to the TSW14J59EVM.
2. Connect a Micro USB cable from the PC to the TSW14J59EVM.

2.1.6 Turn On the DAC39RF12EVM Power Supplies and Connect to the PC

1. The default option uses the power from FMC+ connector on TSW14J59EVM. For this option, the FMC power switch on the TSW14J59EVM must be set to the on position, and power switch on the DAC39RF12EVM must be set to FMC(default). If external power supply is used to power the DAC EVM. Then turn on the 12V power supply connected to the barrel jack on the DAC EVM and set the power switch position on DAC39RF12EVM to JACK position.
   The green Power Good LED(D5) on DAC EVM should turn on, indicating DAC EVM is getting power.
2. Connect the DAC EVM to the PC with the mini-USB cable to the EVM.

2.1.7 Turn On the Signal Generators

1. Turn on the output of the low phase noise RF signal generator and connect to DAC CLKp (J6) via the SMA cable. Set the signal generator to 10.24GHz at a +6dBm output level.
2. Turn on the output of the RF signal generator and connect to REF_CLK (J8) via the SMA cable.
3. Set the signal generator to 160MHz at a +6dBm output level. Using another SMA cable, connect it to OUTAp (J1), the output of the DAC to a spectrum analyzer.

Note

The max clock rate supported by DAC39RF12EVM is 12GHz

2.1.8 Launching the DAC39RF12EVM GUI and Programing the DAC EVM - JMODE 0

Configuration example of DAC39RF12EVM in JMODE 0

1. JMODE 0 is considered bypass mode or real data mode, interpolate x1.
   a. Configuration details:
      i. 10.24GSPS
      ii. 10.3125Gbps SERDES rate
      iii. 16 lanes
      iv. JESD_M = 1
      v. CHA & CHB outputs are equal

2. Simply follow the numerated steps in the subsequent figures, to launch the DAC GUI. Following the steps as shown to configure the EVM.

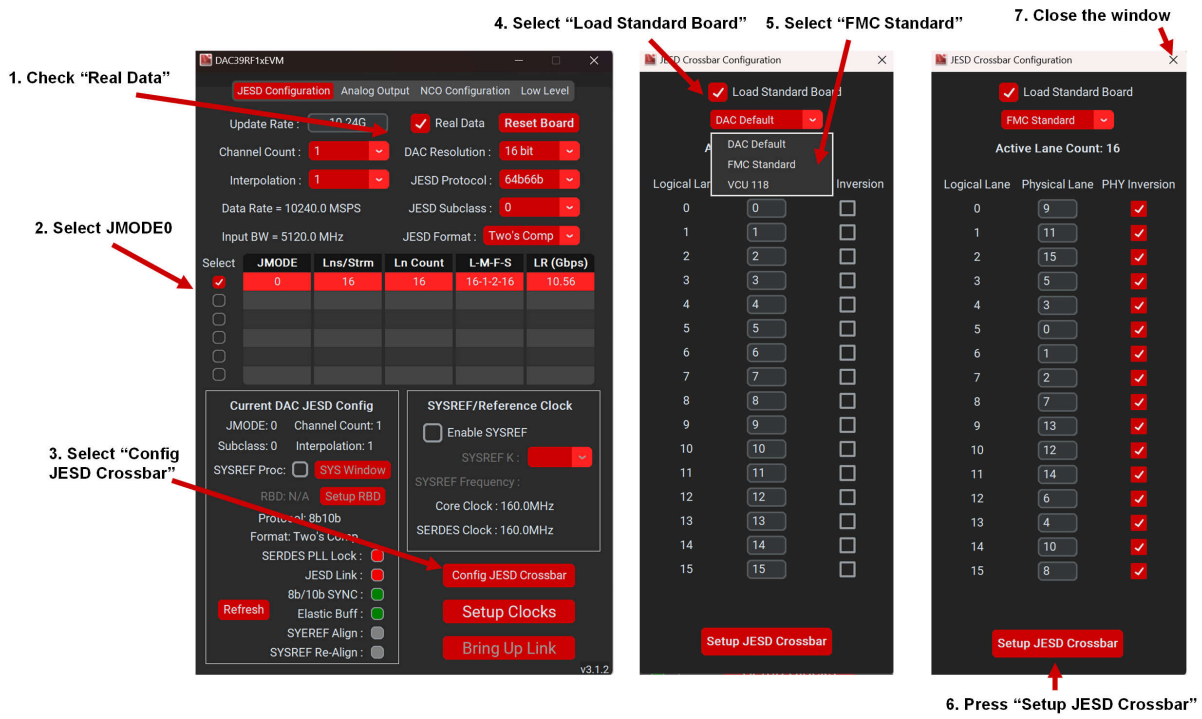


Figure 2-4. DAC39RF12EVM GUI Configuration, Part 1

1. Then launch/bring up the J59_Server.exe. As shown in the figure.
2. Next, launch/bring up J59_Commander. Set the interpolation to 1, then open the DAC Wavegen GUI.

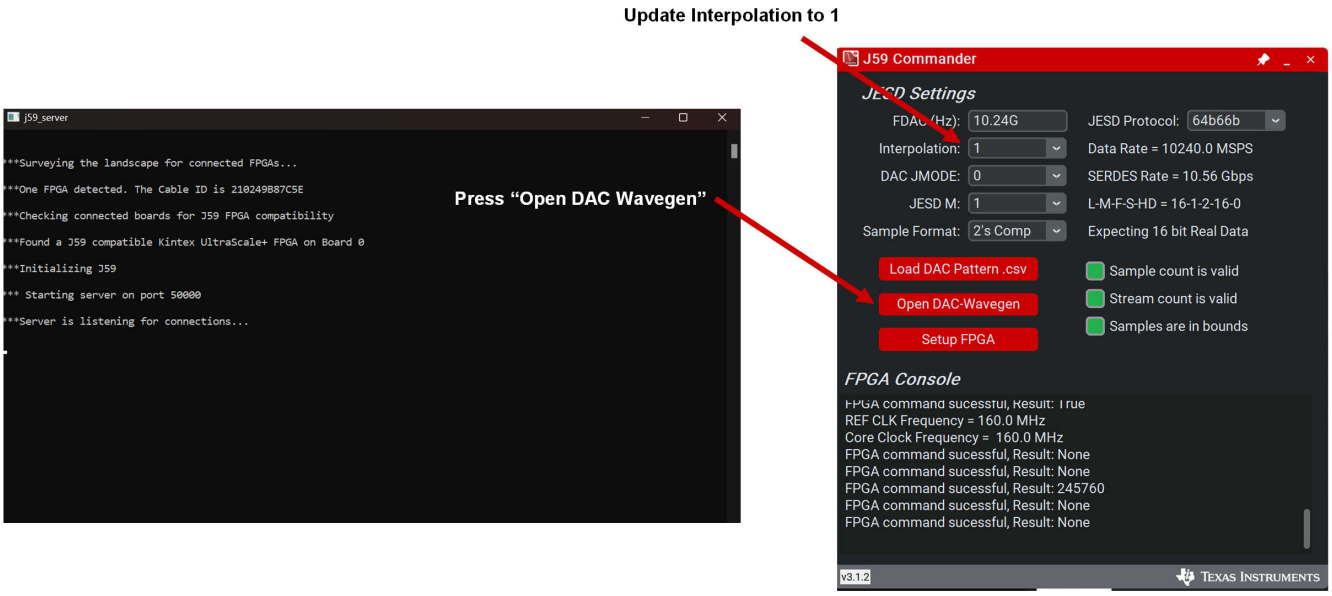


Figure 2-5. J59 Server.exe and J59 Commander, Step 2

1. In the DAC Wavegen GUI, setup the details as noted in figure Figure 2-6.

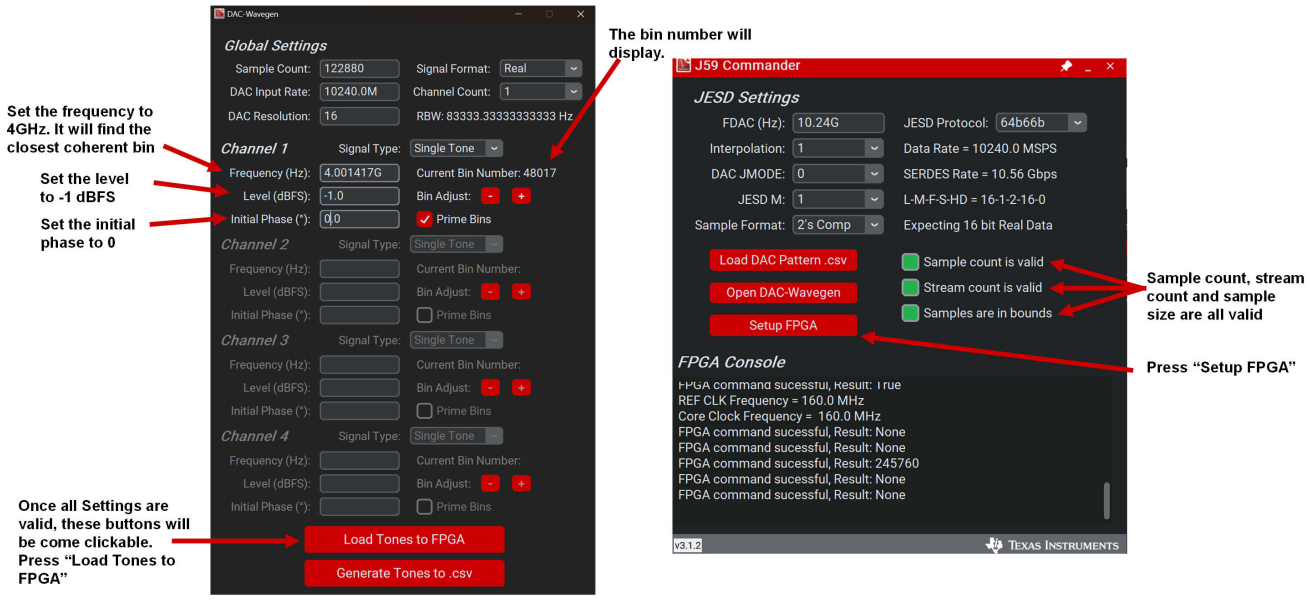


Figure 2-6. DAC Wavegen GUI & J59 Commander setup details, Step 3

2. Once the FPGA is setup, there should be the following output on the spectrum analyzer. Figure Figure 2-8.

Figure 2-7. DAC39RF12EVM GUI Configuration Steps, Step 4

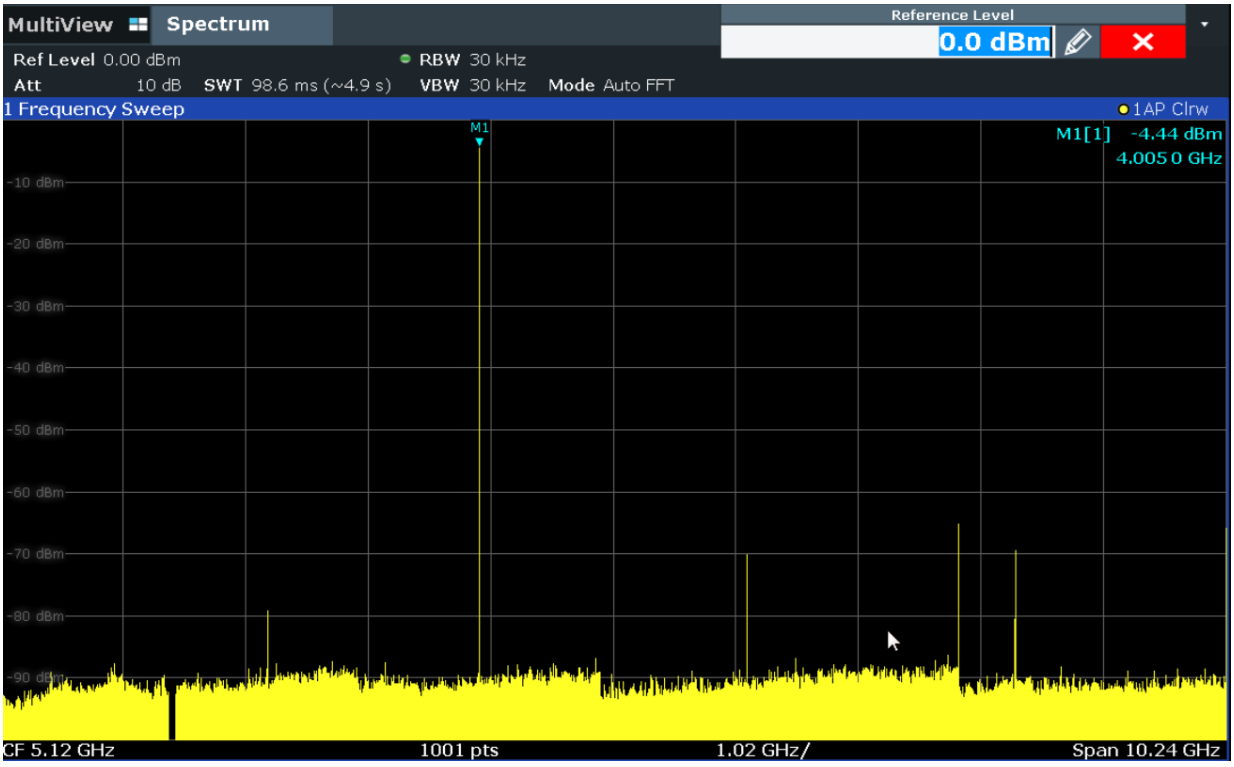


Figure 2-8. DAC39RF12EVM, CHA Output Spectrum in JMODE 0, DES2XL Mode

2.1.9 Launching the DAC39RF12EVM GUI and Programing the DAC EVM - JMODE 1

Configuration example of DAC39RF12EVM in JMODE 1

1. JMODE 1: complex data, interpolate x2.
   a. Configuration details:
      i. 10.24GSPS
      ii. 10.3125Gbps SERDES rate
      iii. 16 lanes
      iv. JESD_M = 2
      v. CHA & CHB outputs are equal

2. Simply follow the numerated steps in the subsequent figures, to launch the DAC GUI. Following the steps as shown to configure the EVM.

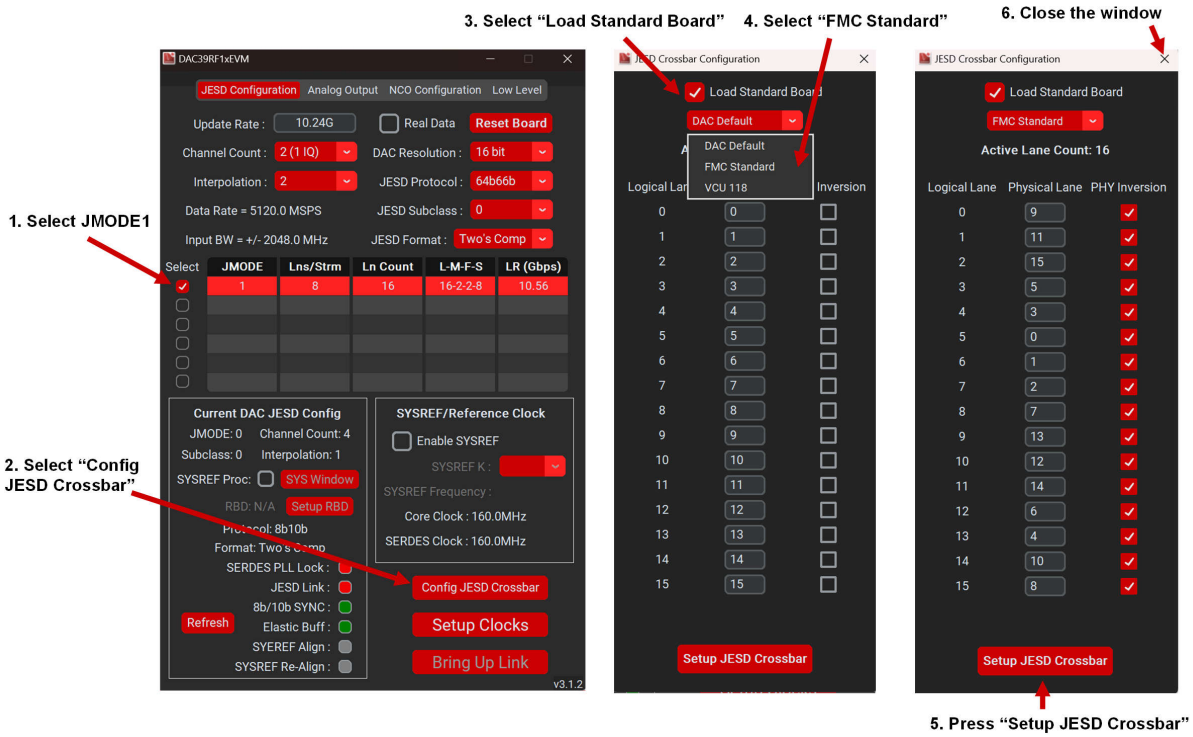


Figure 2-9. DAC39RF12EVM GUI Configuration, Step 1

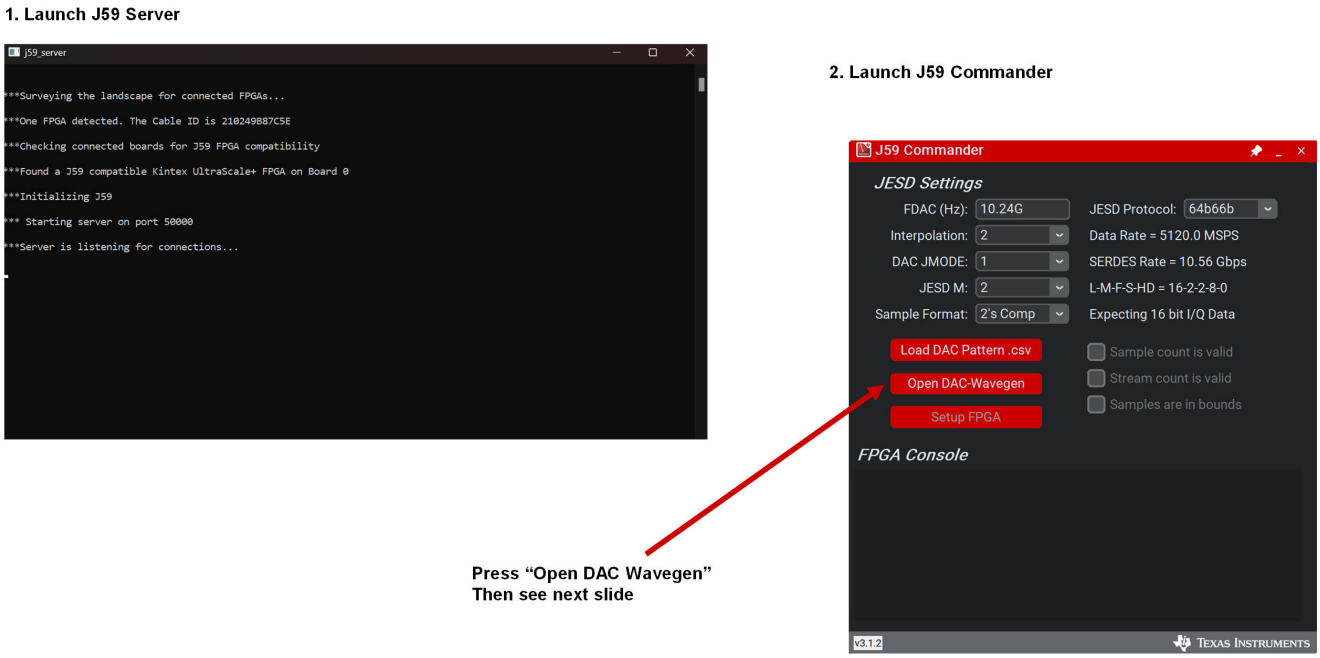


Figure 2-10. J59 Server.exe and J59 Commander Setup, Step 2

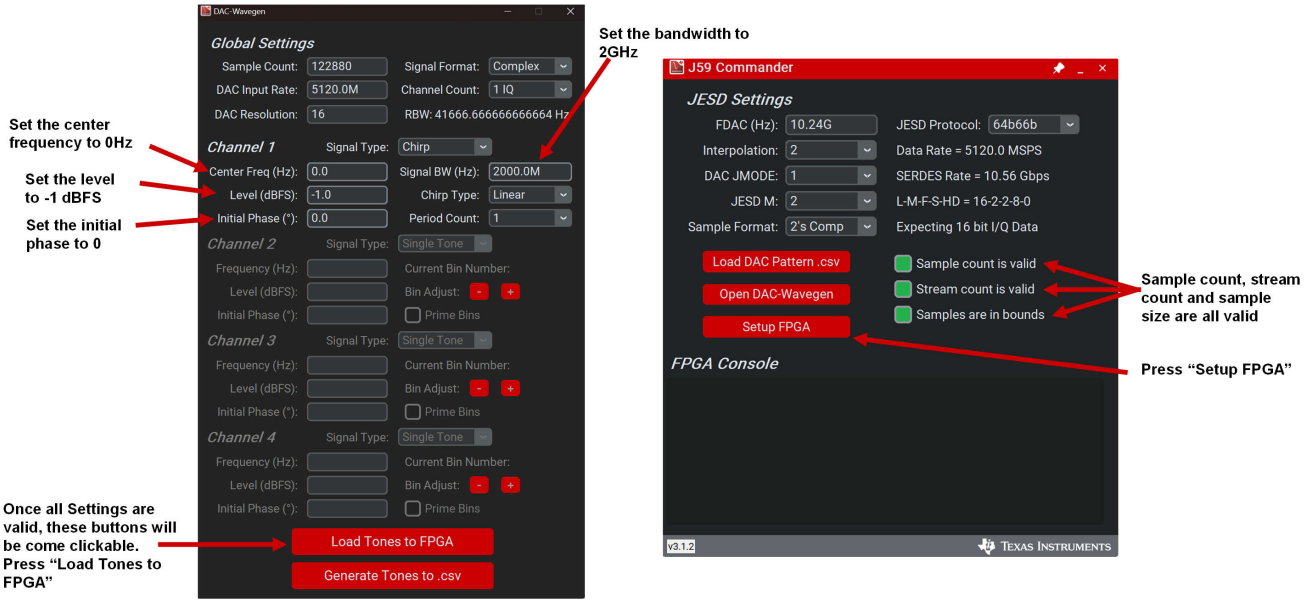


Figure 2-11. DAC Wavegen GUI & J59 Commander setup details, Step 3

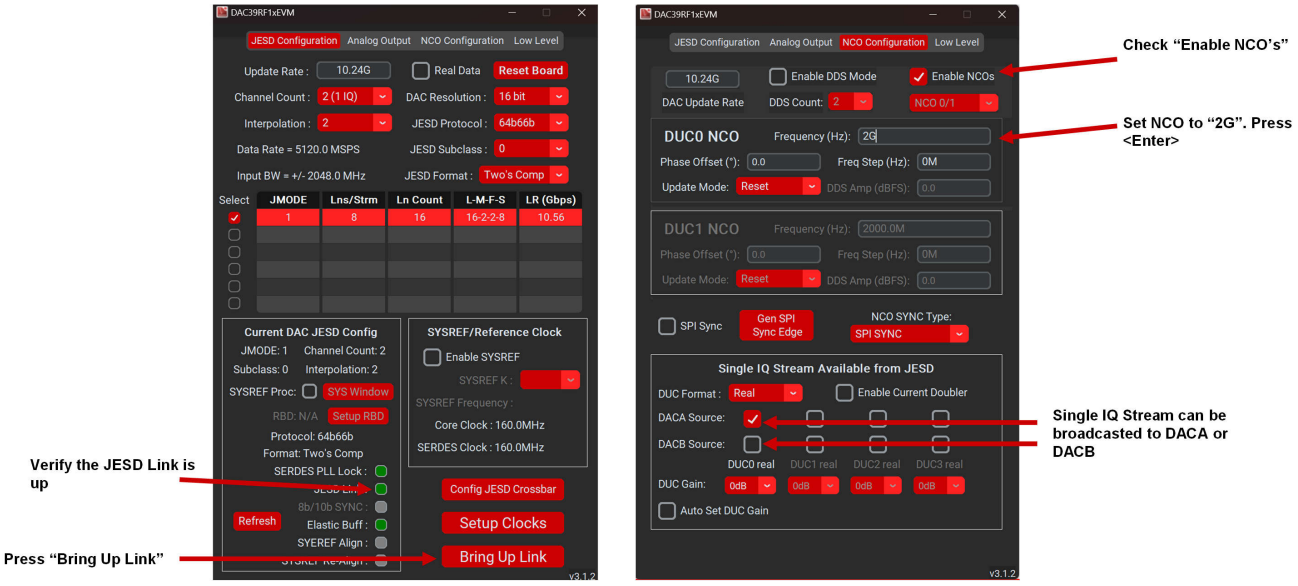


Figure 2-12. DAC39RF12EVM GUI Configuration Steps, Step 4: Moving the modulated waveform up in frequency.

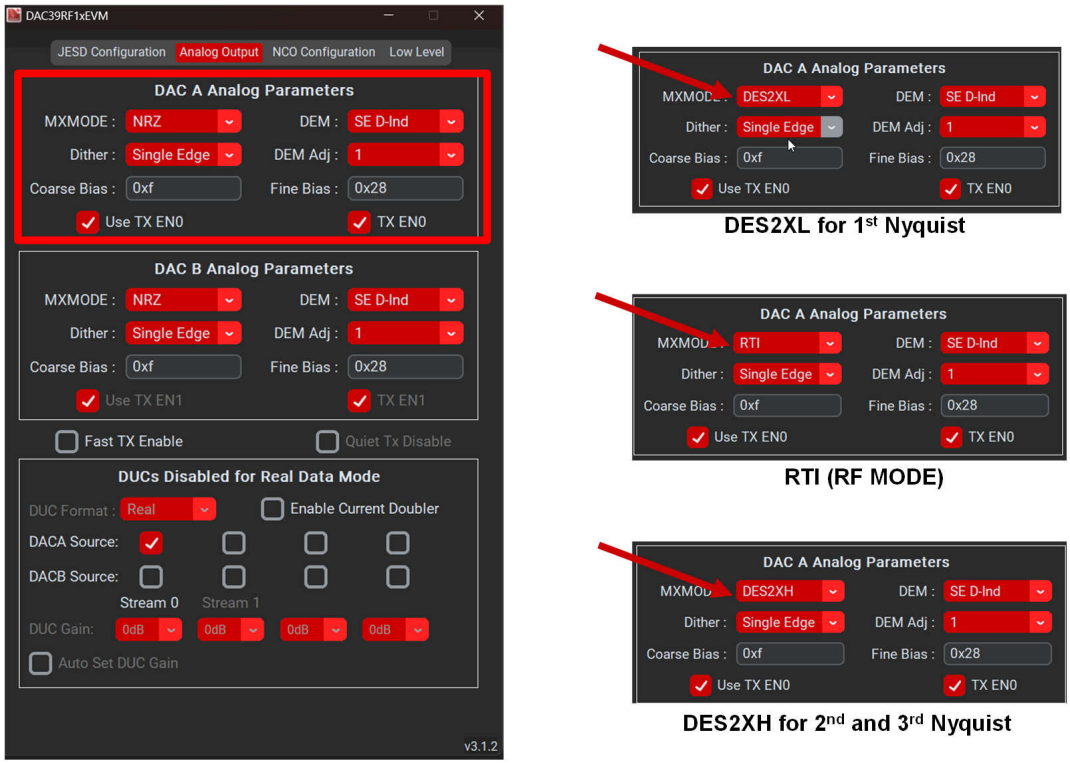


Figure 2-13. DAC39RF12EVM GUI Configuration Steps, Step 5

Note

The MXMODE of each DAC can be changed in real time. This can help with frequency planning.

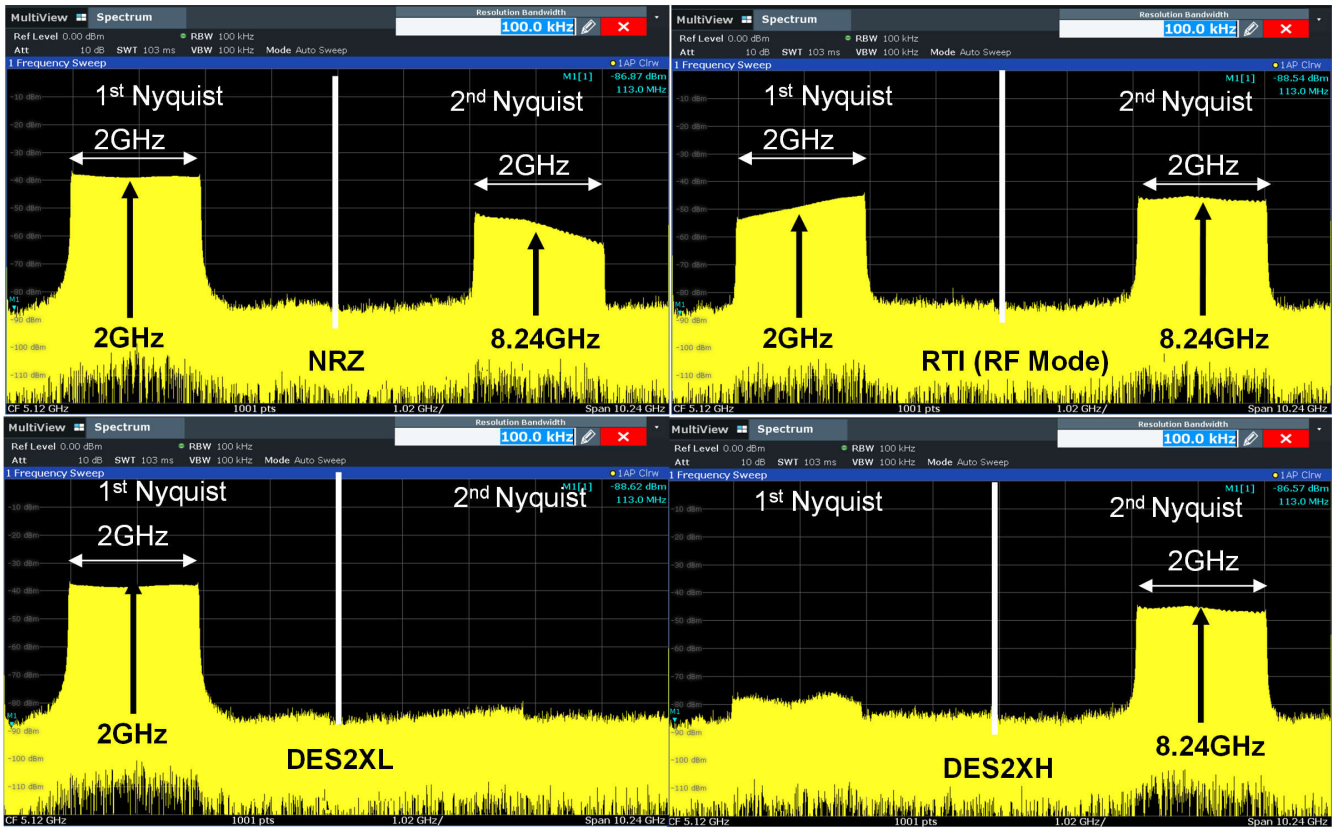


Figure 2-14. DAC39RF12EVM, CHA Output Spectrum in JMODE 1, showing the modulated waveform vs. The different output DAC modes.

2.1.10 Launching the DAC39RF12EVM GUI and Programing the DAC EVM - JMODE 3

Configuration example of DAC39RF12EVM in JMODE 3

1. JMODE 3 is considered complex data, 4 complex streams, interpolate x8.
   a. Configuration details:
      i. 10.24GSPS
      ii. 10.3125Gbps SERDES rate
      iii. 16 lanes
      iv. JESD_M = 8
      v. CHA & CHB outputs are equal

2. Simply follow the numerated steps in the subsequent figures, to launch the DAC GUI. Following the steps as shown to configure the EVM.

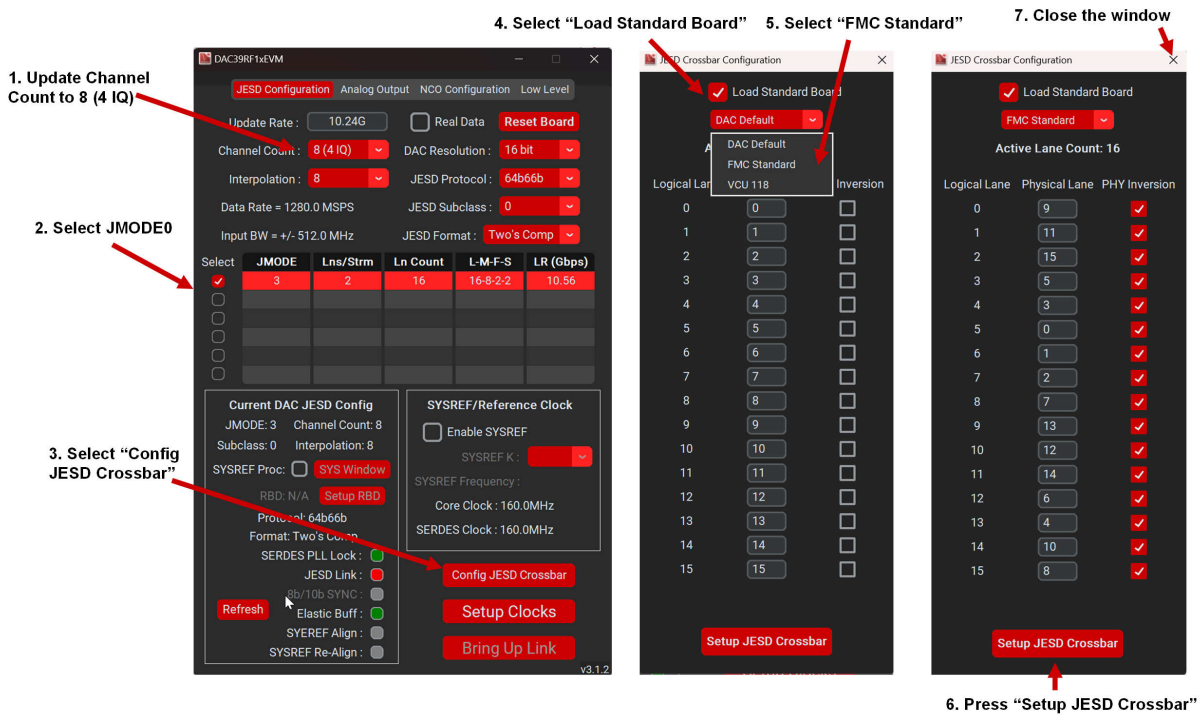


Figure 2-15. DAC39RF12EVM GUI Configuration, Step 1

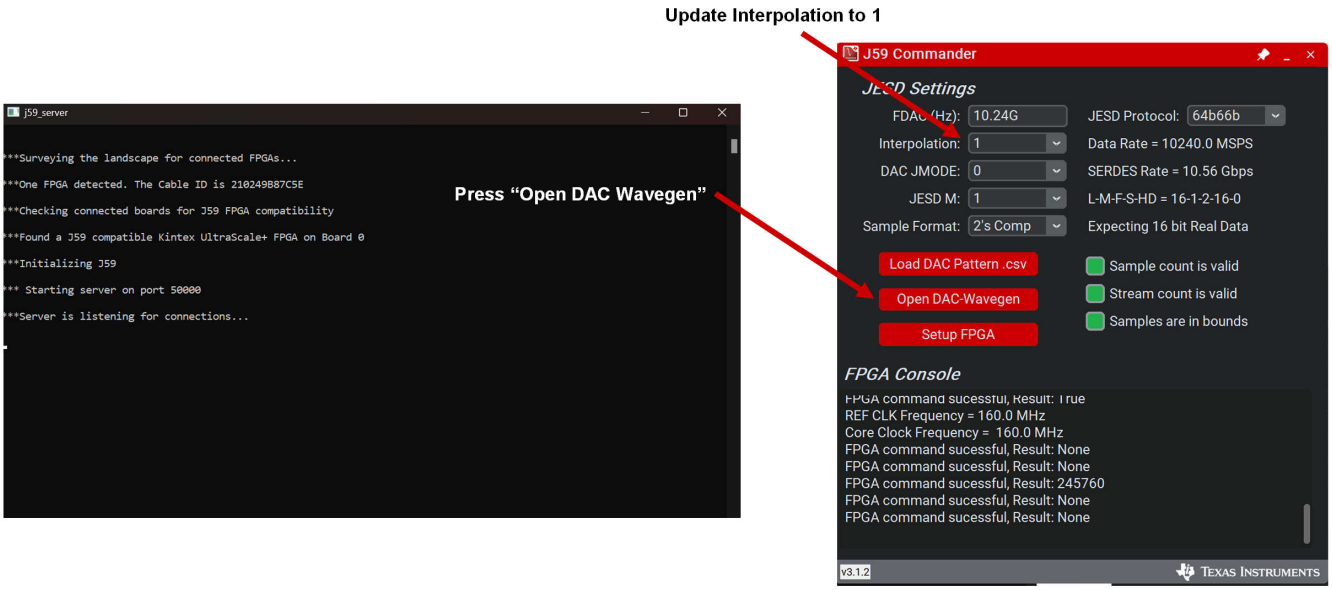


Figure 2-16. J59 Server.exe and J59 Commander Setup, Step 2

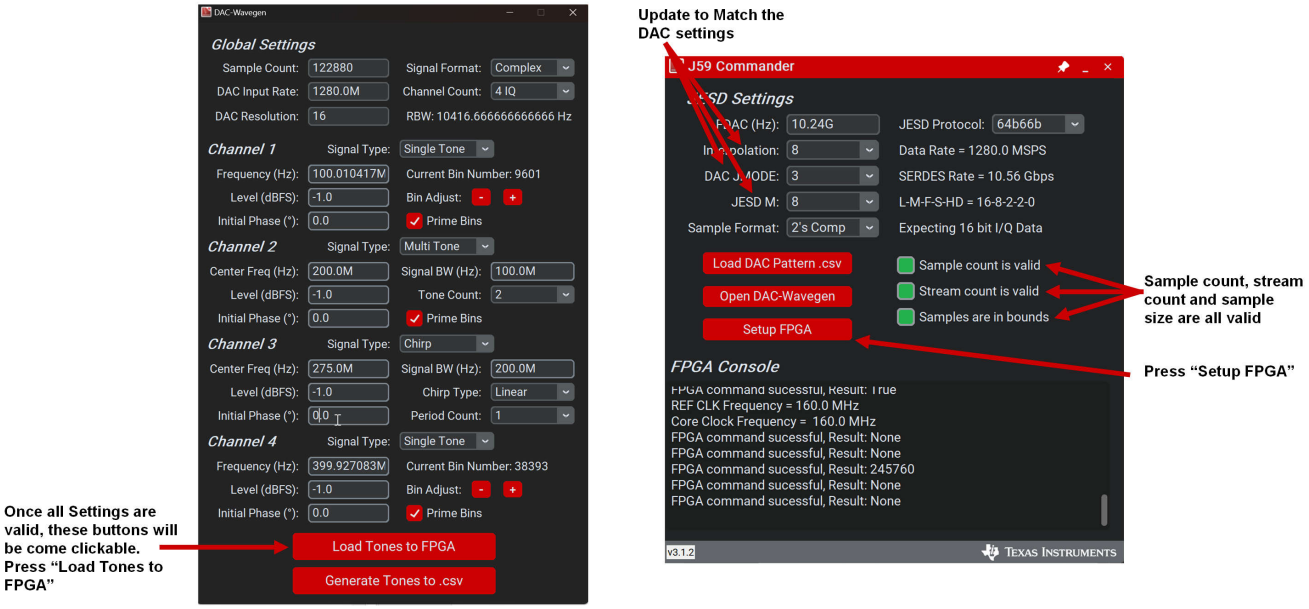


Figure 2-17. DAC Wavegen GUI & J59 Commander setup details, Step 3

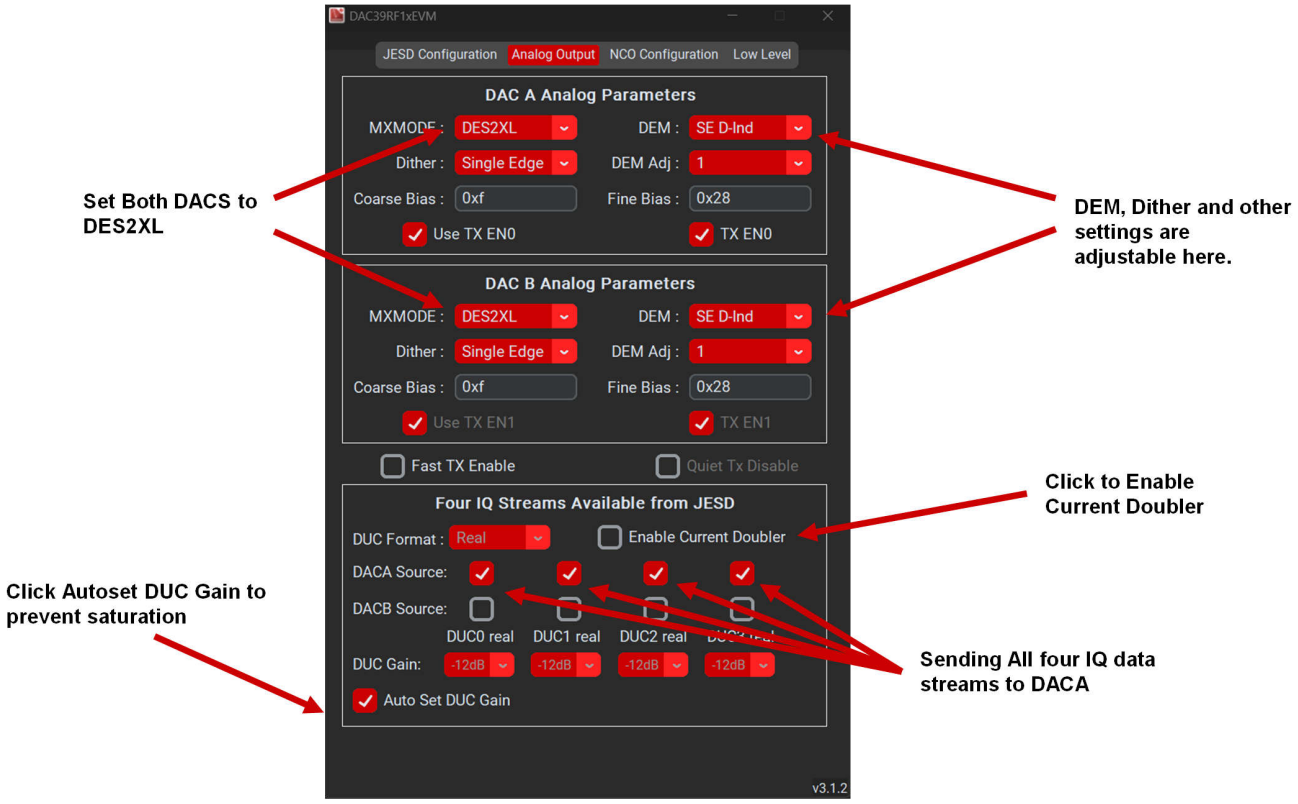


Figure 2-18. DAC39RF12EVM GUI Configuration Steps, Step 4

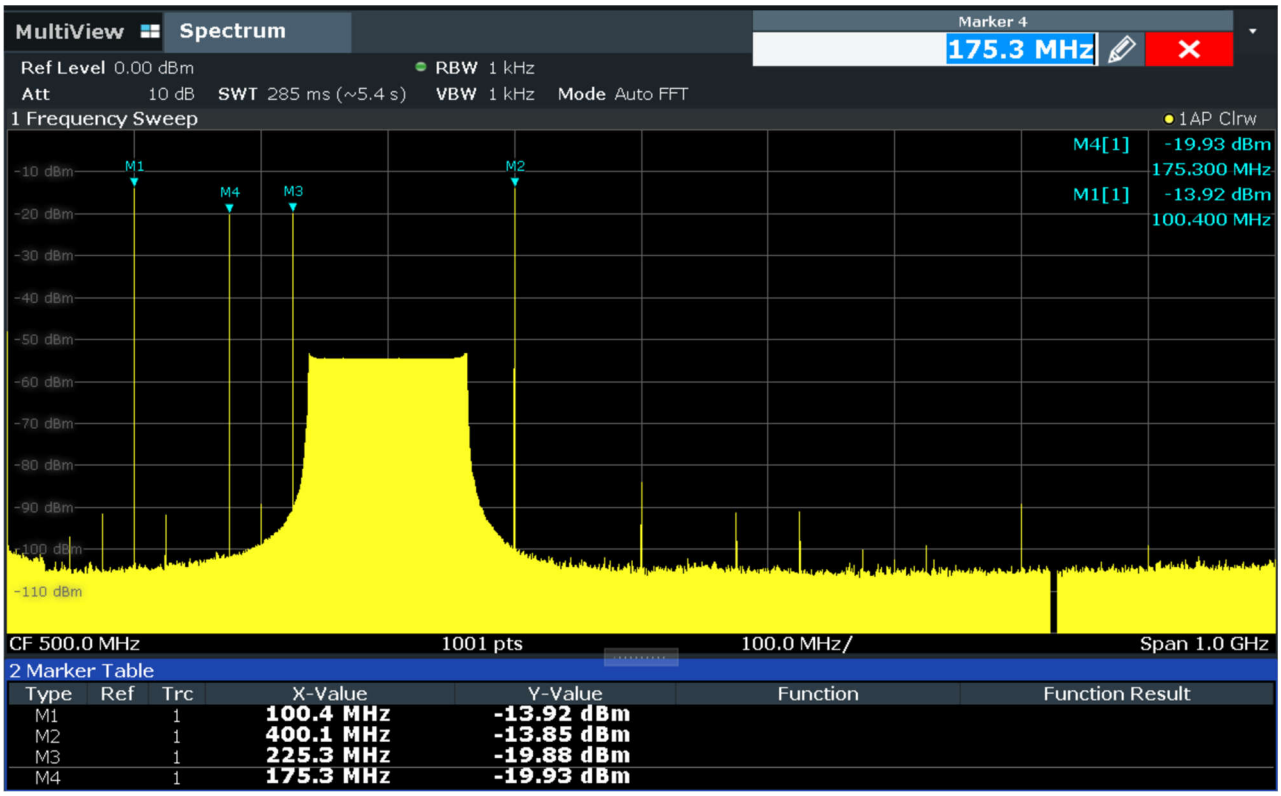


Figure 2-19. DAC39RF12EVM, CHA Output Spectrum in JMODE 3, Baseband Data

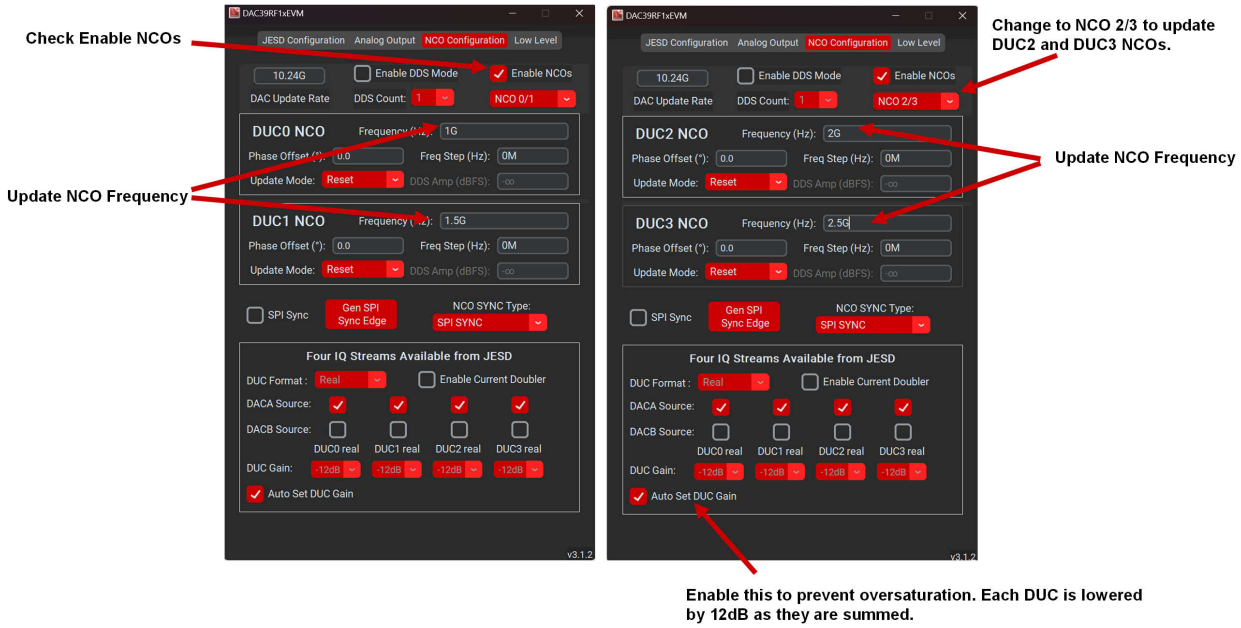


Figure 2-20. DAC39RF12EVM GUI Configuration Steps, Part 3, Enabling the NCO & Setting the frequency. Step 5

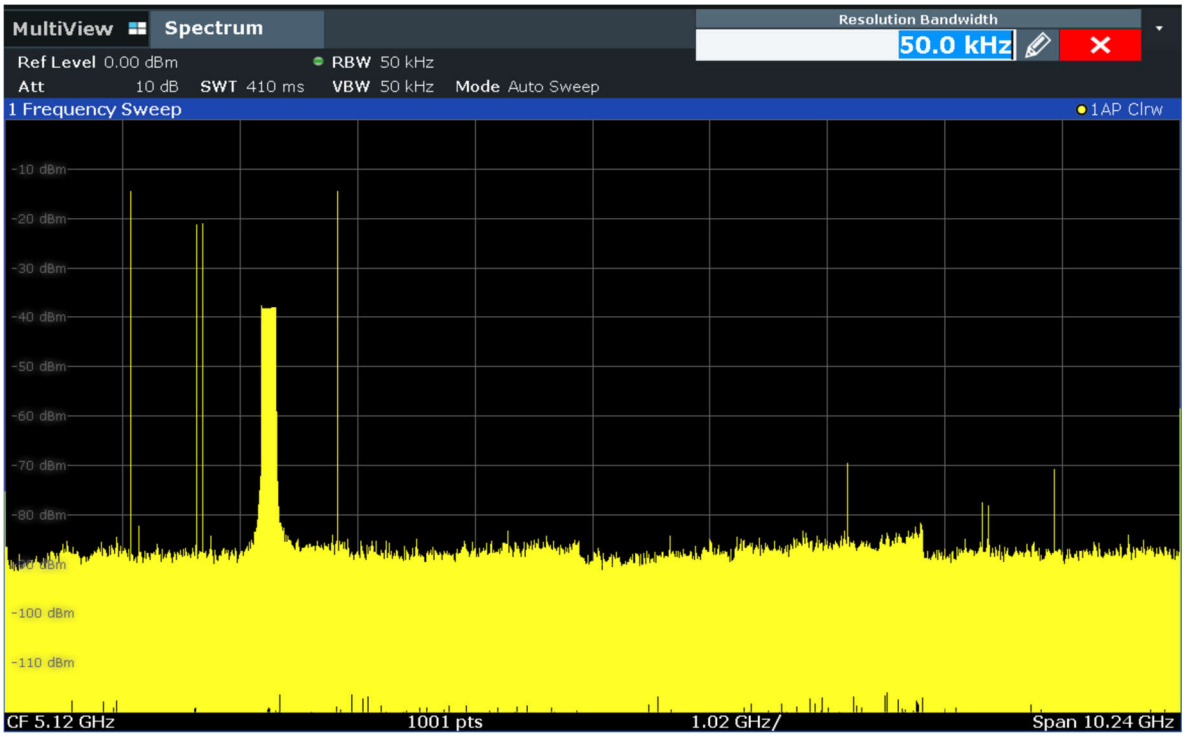


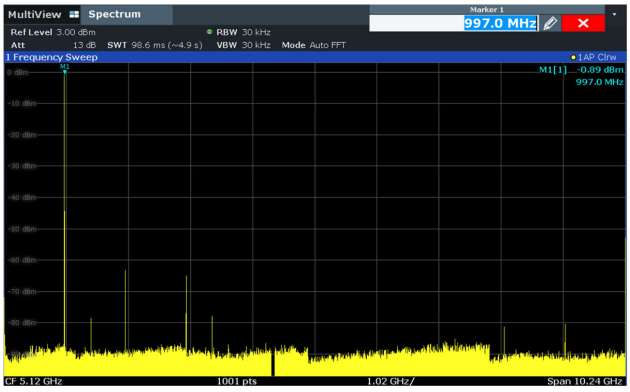
Figure 2-21. DAC39RF12EVM, CHA Output Spectrum in JMODE 3, NCO Enabled

Configuration example of DAC39RF12EVM in DDS Mode

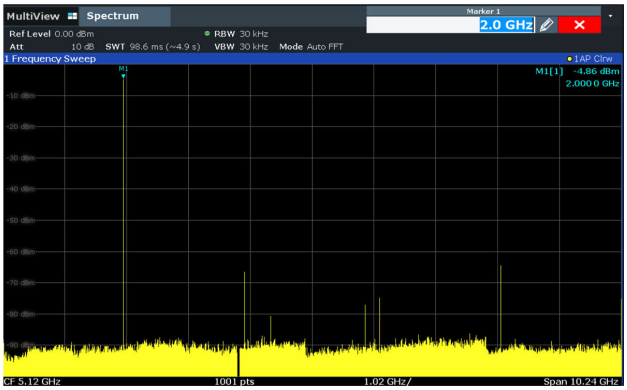
1. Enable DDS Mode
   a. Configuration details:
      i. 10.24GSPS
      ii. With DUC0 mapped to CHA & DUC1 mapped to CHB

2. Simply follow the numerated steps in the figure below after launching the DAC GUI.

Figure 2-22. DAC39RF12EVM GUI Configuration for DDS Mode



DACA Generating a 1GHz tone in DDS mode. Note the reduced 2nd Nyquist image due to DES2XL output mode



DACB Generating a 2GHz tone in DDS mode. Note the reduced 2nd Nyquist image due to DES2XL output mode

Figure 2-23. DDS Mode Output Spectrum

2.2 Evaluation Board Details: Analog Outputs

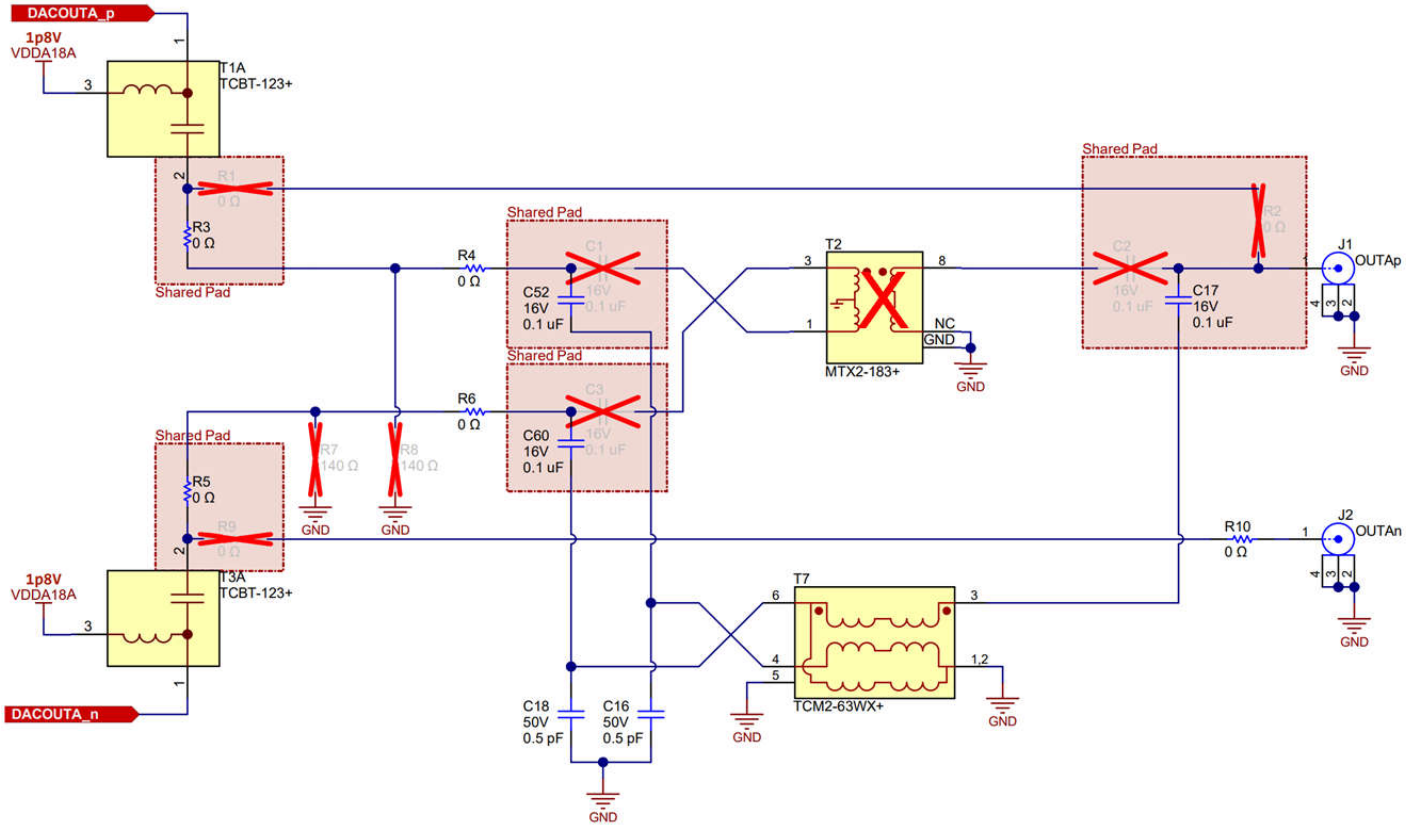
The analog output path can be configured for both a high frequency path (MTX2-183+ balun from Mini-Circuits), which is default on CHB. And low frequency path (TCM2-63WX+ balun from Mini-Circuits) which is default on CHA. To use either balun, some components must be changed to direct the output signal as appropriate. See Table 2-2.

Each analog output path also has the ability to bypass both balun options entirely and allow the user to access the outputs differentially as well. To enable this feature, some components must be changed. See Table 2-3.

Table 2-2. Component Changes to Modify DAC EVM Output Paths

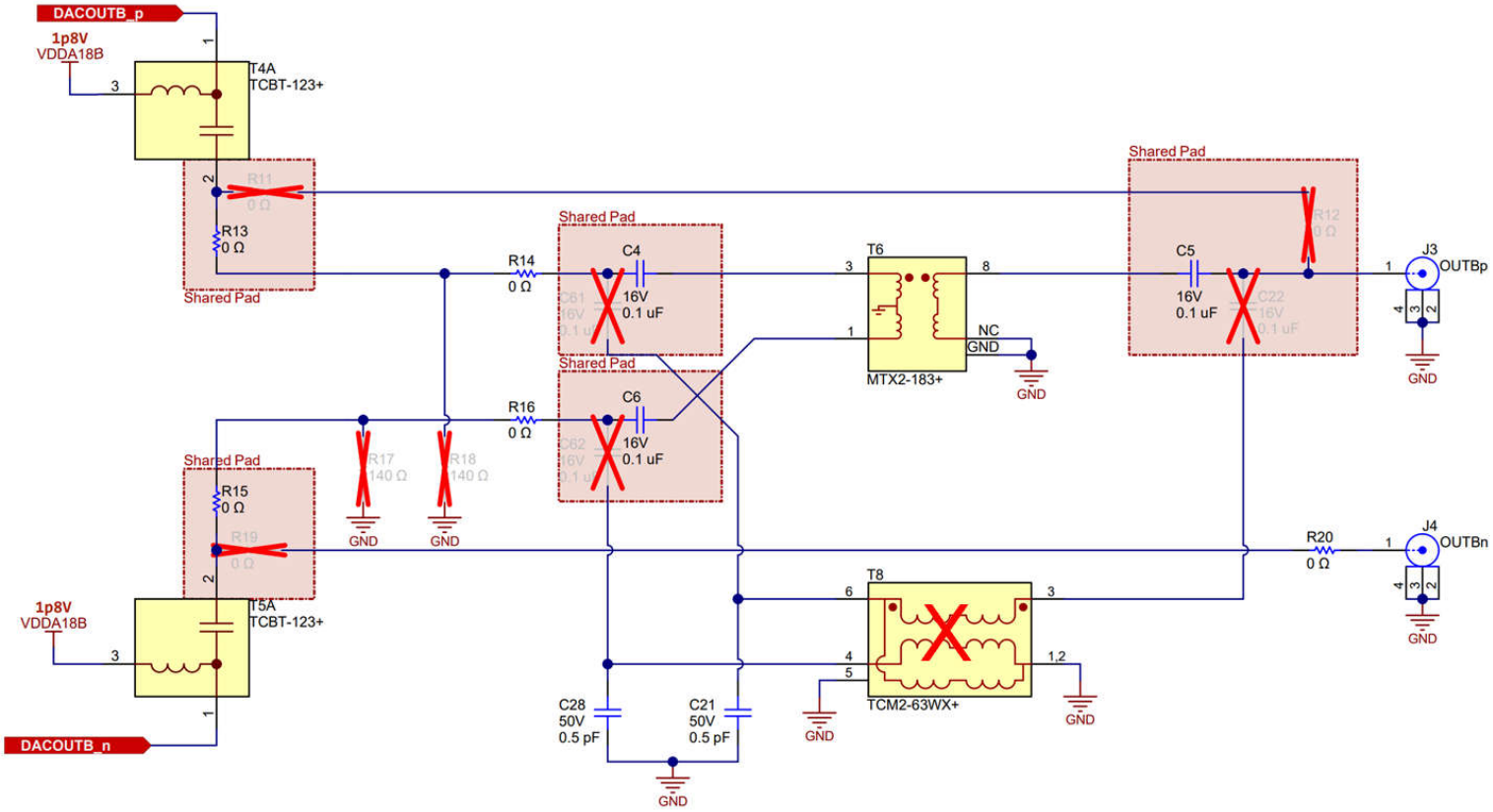
DAC Output Channel	Components to Remove	Components to Populate
CHA - Single-ended (MTX2-183+)	C52, C60, C17	C1, C2, C3 = 0.1µF
CHA - Differential (balun bypass)	R3, R5, C17	R1, R9, R2 = 0Ω
CHB - Single-ended (TCM2-63WX+)	C4, C6, C5	C61, C62, C22 = 0.1µF
CHB - Differential (balun bypass)	R13, R19, C5	R11, R15, R12 = 0Ω

Each analog output path has a wideband biasT on each output P/N pin to bias the outputs appropriately across the DAC supported bandwidth.



A. DACA Output stage. By default the TCM2-63WX+ balun is used for this channel. (30MHz to 6GHz)

Figure 2-24. Analog Output Path - CHA



A. DACB Output stage. By default the MTX2-183+ balun is used for this channel. (2MHz to 18GHz)

Figure 2-25. Analog Output Path - CHB

2.3 FMC Signal Routing

Table 2-3 provides the signal routing details for the DAC39RF12EVM.

All signal routing is handled by the DAC with the internal JESD crossbar feature.

This is also featured in the JESD crossbar dialogue box within the DAC39RF12EVM GUI.

Table 2-3. Signal Routing

DAC JESD Resource	Inverted	FMC Resource	FMC Pins	TSW14J59 FPGA Resource
Lane 9	Yes	DP0_C2M	C2, C3	Q224 MGTYTXN0
Lane 11	Yes	DP1_C2M	A22, A23	Q224 MGTYTXN1
Lane 15	Yes	DP2_C2M	A26, A27	Q224 MGTYTXN2
Lane 5	Yes	DP3_C2M	A30, A31	Q224 MGTYTXN3
Lane 3		DP4_C2M	A34, A35	Q225 MGTYTXN0
Lane 0	Yes	DP5_C2M	A38, A39	Q225 MGTYTXN1
Lane 1	Yes	DP6_C2M	B36, B37	Q225 MGTYTXN2
Lane 2	Yes	DP7_C2M	B32, B33	Q225 MGTYTXN3
Lane 7	Yes	DP8_C2M	B28, B29	Q226 MGTYTXN0
Lane 13	Yes	DP9_C2M	B24, B25	Q226 MGTYTXN1
Lane 12	Yes	DP10_C2M	Z24, Z25	Q226 MGTYTXN2
Lane 14	Yes	DP11_C2M	Y26, Y27	Q226 MGTYTXN3
Lane 6	Yes	DP12_C2M	Z28, Z29	Q227 MGTYTXN0
Lane 4	Yes	DP13_C2M	Y30, Y31	Q227 MGTYTXN1
Lane 10	Yes	DP20_C2M(1)	Z8, Z9	Q227 MGTYTXN2
Lane 8	Yes	DP21_C2M(1)	Y6, Y7	Q227 MGTYTXN3

(1) DP20_C2M and DP21_C2M can be rerouted to DP14_C2M and DP15_C2M to meet VITA compliance with other FPGA boards.

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