Functional Safety Information

INA21x-Q1 and INA199-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA21x-Q1 and INA199-Q1 (SC70-6 package) to aid in a functional safety system design. This document applies to the following devices:

- INA199-Q1
- INA210-Q1
- INA211-Q1
- INA212-Q1
- INA213-Q1
- INA214-Q1
- INA215-Q1

Information provided are:

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- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

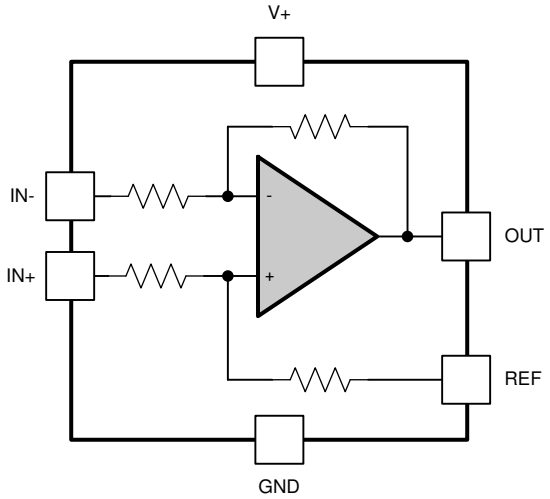

Figure 1-1. Functional Block Diagram

INA21x-Q1 and INA199-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA21x-Q1 and INA199-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 80 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA21x-Q1 and INA199-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT to GND	20%
OUT to VS	15%
OUT functional, not in specification	50%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA21x-Q1 and INA199-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V+ (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the INA21x-Q1 and INA199-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in either of the INA21x-Q1 and INA199-Q1 datasheets.

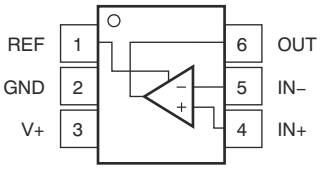

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_{V+} = 5 V
- V_{IN+} = 12 V
- $V_{REF} = V_{V+} / 2$

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; C otherwise
GND	2	Normal operation.	D
V+	3	Power supply shorted to GND.	B
OUT	4	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-	5	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+	6	In high-side configuration, a short from the bus supply to GND will occur.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	C
GND	2	No power to device. Device may be biased through inputs. Output will no longer be referenced to GND.	B
V+	3	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B
OUT	4	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-	5	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed V+ or GND.	B
IN+	6	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed V+ or GND.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	2 - GND	Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; C otherwise
GND	2	3 - V+	Power supply shorted to GND.	B
V+	3	4 - OUT	Output will be pulled to V+ and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
OUT	4	5 - IN-	In high-side configuration, OUT shorted to bus supply with damage possible. In low-side configuration, OUT shorted to GND.	A for high-side; B for low-side.
IN-	5	6 - IN+	Inputs shorted together, so no sense voltage applied. Output will stay close to REF potential.	B
IN+	6	1 - REF	In high-side configuration, REF shorted to bus supply with damage possible. In low-side configuration, REF shorted to GND (normal operation if REF is at GND potential by design).	A for high-side; C for low-side (D if REF=GND by design)

Table 4-5. Pin FMA for Device Pins Short-Circuited to V+

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	Normal operation if REF pin is at V+ potential by design; otherwise the system measurement will be incorrect.	D if REF=V+ by design; C otherwise.
GND	2	Power supply shorted to GND.	B
V+	3	Normal operation.	D
OUT	4	Output will be pulled to V+ and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-	5	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	B
IN+	6	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2020) to Revision A (April 2021) **Page**

- Added the INA199-Q1 device to the document..... 1

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