TMCS1100-Q1 AEC-Q100, 1% High-Precision, Basic Isolation Hall-Effect Current Sensor With ±600V Working Voltage

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature Grade 1: –40°C to 125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Total error: ±0.4% typical, ±0.9% maximum, –40°C to 85°C
  - Sensitivity error: ±0.4%
  - Offset error: 7mA
  - Offset drift: 0.04mA/°C
  - Linearity error: 0.05%
- Lifetime and environmental drift: <±0.5%
- 3kV_{RMS} isolation rating
- Robust 600V lifetime working voltage
- Bidirectional and unidirectional current sensing
- External reference voltage
- Operating supply range: 3V to 5.5V
- Signal bandwidth: 80kHz
- Multiple sensitivity options:
  - TMCS1100A1-Q1: 50mV/A
  - TMCS1100A2-Q1: 100mV/A
  - TMCS1100A3-Q1: 200mV/A
  - TMCS1100A4-Q1: 400mV/A
- Safety related certifications
  - UL 1577 Component Recognition Program
  - IEC/CB 62368-1

2 Applications

- Motor and load control
- Inverter and H-bridge current measurements
- Power factor correction
- Overcurrent protection
- DC and AC power monitoring

3 Description

The TMCS1100-Q1 is a galvanically isolated Hall-effect current sensor capable of DC or AC current measurement with high accuracy, excellent linearity, and temperature stability. A low-drift, temperature-compensated signal chain provides < 1% full-scale error across the device temperature range.

The input current flows through an internal 1.8mΩ conductor that generates a magnetic field measured by an integrated Hall-effect sensor. This structure eliminates external concentrators and simplifies design. Low conductor resistance minimizes power loss and thermal dissipation. Inherent galvanic insulation provides a 600V lifetime working voltage and 3kV_{RMS} basic isolation between the current path and circuitry. Integrated electrical shielding enables excellent common-mode rejection and transient immunity.

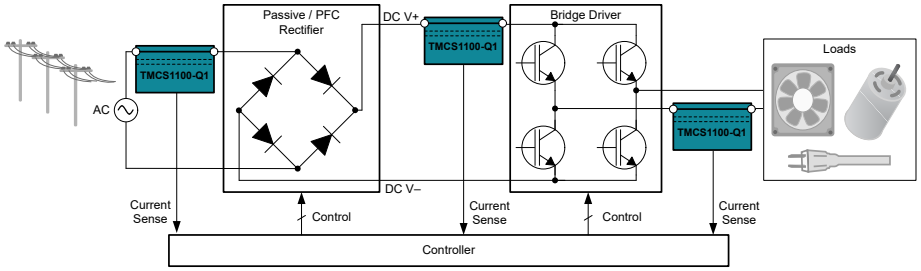
The output voltage is proportional to the input current with four sensitivity options. Fixed sensitivity allows the TMCS1100-Q1 to operate from a single 3V to 5.5V power supply, eliminates ratiometry errors, and improves supply noise rejection. The current polarity is considered positive when flowing into the positive input pin. The VREF input pin provides a variable zero-current output voltage, enabling bidirectional or unidirectional current sensing.

The TMCS1100-Q1 draws a maximum supply current of 6mA, and all sensitivity options are specified over the operating temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMCS1100-Q1	D (SOIC, 8)	4.9mm × 6mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Device Comparison

Table 4-1. Device Comparison

PRODUCT	SENSITIVITY	BIDIRECTIONAL LINEAR MEASUREMENT RANGE, V_{REF} = V_S / 2(1)		UNIDIRECTIONAL LINEAR MEASUREMENT RANGE, V_{REF} = V_{GND} (1)	
	ΔV_{OUT} / $\Delta I_{IN+, IN-}$	V_S = 5V	V_S = 3.3V	V_S = 5V	V_S = 3.3V
TMCS1100A1-Q1	50mV/A	±46A(2)	±29A(2)	1A to 96A(2)	1A to 62A(2)
TMCS1100A2-Q1	100mV/A	±23A(2)	±14.5A	0.5A to 48A(2)	0.5A to 31A(2)
TMCS1100A3-Q1	200mV/A	±11.5A	±7.25A	0.25A to 24A(2)	0.25A to 15.5A
TMCS1100A4-Q1	400mV/A	±5.75A	--	0.125A to 12A	--

(1) Linear range limited by swing to supply and ground.
(2) Current levels must remain below both allowable continuous DC/RMS and transient peak current safe operating areas to not exceed device thermal limits. See the *Safe Operating Area* section.

5 Pin Configuration and Functions

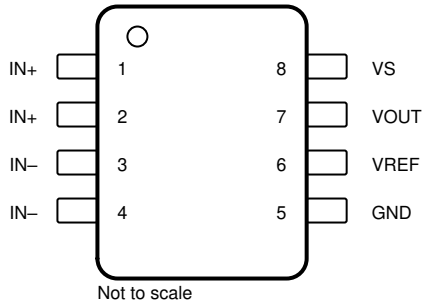


Figure 5-1. D Package 8-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		Type	DESCRIPTION
NO.	NAME		
1	IN+	Analog input	Input current positive pin
2	IN+	Analog input	Input current positive pin
3	IN–	Analog input	Input current negative pin
4	IN–	Analog input	Input current negative pin
5	GND	Analog	Ground
6	VREF	Analog input	Zero current output voltage reference
7	VOUT	Analog output	Output voltage
8	VS	Analog	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage		GND – 0.3	6	V
	Analog input	VREF	GND – 0.3	(V_S) + 0.3	V
	Analog output	VOUT	GND – 0.3	(V_S) + 0.3	V
T_J	Junction temperature		–65	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN+},V_{IN-} (1)	Input voltage	–600		600	V_{PK}
V_S	Operating supply voltage, TMCS1100A1-Q1 – TMCS1100A3-Q1	3	5	5.5	V
V_S	Operating supply voltage, TMCS1100A4-Q1	4.5	5	5.5	V
T_A (2)	Operating free-air temperature	–40		125	°C

(1) V_{IN+} and V_{IN-} refer to the voltage at input current pins IN+ and IN–, relative to pin 5 (GND).
(2) Input current safe operating area is constrained by junction temperature. Recommended condition based on the TMCS1100EVM . Input current rating is derated for elevated ambient temperatures.

6.4 Thermal Information

THERMAL METRIC(1)		TMCS1100-Q1 (2) D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	–0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Applies when device mounted on TMCS1100EVM . For more details, see the *Safe Operating Area* section.

6.5 Power Ratings

V_S = 5.5 V, V_{REF} = GND, T_A = 125°C, T_J = 150°C, device soldered on TMCS1100EVM .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)				673	mW
P_{D1}	Maximum power dissipation (current input, side-1)	I_{IN} = 16 A			640	mW
P_{D2}	Maximum power dissipation by (side-2)	V_S = 5.5 V, I_Q = 6mA, no VOUT load			33	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	60	µm
CTI	Comparative tracking index	DIN EN 60112; IEC 60112	>400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	600	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); Time Dependent Dielectric Breakdown test, see Insulation Lifetime.	424	V_{RMS}
		DC voltage	600	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM} = 4242V_{PK}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM} = 5090V_{PK}$, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800V_{PK}$ (qualification)	6000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM} = 4242V_{PK}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 700V_{PK}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM} = 4242V_{PK}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 700V_{PK}$, t_m = 10 s	≤5	
		Method b3: At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM} = 5090V_{PK}$, t_{ini} = 1 s; $V_{pd(m)} = 1.2 \times V_{IOTM} = 5090V_{PK}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	0.6	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	Ω
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Take care to maintain the creepage and clearance distance of the board design to make sure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

UL	
UL 1577 Component Recognition Program	Certified according to IEC 62368-1 CB
File number: E181974	Certificate number: US-36733-UL

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input current (side 1)(1)	$R_{\theta JA}$ = 36.6°C/W, T_J = 150°C, T_A = 25°C, see Thermal Derating Curve, Side 1.			30	A
I_S	Safety input, output, or supply current (side 2)(1)	$R_{\theta JA}$ = 36.6°C/W, V_I = 5 V, T_J = 150°C, T_A = 25°C, see Thermal Derating Curve, Side 2.			0.68	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 36.6°C/W, T_J = 150°C, T_A = 25°C, see Thermal Derating Curve, Both Sides.			3.4	W
T_S	Safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Section 6.4* table is that of a device installed on the TMCS1100EVM . Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

at T_A = 25°C, V_S = 5 V, V_{REF} = 2.5 V (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Sensitivity[7]	TMCS1100A1-Q1		50		mV/A
		TMCS1100A2-Q1		100		mV/A
		TMCS1100A3-Q1		200		mV/A
		TMCS1100A4-Q1		400		mV/A
	Sensitivity error	0.05 V ≤ V_{OUT} ≤ V_S – 0.2 V, T_A= 25ºC		±0.2%	±0.7%	
	Sensitivity error, including lifetime and environmental drift [5]	0.05 V ≤ V_{OUT} ≤ V_S – 0.2 V, T_A= 25ºC		-0.47%	±1.02%	
	Sensitivity error	0.05 V ≤ V_{OUT} ≤ V_S – 0.2 V, T_A= –40ºC to +85ºC		±0.4%	±0.85%	
		0.05 V ≤ V_{OUT} ≤ V_S – 0.2 V, T_A= –40ºC to +125ºC		±0.5%	±1.15%	
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.05%		
V_{OE}	Output voltage offset error[1]	TMCS1100A1-Q1		±0.4	±3	mV
		TMCS1100A2-Q1		±0.6	±5	mV
		TMCS1100A3-Q1		±0.8	±8	mV
		TMCS1100A4-Q1		±2.2	±19	mV
	Output voltage offset drift	TMCS1100A1-Q1, T_A= –40ºC to +125ºC		±3.7	±12	µV/ºC
		TMCS1100A2-Q1, T_A= –40ºC to +125ºC		±4	±19	µV/ºC
		TMCS1100A3-Q1, T_A= –40ºC to +125ºC		±8.2	±35	µV/ºC
		TMCS1100A4-Q1, T_A= –40ºC to +125ºC		±26	±138	µV/ºC
I_{OS}	Offset error, RTI[1] [3]	TMCS1100A1-Q1		±8	±60	mA
		TMCS1100A2-Q1		±6	±50	mA
		TMCS1100A3-Q1		±4	±40	mA
		TMCS1100A4-Q1		±5.5	±47.5	mA
	Offset error temperature drift, RTI[3]	TMCS1100A1-Q1, T_A= –40ºC to +125ºC		±74	±240	µA/°C
		TMCS1100A2-Q1, T_A= –40ºC to +125ºC		±40	±190	µA/°C
		TMCS1100A3-Q1, T_A= –40ºC to +125ºC		±41	±175	µA/°C
		TMCS1100A4-Q1, T_A= –40ºC to +125ºC		±65	±345	µA/°C
PSRR	Power-supply rejection ratio	TMCS1100A1-Q1 – TMCS1100A3-Q1, V_S = 3 V to 5.5 V, V_{REF} = V_S/2, T_A= –40ºC to +125ºC		±1	±2	mV/V
		TMCS1100A4-Q1, V_S = 4.5 V to 5.5 V, V_{REF} = V_S/2, T_A= –40ºC to +125ºC		±1	±3	mV/V
CMTI	Common mode transient immunity			50		kV/µs
CMRR	Common mode rejection ratio, RTI[3]	DC to 60Hz		5		uA/V
RVRR	Reference voltage rejection ratio, output referred	TMCS1100A1-Q1 – TMCS1100A3-Q1, V_{REF} = 0.5 V to 4.5 V		1	3.5	mV/V
		TMCS1100A4-Q1, V_{REF} = 0.5 V to 4.5 V		1.5	8	mV/V
	Noise density, RTI[3]	TMCS1100A1-Q1		380		µA/√Hz
		TMCS1100A2-Q1		330		µA/√Hz
		TMCS1100A3-Q1		300		µA/√Hz
		TMCS1100A4-Q1		225		µA/√Hz
INPUT						
R_{IN}	Input conductor resistance	IN+ to IN–		1.8		mΩ
	Input conductor resistance temperature drift	T_A= –40ºC to +125ºC		4.4		µΩ/°C
G	Magnetic coupling factor	T_A= 25ºC		1.1		mT/A
$I_{IN,max}$	Allowable continuous RMS current [4]	T_A= 25ºC		30		A
		T_A= 85ºC		25		A
		T_A= 105ºC		22.5		A
		T_A= 125ºC		16		A

at T_A = 25°C, V_S = 5 V, V_{REF} = 2.5 V (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference input voltage		V_{GND}		V_S	V
	V_{REF} input current	VREF = GND, VS		±1	±5	µA
	V_{REF} external source impedance	Maximum source impedance of external circuit driving V_{REF}			5	kΩ
VOLTAGE OUTPUT						
Z_{OUT}	Closed loop output impedance	f = 1 Hz to 1 kHz		0.2		Ω
		f = 10 kHz		2		Ω
	Maximum capacitive load	No sustained oscillation		1		nF
	Short circuit output current	VOUT short to ground, short to V_S		90		mA
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A= –40ºC to +125ºC		V_S – 0.02	V_S – 0.1	V
	Swing to GND, current driven	R_L = 10 kΩ to GND, T_A= –40ºC to +125ºC		V_{GND} + 5	V_{GND} + 10	mV
	Swing to GND, zero current	TMCS1100A1-Q1 – TMCS1100A3-Q1, R_L = 10 kΩ to GND, T_A= –40ºC to +125ºC, VREF = GND, I_{IN} = 0 A		V_{GND} + 5	V_{GND} + 20	mV
		TMCS1100A4-Q1, R_L = 10 kΩ to GND, T_A= –40ºC to +125ºC, VREF = GND, I_{IN} = 0 A		V_{GND} + 20	V_{GND} + 55	mV
FREQUENCY RESPONSE						
BW	Bandwidth(6)	–3-dB Bandwidth		80		kHz
SR	Slew rate(6)	Slew rate of output amplifier during single transient step.		1.5		V/µs
t_r	Response time(6)	Time between the input current step reaching 90% of final value to the sensor output reaching 90% of its final value, for a 1V output transition.		6.5		µs
t_p	Propagation delay(6)	Time between the input current step reaching 10% of final value to the sensor output reaching 10% of its final value, for a 1V output transition.		4		µs
$t_{r,SC}$	Current overload response time(6)	Time between the input current step reaching 90% of final value to the sensor output reaching 90% of its final value. Input current step amplitude is twice full scale output range.		5		µs
$t_{p,SC}$	Current overload propagation delay(6)	Time between the input current step reaching 10% of final value to the sensor output reaching 10% of its final value. Input current step amplitude is twice full scale output range.		3		µs
	Current overload recovery time	Time from end of current causing output saturation condition to valid output		15		µs
POWER SUPPLY						
I_Q	Quiescent current	T_A = 25ºC		4.5	5.5	mA
		T_A = –40ºC to +125ºC			6	mA
	Power on time	Time from V_S > 3 V to valid output		25		ms

(1) Excludes effect of external magnetic fields. See the *Accuracy Parameters* section for details to calculate error due to external magnetic fields.
(2) Excluding magnetic coupling from layout deviation from recommended layout. See the *Layout* section for more information.
(3) RTI = referred-to-input. Output voltage is divided by device sensitivity to refer signal to input current. See the *Parameter Measurement Information* section.
(4) Thermally limited by junction temperature. Applies when device mounted on TMCS1100EVM . For more details, see the *Safe Operating Area* section.
(5) Lifetime and environmental drift specifications based on three lot AEC-Q100 qualification stress test results. Typical values are population mean+1σ from worst case stress test condition. Min/max are tested device population mean±6σ; devices tested in AEC-Q100 qualification stayed within min/max limits for all stress conditions. See *Lifetime and Environmental Stability* section for more details.
(6) Refer to the *Transient Response* section for details of frequency and transient response of the device.
(7) Centered parameter based on TMCS1100EVM PCB layout. See *Layout* section. Device must be operated below maximum junction temperature.

6.10 Typical Characteristics

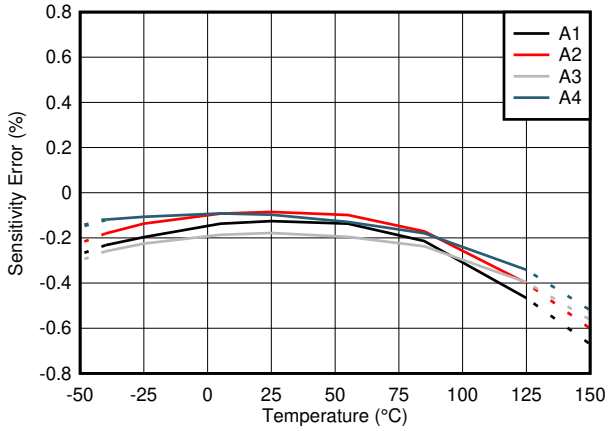


Figure 6-1. Sensitivity Error vs Temperature

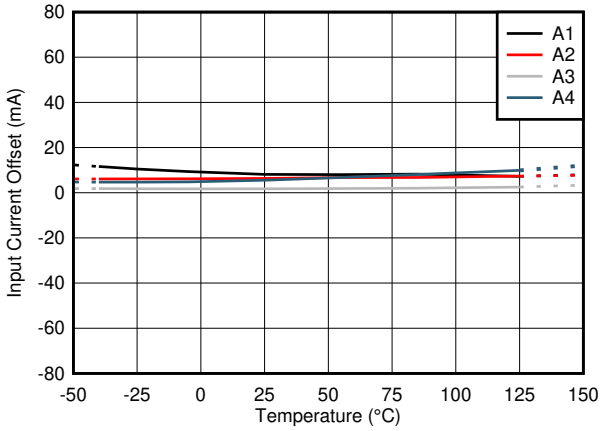


Figure 6-2. Input Offset Current vs Temperature

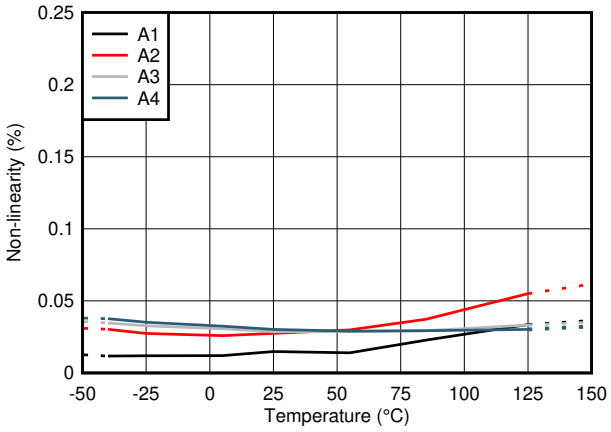


Figure 6-3. Non-Linearity vs Temperature

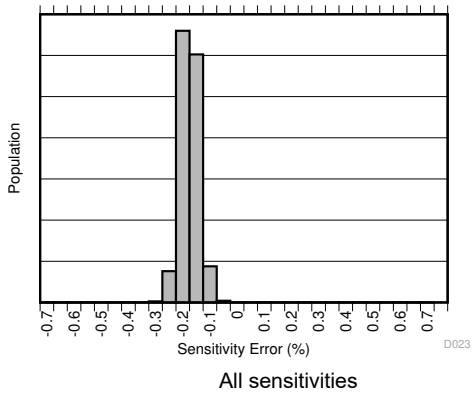


Figure 6-4. Sensitivity Error Production Distribution

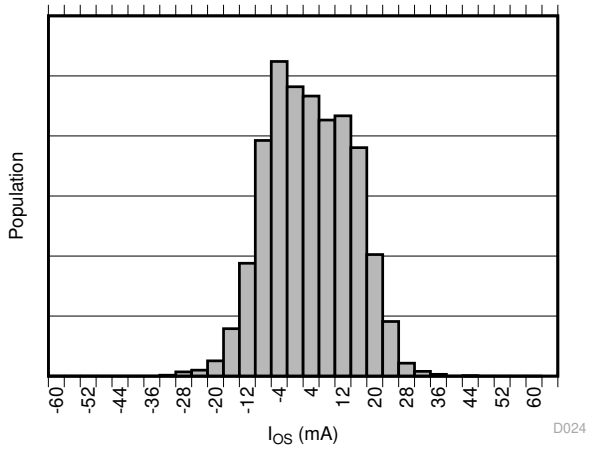


Figure 6-5. Input Offset Current Production Distribution

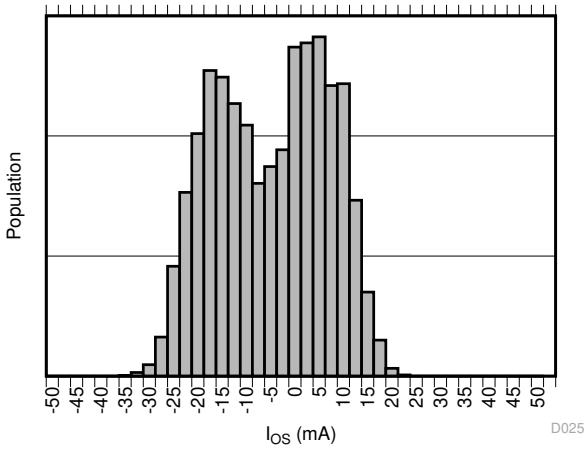


Figure 6-6. Input Offset Current Production Distribution

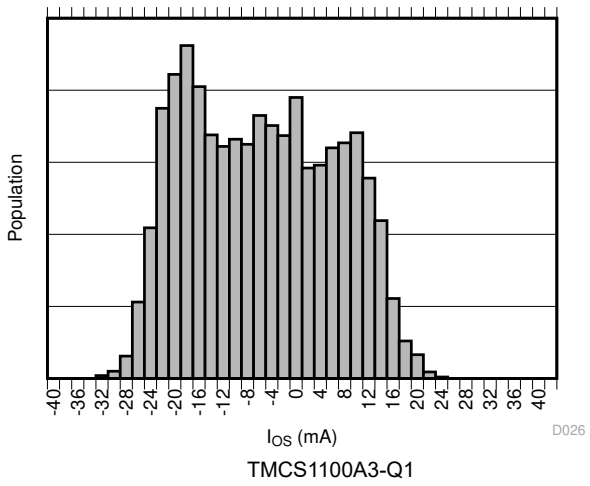


Figure 6-7. Input Offset Current Production Distribution

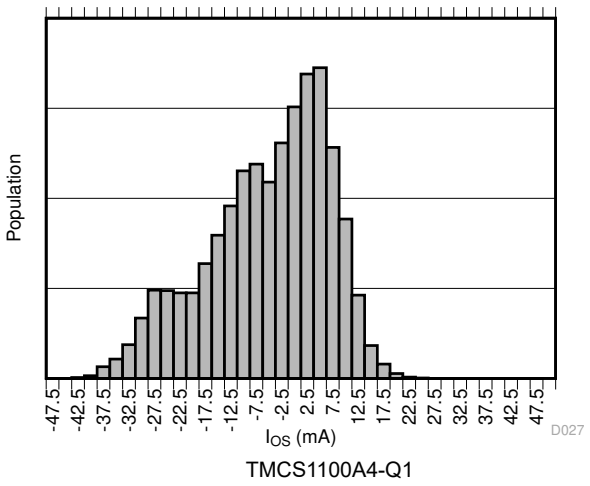


Figure 6-8. Input Offset Current Production Distribution

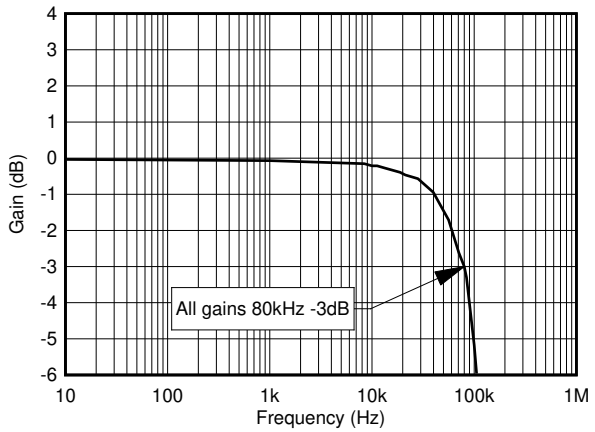


Figure 6-9. Sensitivity vs Frequency, All Gains Normalized to 1Hz

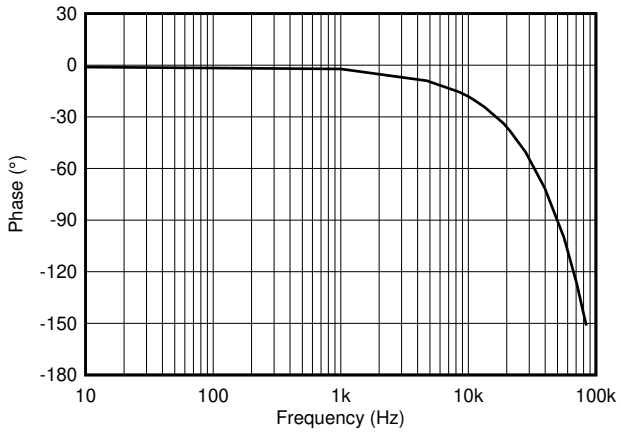


Figure 6-10. Phase vs Frequency, All Gains

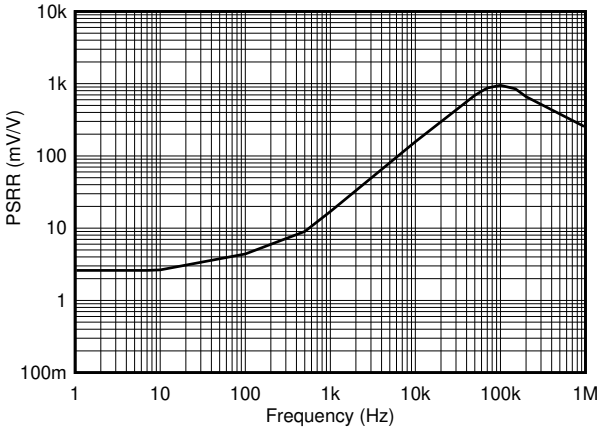


Figure 6-11. PSRR vs Frequency

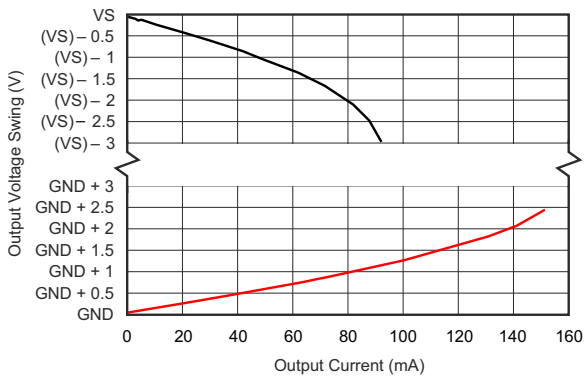


Figure 6-12. Output Swing vs Output Current

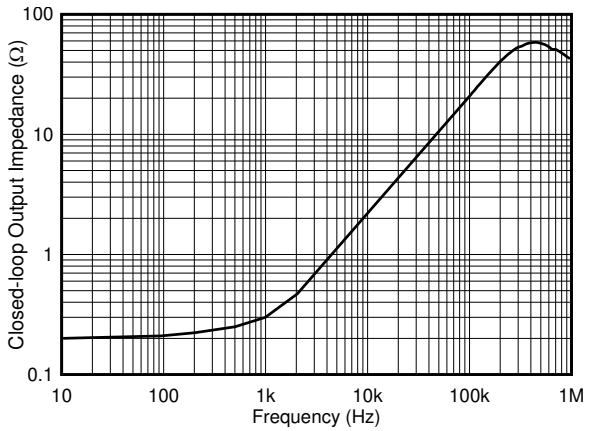


Figure 6-13. Output Impedance vs Frequency

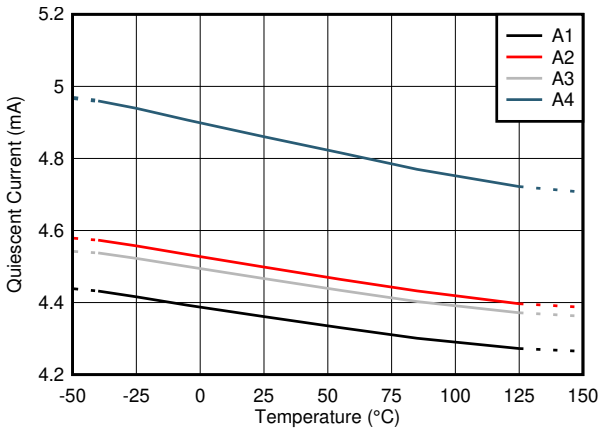


Figure 6-14. Quiescent Current vs Temperature

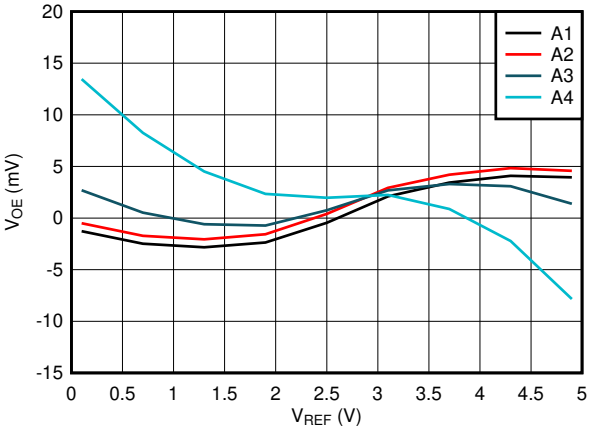


Figure 6-15. Output Voltage Offset vs V_{REF}

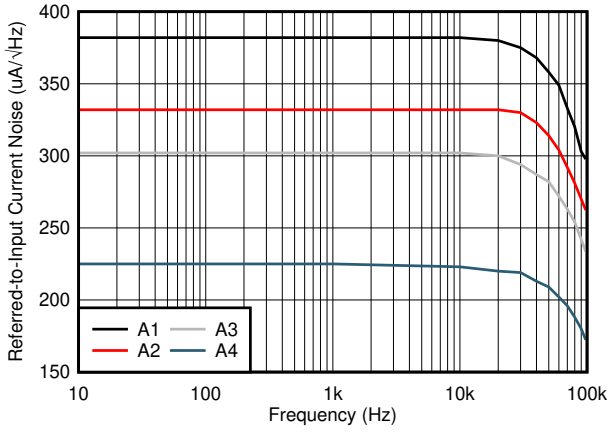


Figure 6-16. Input-Referred Noise vs Frequency

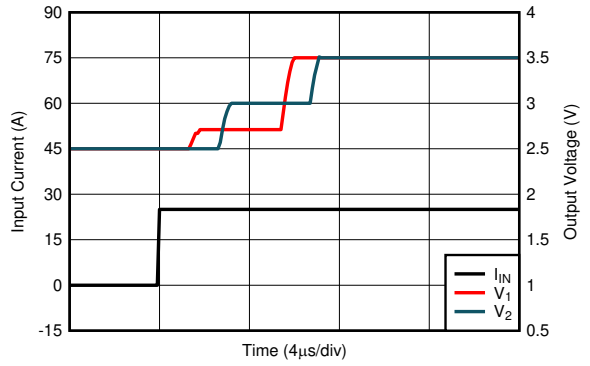


Figure 6-17. Voltage Output Step, Rising

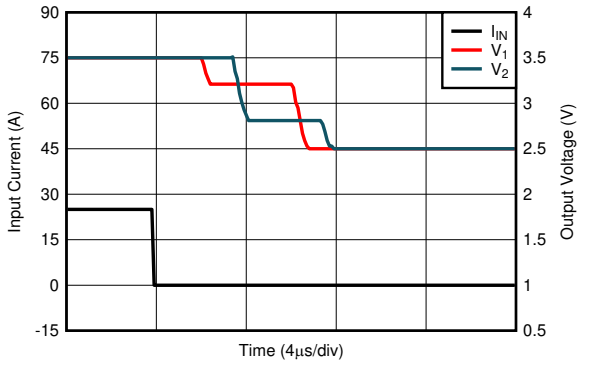


Figure 6-18. Voltage Output Step, Falling

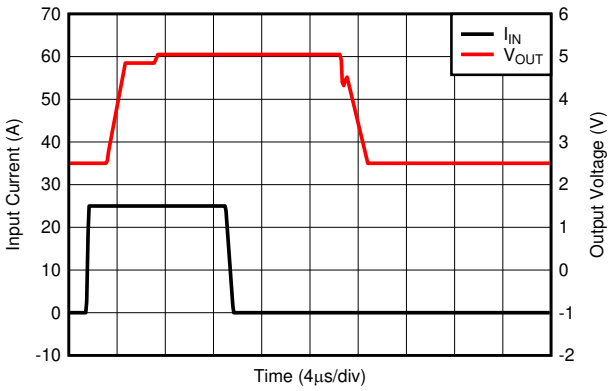


Figure 6-19. Current Overload Response

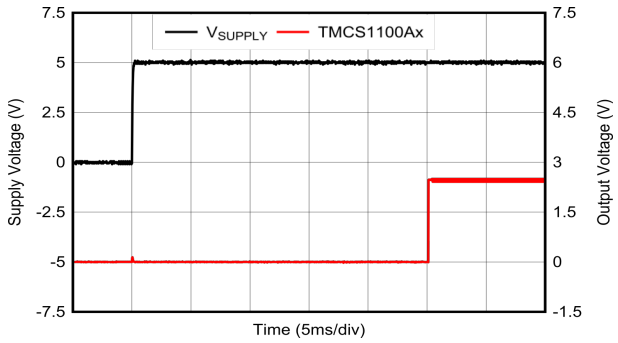


Figure 6-20. Startup Transient Response

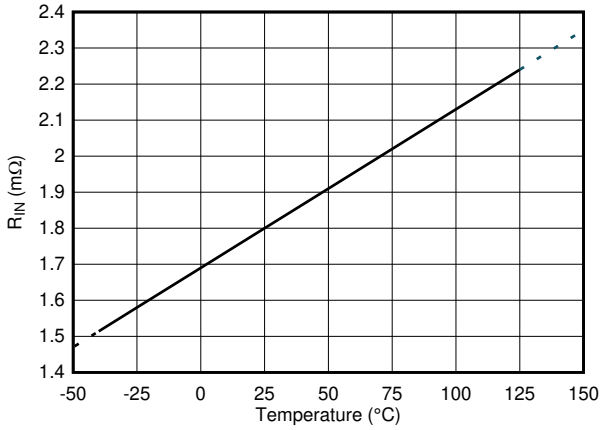


Figure 6-21. Input Conductor Resistance vs Temperature

6.10.1 Insulation Characteristics Curves

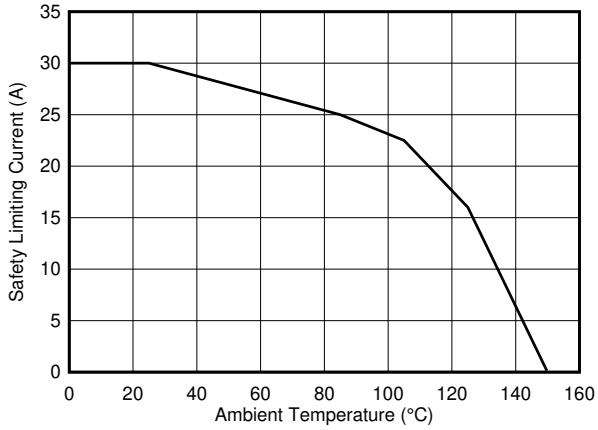


Figure 6-22. Thermal Derating Curve for Safety-Limiting Current, Side 1

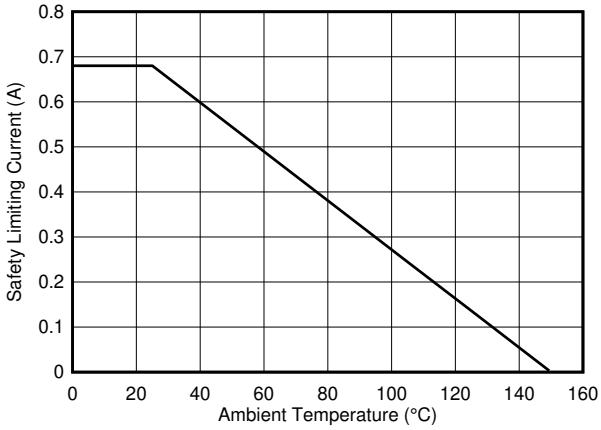


Figure 6-23. Thermal Derating Curve for Safety-Limiting Current, Side 2

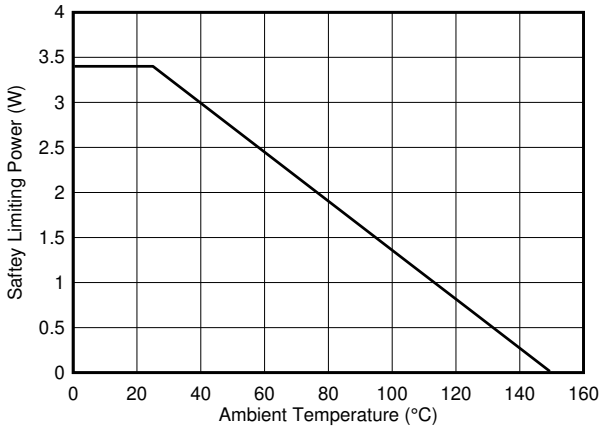


Figure 6-24. Thermal Derating Curve for Safety-Limiting Power

7 Parameter Measurement Information

7.1 Accuracy Parameters

The ideal first-order transfer function of the TMCS1100-Q1 is given by Equation 1, where the output voltage is a linear function of input current. The accuracy of the device is quantified both by the error terms in the transfer function parameters, as well as by nonidealities that introduce additional error terms not in the simplified linear model. See *Total Error Calculation Examples* for example calculations of total error, including all device error terms.

$$V_{OUT} = S \times I_{IN} + V_{REF} \quad (1)$$

where

- V_{OUT} is the analog output voltage.
- S is the ideal sensitivity of the device.
- I_{IN} is the isolated input current.
- V_{REF} is the voltage applied to the reference voltage input.

where

- V_{OUT} is the analog output voltage.
- S is the ideal sensitivity of the device.
- I_{IN} is the isolated input current.
- $V_{OUT,0A}$ is the zero current output voltage for the device variant.

7.1.1 Sensitivity Error

Sensitivity is the proportional change in the sensor output voltage due to a change in the input conductor current. This sensitivity is the slope of the first-order transfer function of the sensor, as shown in Figure 7-1. The sensitivity of the TMCS1100-Q1 is tested and calibrated at the factory for high accuracy.

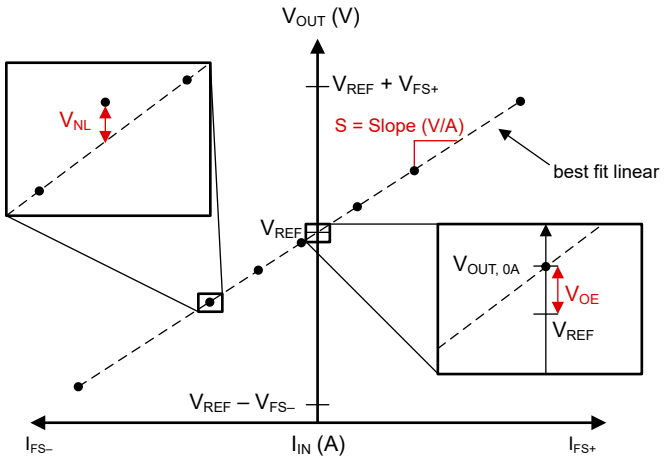


Figure 7-1. Sensitivity, Offset, and Nonlinearity Error

Deviation from ideal sensitivity is quantified by sensitivity error, defined as the percent variation of the best-fit measured sensitivity from the ideal sensitivity. When specified over a temperature range, this is the worst-case sensitivity error at any temperature within the range.

$$e_S = [(S_{fit} - S_{ideal}) / S_{ideal}] \times 100\% \quad (2)$$

where

- e_S is the sensitivity error.
- S_{fit} is the best fit sensitivity.
- S_{Ideal} is the ideal sensitivity.

7.1.2 Offset Error and Offset Error Drift

Offset error is the deviation from the ideal output voltage with zero input current through the device. Offset error can be referred to the output as a voltage error V_{OE} or referred to the input as a current offset error I_{OS}. Offset error is a single error source, however, and must only be included once in error calculations.

The output voltage offset error of the TMCS1100-Q1 is the error in the zero current output voltage from the VREF pin voltage as in Equation 3.

$$V_{OE} = V_{OUT,0A} - V_{REF} \quad (3)$$

where

- $V_{OUT,0A}$ is the device output voltage with zero input current.

The offset error includes the magnetic offset of the Hall sensor and any offset voltage errors of the signal chain.

The input referred (RTI) offset error is the output voltage offset error divided by the sensitivity of the device, shown in Equation 4. Refer the offset error to the input of the device to allow for easier total error calculations and direct comparison to input current levels. No matter how the calculations are done, the error sources quantified by V_{OE} and I_{OS} are the same, and must only be included once for error calculations.

$$I_{OS} = \frac{V_{OE}}{S} \quad (4)$$

Offset error drift is the change in the input-referred offset error per degree Celsius change in ambient temperature. This parameter is reported in µA/°C. To convert offset drift to an absolute offset for a given change in temperature, multiply the drift by the change in temperature and convert to percentage, as in Equation 5.

$$e_{I_{OS,\,\Delta T}}(\%) = \frac{I_{OS,\,25°C} + I_{OS,\,drift}\left(\frac{\mu A}{°C}\right) \times \Delta T}{I_{IN}} \quad (5)$$

where

- $I_{OS,drift}$ is the specified input-referred device offset drift.
- ΔT is the temperature range from 25°C.

7.1.3 Nonlinearity Error

Nonlinearity is the deviation of the output voltage from a linear relationship to the input current. Nonlinearity voltage, as shown in Figure 7-1, is the maximum voltage deviation from the best-fit line based on measured parameters, calculated by Equation 6.

$$V_{NL} = V_{OUT,MEAS} - (I_{MEAS} \times S_{fit} + V_{OUT,0A}) \quad (6)$$

where

- $V_{OUT,MEAS}$ is the voltage output at maximum deviation from best fit.
- I_{MEAS} is the input current at maximum deviation from best fit.
- S_{fit} is the best-fit sensitivity of the device.
- $V_{OUT,0A}$ is the device zero current output voltage.

Nonlinearity error (e_{NL}) for the TMCS1100-Q1 is the nonlinearity voltage specified as a percentage of the full-scale output range (V_{FS}), as shown in Equation 7.

$$e_{NL} = 100\% \times \frac{V_{NL}}{V_{FS}} \quad (7)$$

7.1.4 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is the change in device offset due to variation of supply voltage from the nominal 5V. The error contribution at the input current of interest can be calculated by Equation 8.

$$e_{PSRR}\left(\%\right) = \frac{PSRR \times (V_S - 5)}{(S \div I_{IN})} \quad (8)$$

where

- V_S is the operational supply voltage.
- S is the device sensitivity.

7.1.5 Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) quantifies the effective input current error due to a varying voltage on the isolated input of the device. Due to magnetic coupling and galvanic isolation of the current signal, the TMCS1100-Q1 has very high rejection of input common-mode voltage. Percent error contribution from input common-mode variation can be calculated by Equation 9.

$$e_{CMRR}\left(\%\right) = \frac{CMRR \times V_{CM}}{I_{IN}} \quad (9)$$

where

- V_{CM} is the maximum operational AC or DC voltage on the input of the device.

7.1.6 Reference Voltage Rejection Ratio

The voltage applied to the VREF pin sets the zero current output voltage for the TMCS1100-Q1. Ideally, the zero current output voltage directly tracks V_{REF}. Light internal mismatch can cause minor errors. When the reference voltage deviates from half of the supply, an additional effective output offset error is introduced into the device transfer function. The reference voltage rejection ratio (RVRR) is the effective change in output offset voltage due to this deviation. Error due to reference rejection can be calculated by Equation 10.

$$e_{V_{REF}}\left(\%\right) = \left| \frac{RVRR \times \left(V_{REF} - \frac{V_S}{2}\right)}{\frac{S}{I_{IN}}} \right| \quad (10)$$

7.1.7 External Magnetic Field Errors

The TMCS1100-Q1 does not have stray field-rejection capabilities, so external magnetic fields from adjacent high-current traces or nearby magnets can impact the output measurement. The total sensitivity (S) of the device is comprised of the initial transformation of input current to magnetic field quantified as the magnetic coupling factor (G), as well as the sensitivity of the Hall element and the analog circuitry that is factory calibrated to provide a final sensitivity. The output voltage is proportional to the input current by the device sensitivity, as defined in Equation 11.

$$S = G \times S_{Hall} \times A_V \tag{11}$$

where

- S is the TMCS1100-Q1 sensitivity in mV/A.
- G is the magnetic coupling factor in mT/A.
- S_{Hall} is the sensitivity of the Hall plate in mV/mT.
- A_V is the calibrated analog circuitry gain in V/V.

An external field, B_{EXT}, is measured by the Hall sensor and signal chain, in addition to the field generated by the leadframe current, and is added as an extra input term in the total output voltage function:

$$V_{OUT} = B_{EXT} \times S_{Hall} \times A_V + I_{IN} \times G \times S_{Hall} \times A_V \times V_{OUT,\,0A} \tag{12}$$

Observable from Equation 12 is that the impact of an external field is an additional equivalent input current signal, I_{BEXT}, shown in Equation 13. This effective additional input current has no dependence on Hall or analog circuitry sensitivity, so all gain variants have equivalent input-referred current error due to external magnetic fields.

$$I_{B_{EXT}} = \frac{B_{EXT}}{G} \tag{13}$$

This additional current error generates a percentage error defined by Equation 14.

$$e_{B_{EXT}}(\%) = \frac{\left|\frac{B_{EXT}}{G}\right|}{I_{IN}} \tag{14}$$

7.2 Transient Response Parameters

The transient response of the TMCS1100-Q1 is impacted by the 250kHz sampling rate as defined in *Transient Response*. Figure 7-2 shows the TMCS1100-Q1 response to an input current step sufficient to generate a 1V output change. The typical 4µs sampling window can be observed as a periodic step. This sampling window dominates the response of the device, and the response has some probabilistic nature due to alignment of the input step and the sampling window interval.

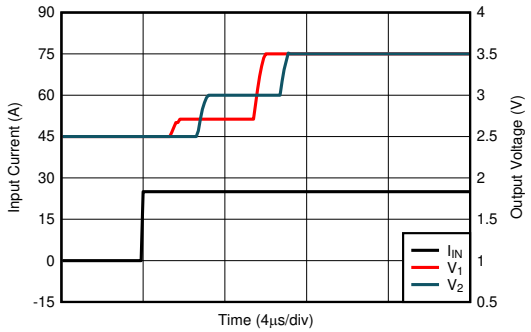


Figure 7-2. Transient Step Response

7.2.1 Slew Rate

Slew rate (SR) is defined as the V_{OUT} rate of change for a single integration step output transition, as shown in Figure 7-3. Because the device often requires two sampling windows to reach a full 90% settling of the final value, this slew rate is not equal to the 10%-90% transition time for the full output swing.

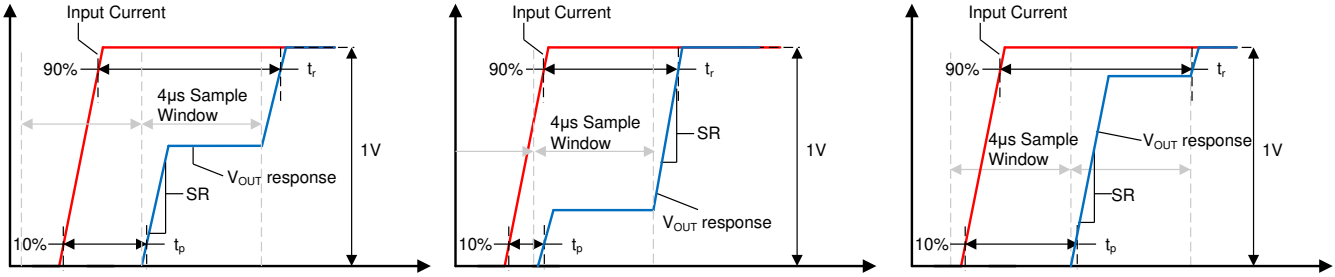


Figure 7-3. Small Current Input Step Transient Response

7.2.2 Propagation Delay and Response Time

Propagation delay is the time period between the input current waveform reaching 10% of the final value and V_{OUT} reaching 10% of the final value. This propagation delay is heavily dependent upon the alignment of the input current step and the sampling period of the TMCS1100-Q1, as shown for several different sampling window cases in Figure 7-3.

Response time is the time period between the input current reaching 90% of the final value and the output reaching 90% of the final value, for an input current step sufficient to cause a 1V transition on the output. Figure 7-3 shows the response time of the TMCS1100-Q1 under three different time cases. Unless a step input occurs directly during the beginning of one sampling window the response time includes two sampling intervals.

7.2.3 Current Overload Parameters

Current overload response parameters are the transient behavior of the TMCS1100-Q1 to an input current step consistent with a short circuit or fault event. Tested amplitude is twice the full scale range of the device, or 10V / Sensitivity in V/A. Under these conditions, the TMCS1100-Q1 output responds faster than in the case of a small input current step due to the higher input amplitude signal. Response time and propagation delay are measured in a similar manner to the case of a small input current step, as shown in Figure 7-4.

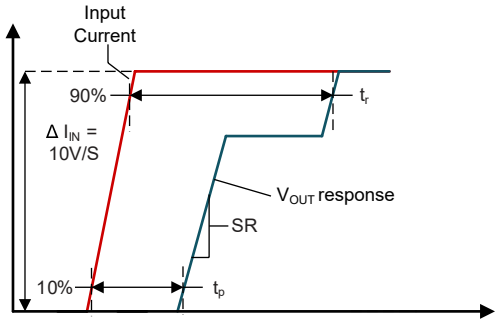


Figure 7-4. Current Overload Transient Response

Current overload recovery time is the required time for the device output to exit a saturated condition and return to normal operation. The transient response of the device during this recovery period from a current overload is shown in Figure 6-19.

7.2.4 CMTI, Common-Mode Transient Immunity

CMTI is the capability of the device to tolerate a rising/falling voltage step on the input without disturbance on the output signal. The device is specified for the maximum common-mode transition rate under which the output

signal does not experience a greater than 200mV disturbance that lasts longer than 1µs. Higher edge rates than the specified CMTI can be supported with sufficient filtering or blanking time after common-mode transitions.

7.3 Safe Operating Area

The isolated input current safe operating area (SOA) of the TMCS1100-Q1 is constrained by self-heating due to power dissipation in the input conductor. Depending upon the use case, the SOA is constrained by multiple conditions, including exceeding maximum junction temperature, Joule heating in the leadframe, or leadframe fusing under extremely high currents. These mechanisms depend on pulse duration, amplitude, and device thermal states.

Current SOA strongly depends on the thermal environment and design of the system-level board. Multiple thermal variables control the transfer of heat from the device to the surrounding environment, including air flow, ambient temperature, and printed-circuit board (PCB) construction and design. All ratings are for a single TMCS1100-Q1 device on the TMCS1100EVM, with no air flow in the specified ambient temperature conditions. Device use profiles must satisfy both continuous conduction and short-duration transient SOA capabilities for the thermal environment under which the system is operated.

7.3.1 Continuous DC or Sinusoidal AC Current

The longest thermal time constants of device packaging and PCBs are in the order of seconds; therefore, any continuous DC or sinusoidal AC periodic waveform with a frequency higher than 1Hz can be evaluated based on the RMS continuous-current level. The continuous-current capability has a strong dependence upon the operating ambient temperature range expected in operation. Figure 7-5 shows the maximum continuous current-handling capability of the device on the TMCS1100EVM. Current capability falls off at higher ambient temperatures because of the reduced thermal transfer from junction-to-ambient and increased power dissipation in the leadframe. By improving the thermal design of an application, the SOA can be extended to higher currents at elevated temperatures. Using larger and heavier copper power planes, providing air flow over the board, or adding heat sinking structures to the area of the device can all improve thermal performance.

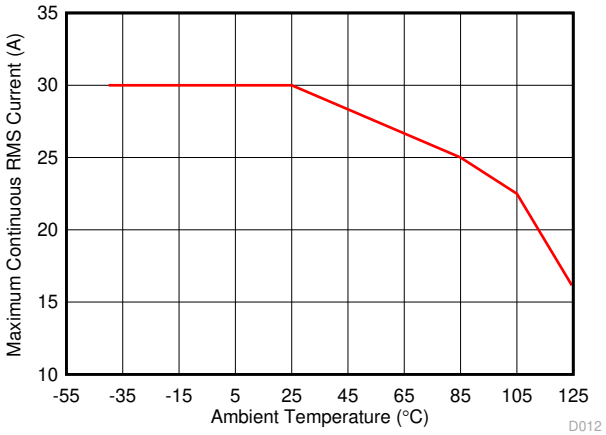


Figure 7-5. Maximum Continuous RMS Current vs Ambient Temperature

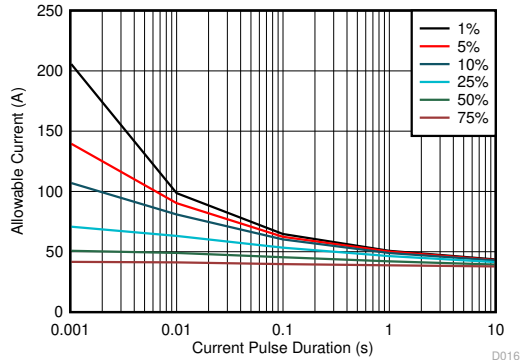
7.3.2 Repetitive Pulsed Current SOA

For applications where current is pulsed between a high current and no current, the allowable capabilities are limited by short-duration heating in the leadframe. The TMCS1100-Q1 can tolerate higher current ranges under some conditions, however, for repetitive pulsed events, the current levels must satisfy both the pulsed current SOA and the RMS continuous current constraint. Pulse duration, duty cycle, and ambient temperate all impact the SOA for repetitive pulsed events. Figure 7-6, Figure 7-7, Figure 7-8, and Figure 7-9 illustrate repetitive stress levels based on test results from the TMCS1100EVM under which parametric performance and isolation integrity is not impacted post-stress for multiple ambient temperatures. At high duty cycles or long pulse durations, this limit approaches the continuous current SOA for a RMS value defined by Equation 15.

$$I_{IN,\ RMS} = I_{IN,P} \times \sqrt{D} \tag{15}$$

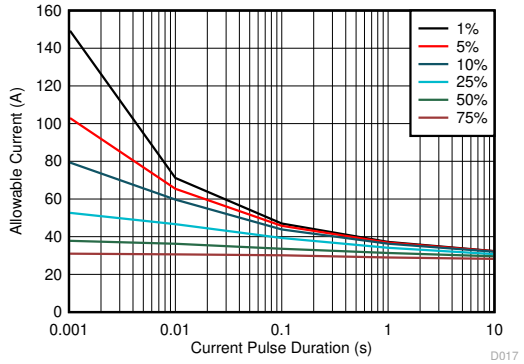
where

- $I_{IN,RMS}$ is the RMS input current level
- $I_{IN,P}$ is the pulse peak input current
- D is the pulse duty cycle



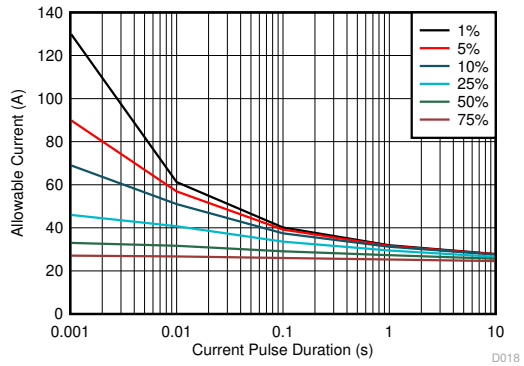
T_A = 25°C

Figure 7-6. Maximum Repetitive Pulsed Current vs. Pulse Duration



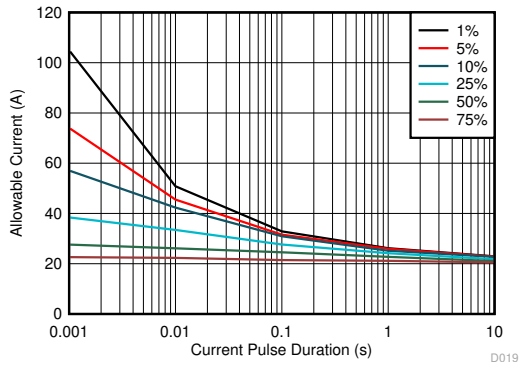
T_A = 85°C

Figure 7-7. Maximum Repetitive Pulsed Current vs. Pulse Duration



T_A = 105°C

Figure 7-8. Maximum Repetitive Pulsed Current vs. Pulse Duration



T_A = 125°C

Figure 7-9. Maximum Repetitive Pulsed Current vs. Pulse Duration

7.3.3 Single Event Current Capability

Single higher-current events that are shorter duration can be tolerated by the TMCS1100-Q1, because the junction temperature does not reach thermal equilibrium within the pulse duration. Figure 7-10 shows the short-circuit duration curve for the device for single current-pulse events, where the leadframe resistance changes after stress. This level is reached before a leadframe fusing event, but must be considered an upper limit for short duration SOA. For long-duration pulses, the current capability approaches the continuous RMS limit at the given ambient temperature.

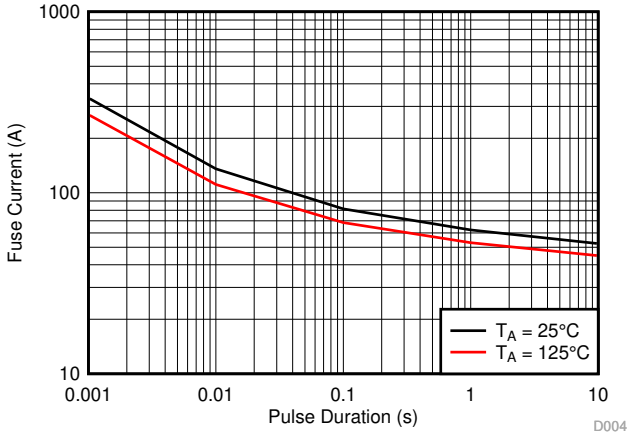


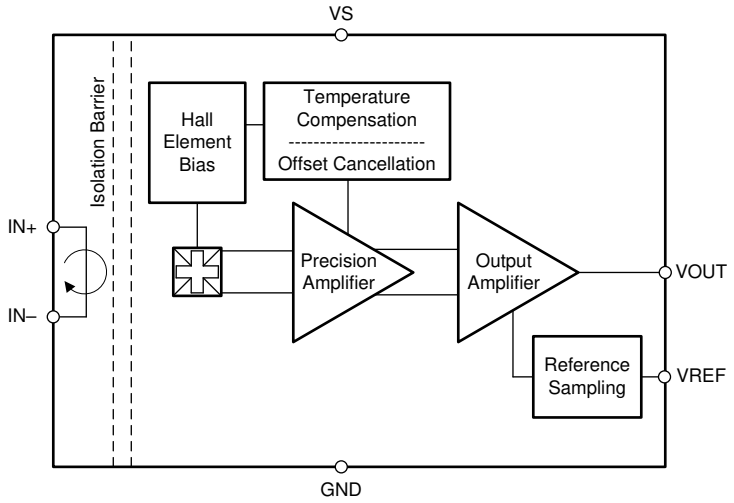
Figure 7-10. Single-Pulse Leadframe Capability

8 Detailed Description

8.1 Overview

The TMCS1100-Q1 is a precision Hall-effect current sensor, featuring a 600V basic isolation working voltage, < 1% full-scale error across temperature, and an external reference voltage enabling unidirectional or bidirectional current sensing Input current flows through a conductor between the isolated input current pins. The conductor has a 1.8mΩ resistance at room temperature for low power dissipation and a 20A RMS continuous current handling capability up to 105°C ambient temperature on the TMCS1100EVM. The low-ohmic leadframe path reduces power dissipation compared to alternative current measurement methodologies, and does not require any external passive components, isolated supplies, or control signals on the high-voltage side. The magnetic field generated by the input current is sensed by a Hall sensor and amplified by a precision signal chain. The device can be used for both AC and DC current measurements and has a bandwidth of 80kHz. There are multiple fixed-sensitivity device variants for a wide option of linear sensing ranges, and the TMCS1100-Q1 can operate with a low voltage supply from 3V to 5.5V. The TMCS1100-Q1 is optimized for high accuracy and temperature stability, with both offset and sensitivity compensated across the entire operating temperature range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Current Input

Input current to the TMCS1100-Q1 passes through the isolated side of the package leadframe through the IN+ and IN– pins. The current flow through the package generates a magnetic field that is proportional to the input current, and measured by a galvanically isolated, precision, Hall sensor IC. As a result of the electrostatic shielding on the Hall sensor die, only the magnetic field generated by the input current is measured, thus limiting input voltage switching pass-through to the circuitry. This configuration allows for direct measurement of currents with high-voltage transients without signal distortion on the current-sensor output. The leadframe conductor has a nominal resistance of 1.8mΩ at 25°C, and has a typical positive temperature coefficient as defined in the *Electrical Characteristics* table.

8.3.2 Input Isolation

The separation between the input conductor and the Hall sensor die due to the TMCS1100-Q1 construction provides inherent galvanic isolation between package pins 1-4 and pins 5-8. Insulation capability is defined according to certification agency definitions and using industry-standard test methods as defined in the *Insulation Specifications* table. Assessment of device lifetime working voltages follow the VDE 0884-11 standard for basic insulation, requiring time-dependent dielectric breakdown (TDDB) data-projection failure rates of less than 1000 part per million (ppm), and a minimum insulation lifetime of 20 years. The VDE standard also requires an

additional safety margin of 20% for working voltage, and a 30% margin for insulation lifetime, translating into a minimum required lifetime of 26 years at 509 V_{RMS} for the TMCS1100-Q1.

Figure 8-1 shows the intrinsic capability of the isolation barrier to withstand high-voltage stress over the lifetime of the device. Based on the TDDB data, the intrinsic capability of these devices is 424 V_{RMS} with a lifetime of > 100 years. Other factors such as operating environment and pollution degree can further limit the working voltage of the component in an end system.

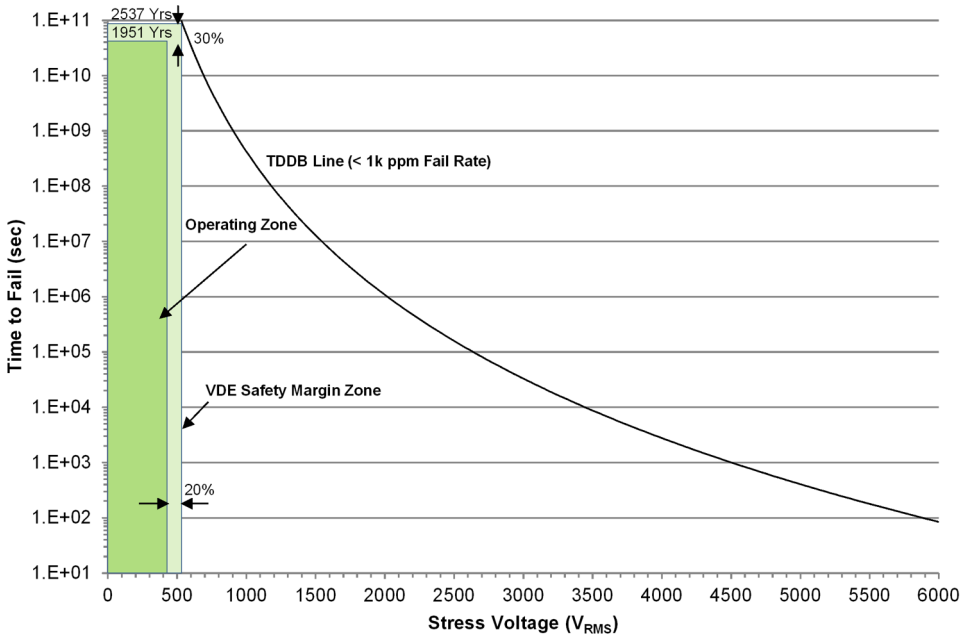


Figure 8-1. Insulation Lifetime

8.3.3 High-Precision Signal Chain

The TMCS1100-Q1 uses a precision, low-drift signal chain with proprietary sensor linearization techniques to provide a highly accurate and stable current measurement across the full temperature range of the device. The device is fully tested and calibrated at the factory to account for any variations in either silicon or packaging process variations. The full signal chain provides a fixed sensitivity voltage output that is proportional to the current through the leadframe of the isolated input.

8.3.3.1 Temperature Stability

The TMCS1100-Q1 includes a proprietary temperature compensation technique which results in significantly improved parametric drift across the full temperature range. This compensation technique accounts for changes in ambient temperature, self-heating, and package stress. A zero-drift signal chain architecture and Hall sensor temperature stabilization methods enable stable sensitivity and minimize offset errors across temperature, and drastically improves system-level performance across the required operating conditions.

Figure 8-2 shows the offset error across the full device ambient temperature range. Figure 8-3 shows the typical sensitivity. There are no other external components introducing errors sources; therefore, the high intrinsic accuracy and stability over temperature directly translates to system-level performance. As a result of this high precision, even a system with no calibration can reach < 1% of total error current-sensing capability.

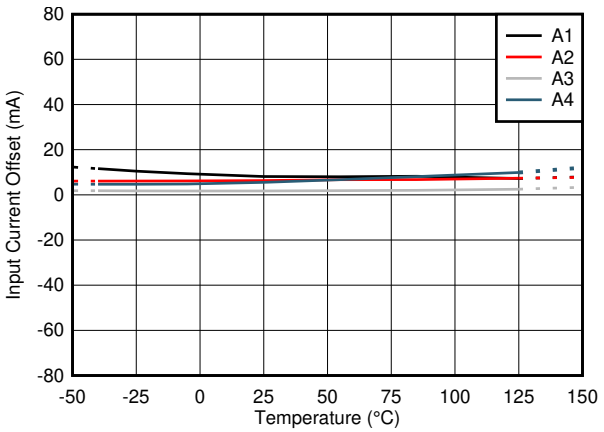


Figure 8-2. Offset Error Drift Across Temperature

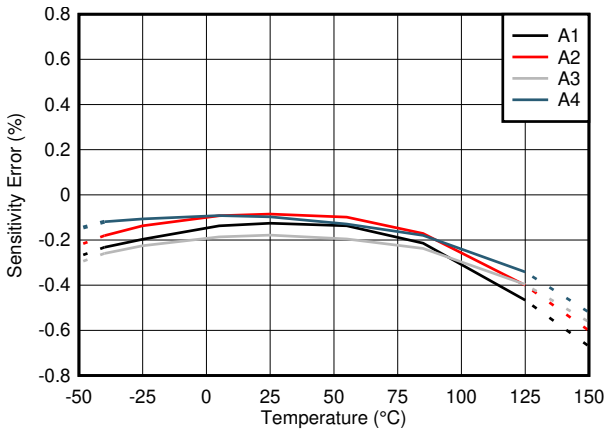


Figure 8-3. Sensitivity Drift Across Temperature

8.3.3.2 Lifetime and Environmental Stability

The same compensation techniques used in the TMCS1100-Q1 to reduce temperature drift also greatly reduce lifetime drift due to aging, stress, and environmental conditions. Typical magnetic sensors suffer from up to 2% to 3% of sensitivity drift due to aging at high operating temperatures. The TMCS1100-Q1 has greatly improved lifetime drift, as defined in the *Electrical Characteristics* for total sensitivity error measured after the worst case stress test during a three lot AEC-Q100 qualification. All other stress tests prescribed by an AEC-Q100 qualification caused lower than the specified sensitivity error, and are within the bounds specified within the *Electrical Characteristics* table. Figure 8-4 shows the total sensitivity error after the worst-case stress test, a Highly Accelerated Stress Test (HAST) at 130°C and 85% relative humidity (RH), while Figure 8-5 and Figure 8-6 show the sensitivity and offset error drift after a 1000 hour, 125°C high temperature operating life stress test as specified by AEC-Q100. This test mimics typical device lifetime operation, and shows the likely device performance variation due to aging is vastly improved compared to typical magnetic sensors.

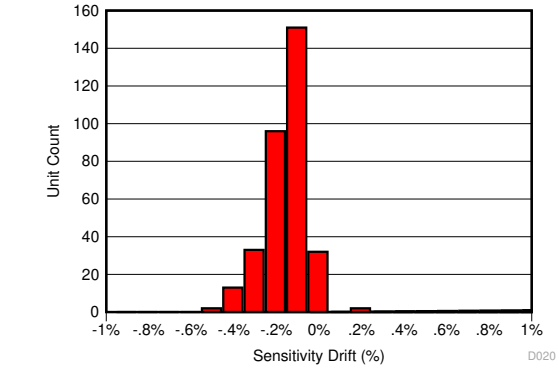


Figure 8-4. Sensitivity Error After 130°C, 85% RH HAST

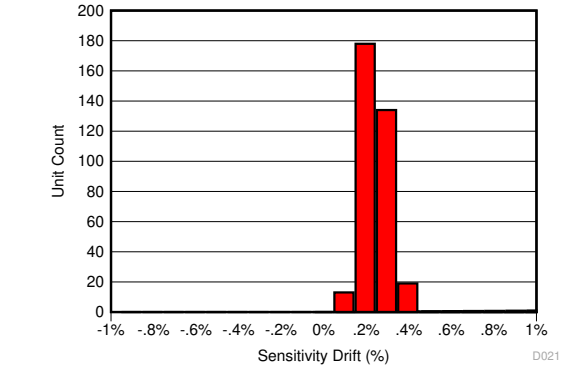


Figure 8-5. Sensitivity Error Drift After AEC-Q100 High Temperature Operating Life Stress Test

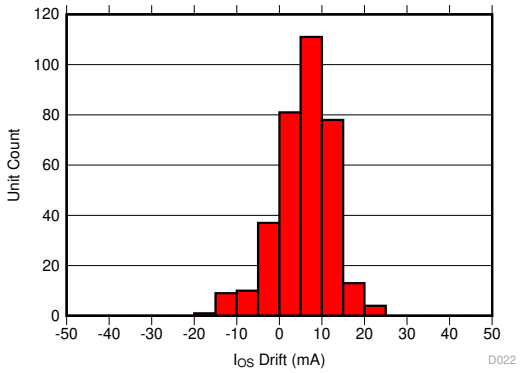


Figure 8-6. Input-Referred Offset Drift After AEC-Q100 High Temperature Operating Life Stress Test

8.3.3.3 Frequency Response

The TMCS1100-Q1 signal chain has a spectral response atypical of a linear analog system due to the discrete time sampling. The 250kHz sampling interval implies an effective Nyquist frequency of 125kHz, which limits spectral response to below this frequency. Higher frequency content than this frequency is aliased down to lower spectrums.

The TMCS1100-Q1 bandwidth is defined by the –3dB spectral response of the entire signal chain which is constrained by the sampling frequency. Normalized gain and phase plots across frequency are shown below in Figure 8-7 and Figure 8-8, all variants have the same bandwidth and phase response. Signal content beyond the 3dB bandwidth level still has significant fundamental frequency transmissions through the signal chain, but at increasing distortion levels

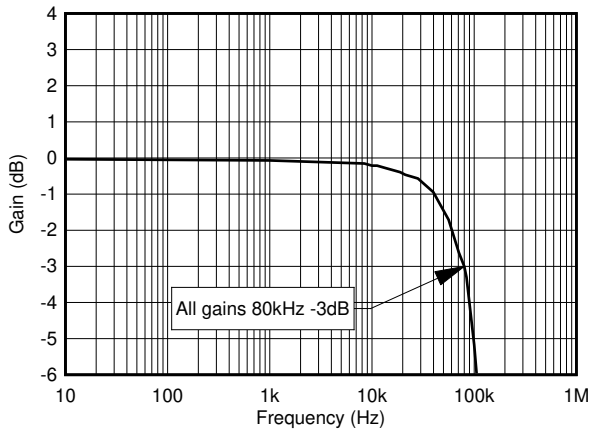


Figure 8-7. Normalized Gain, All Variants

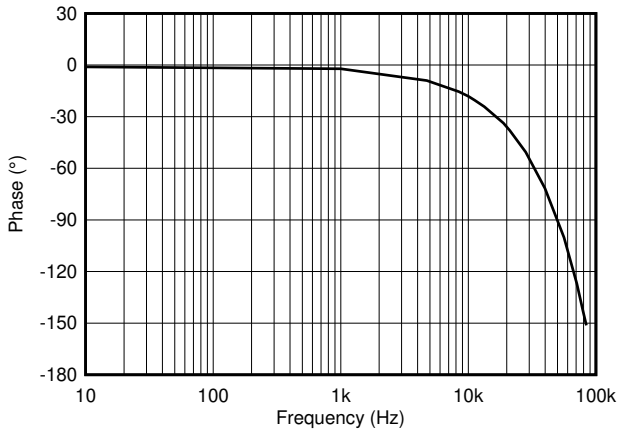


Figure 8-8. Normalized Phase, All Variants

8.3.3.4 Transient Response

The TMCS1100-Q1 signal chain includes a precision analog front end followed by a sampled integrator. At the end of each integration cycle, the signal propagates to the output. Depending on the alignment of a change in input current relative to the sampling window, the output does not always settle to the final signal until the second integration cycle. Figure 8-9 shows a typical output waveform response to a 10kHz sine wave input current. For a slowly varying input current signal, the output is a discrete time representation with a phase delay of the integration sampling window. Adding a first order filter of 100kHz effectively smooths the output waveform with minimal impact to phase response.

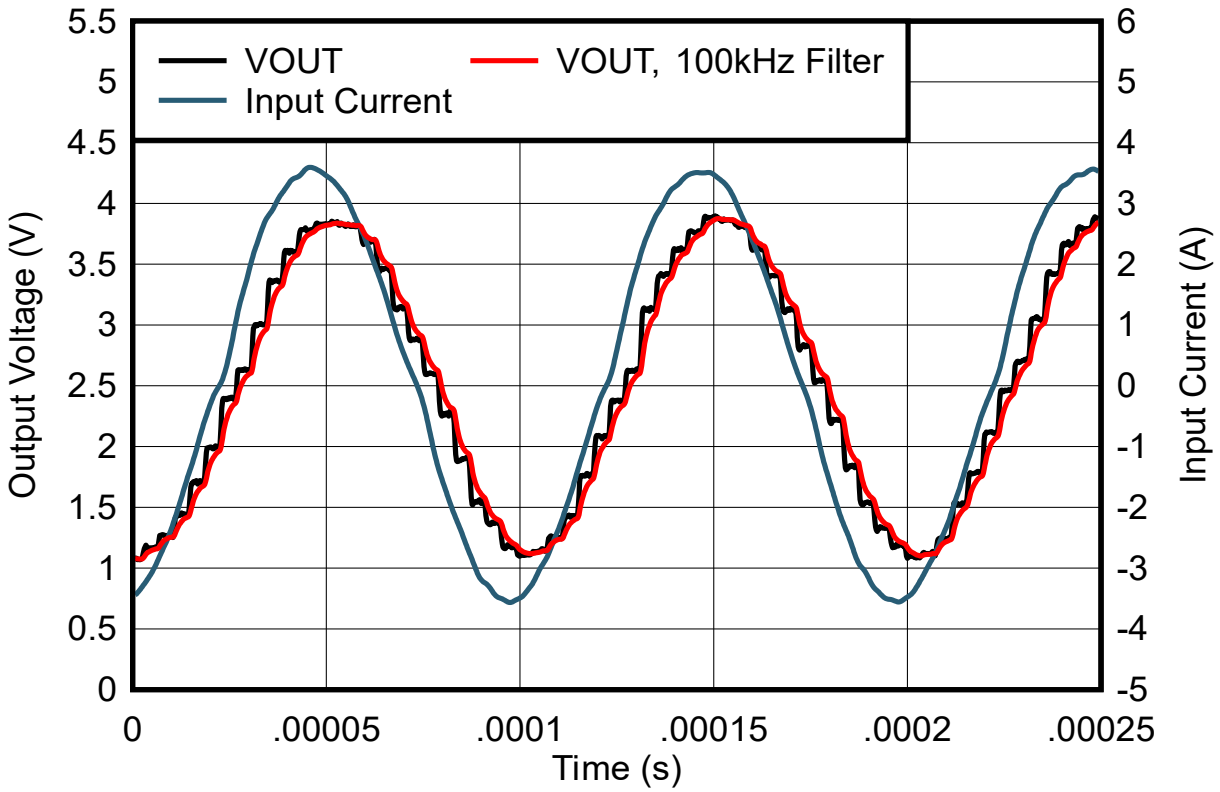


Figure 8-9. Response Behavior to 10kHz Sine Wave Input Current

Figure 8-10 shows two transient waveforms to an input-current step event, but occurring at different times during the sampling interval. In both cases, the full transition of the output takes two sampling intervals to reach the final output value. The timing of the current event relative to the sampling window determines the proportional amplitude of the first and second sampling intervals.

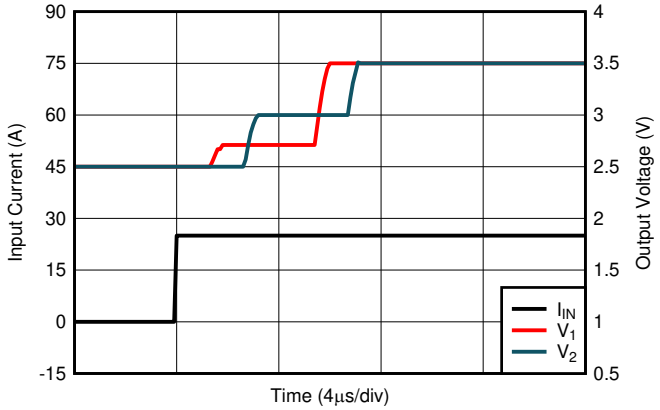


Figure 8-10. Transient Response to Input-Current Step Sufficient for 1V Output Swing

The output value is effectively an average over the sampling window; therefore, a large-enough current transient can drive the output voltage to near the full scale range in the first sample response. This condition is likely to be true in the case of a short-circuit or fault event. Figure 8-11 shows an input-current step twice the full scale measurable range with two output voltage responses illustrating the effect of the sampling window. The relative timing and size of the input current transition determines both the time and amplitude of the first output transition. In either case, the total response time is slightly longer than one integration period.

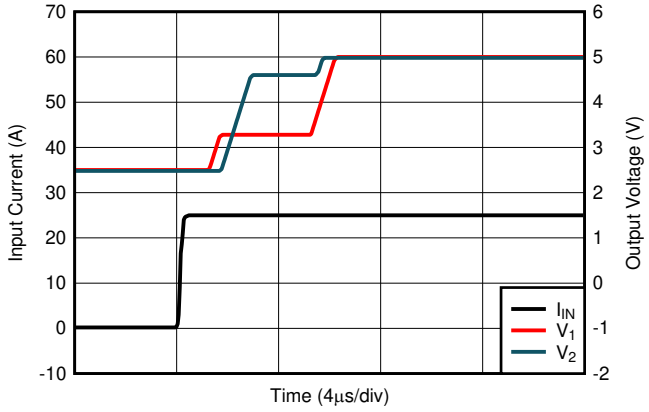


Figure 8-11. Transient Response to a Large Input Current Step

8.3.4 External Reference Voltage Input

The reference voltage provided externally to the TMCS1100-Q1 on the VREF pin determines the zero current output voltage, $V_{OUT,0A}$. This zero-current output level along with sensitivity determine the measurable input current range of the device, and allows for unidirectional or bidirectional sensing, as described in the *Absolute Maximum Ratings* table. Figure 8-12 illustrates the transfer function of the TMCS1100A2-Q1 with varying V_{REF} voltages of 0V, 1.25V, and 2.5V. By shifting the zero current output voltage of the device, the dynamic range of measurable input current can be modified.

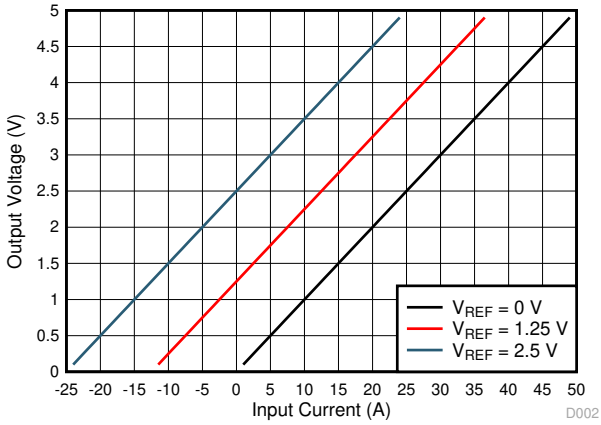


Figure 8-12. Output Voltage Relationship to Input Current With Varying VREF Voltages

The input voltage on this pin can be provided by any external voltage source or potential, such as a discrete precision reference, a voltage divider, ADC reference, or ground. The VREF pin is sampled by the internal circuitry at approximately 1MHz, then buffered and provided to the signal chain of the device. An apparent DC load of approximately 1µA is observed by the external reference. To prevent errors due to sampling settling, keep the source impedance below the level specified in the *Electrical Characteristics* table.

8.3.5 Current-Sensing Measurable Ranges

The TMCS1100-Q1 can be configured to allow for bidirectional or unidirectional measurable current ranges based on the external voltage on the VREF pin. The output voltage is limited by V_{OUT} swing to either supply or ground. Linear output swing range to both V_S and GND is calculated by equations Equation 16 and Equation 17.

$$V_{OUT,max} = V_S - Swing_{VS} \quad (16)$$

$$V_{OUT,min} = Swing_{GND} \quad (17)$$

Rearranging the transfer function of the device to solve for input current, and substituting $V_{OUT,max}$ and $V_{OUT,min}$ yields the maximum and minimum measurable input current ranges as shown in Equation 18 and Equation 19.

$$I_{IN,MAX+} = (V_{OUT,max} – V_{REF}) / S \quad (18)$$

$$I_{IN,MAX-} = (V_{REF} – V_{OUT,min}) / S \quad (19)$$

where

- $I_{IN,MAX+}$ is the maximum linear measurable positive input current.
- $I_{IN,MAX-}$ is the maximum linear measurable negative input current.
- S is the sensitivity of the device variant.

Setting V_{REF} to the middle of the output swing range provides bidirectional measurement capability, whereas setting V_{REF} close to the ground provides a unidirectional measurement. Custom ranges with nonuniform positive and negative input current ranges can be achieved by appropriately scaling the V_{REF} potential relative to the full output voltage range.

8.4 Device Functional Modes

8.4.1 Power-Down Behavior

As a result of the inherent galvanic isolation of the device, very little consideration must be paid to powering down the device, as long as the limits in the *Absolute Maximum Ratings* table are not exceeded on any pins. The isolated current input and the low-voltage signal chain can be decoupled in operational behavior, as either can be energized with the other shut down, as long as the isolation barrier capabilities are not exceeded. The low-voltage power supply can be powered down while the isolated input is still connected to an active high-voltage signal or system.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The key feature sets of the TMCS1100-Q1 provide significant advantages in any application where an isolated current measurement is required.

- Galvanic isolation provides a high isolated working voltage and excellent immunity to input voltage transients.
- Hall based measurement simplifies system level design without the need for a power supply on the high voltage (HV) side.
- An input current path through the low impedance conductor minimizes power dissipation.
- Excellent accuracy and low temperature drift eliminate the need for multipoint calibrations without sacrificing system performance.
- An external reference input maximizes flexibility for unidirectional or bidirectional measurement with custom dynamic ranges, and improves accuracy at the system level.
- A wide operating supply range enables a single device to function across a wide range of voltage levels.

These advantages increase system-level performance while minimizing complexity for any application where precision current measurements must be made on isolated currents. Specific examples and design requirements are detailed in the following section.

9.1.1 Total Error Calculation Examples

Total error can be calculated for any arbitrary device condition and current level. Error sources considered must include input-referred offset current, power-supply rejection, input common-mode rejection, sensitivity error, nonlinearity, V_{REF} to V_{OUT} gain error, and the error caused by any external fields. Compare each of these error sources in percentage terms, as some are significant drivers of error and some have inconsequential impact to current error. Offset (Equation 20), CMRR (Equation 22), PSRR (Equation 21), VREF gain error (Equation 23), and external field error (Equation 24) are all referred to the input, and so, are divided by the actual input current I_{IN} to calculate percentage errors. For calculations of sensitivity error and nonlinearity error, the percentage limits explicitly specified in the *Electrical Characteristics* table can be used.

$$e_{I_{OS}}(\%) = \frac{I_{OS}}{I_{IN}} \tag{20}$$

$$e_{PSRR}(\%) = \left| \frac{\frac{PSRR * (V_S - 5)}{S}}{I_{IN}} \right| \tag{21}$$

$$e_{CMRR}(\%) = \left| \frac{CMRR * V_{CM}}{I_{IN}} \right| \tag{22}$$

$$e_{V_{REF}}(\%) = \frac{\left| \frac{RVRR * (V_{REF} - \frac{V_S}{2})}{S} \right|}{I_{IN}} \tag{23}$$

$$e_{B_{EXT}}(\%) = \frac{\left|\frac{B_{EXT}}{G}\right|}{I_{IN}} \quad (24)$$

When calculating error contributions across temperature, only the input offset current and sensitivity error contributions vary significantly. For determining offset error over a given temperature range (ΔT), use Equation 25 to calculate total offset error current. Sensitivity error is specified for both –40°C to 85°C and –40°C to 125°C. The appropriate specification must be used based on application operating ambient temperature range.

$$e_{I_{OS},\Delta T}(\%) = \frac{I_{OS,25°C} + I_{OS,drift}\left(\frac{\mu A}{°C}\right) \times \Delta T}{I_{IN}} \quad (25)$$

To accurately calculate the total expected error of the device, the contributions from each of the individual components above must be understood in reference to operating conditions. To account for the individual error sources that are statistically uncorrelated, a root sum square (RSS) error calculation must be used to calculate total error. For the TMCS1100-Q1, only the input referred offset current (I_{OS}), CMRR, and PSRR are statistically correlated. These error terms are lumped in an RSS calculation to reflect this nature, as shown in Equation 26 for room temperature and Equation 27 for across a given temperature range. The same methodology can be applied for calculating typical total error by using the appropriate error term specification.

$$e_{RSS}(\%) = \sqrt{\left(e_{I_{OS}} + e_{PSRR} + e_{CMRR}\right)^2 + e_{V_{REF}}{}^2 + e_{B_{EXT}}{}^2 + e_S{}^2 + e_{NL}{}^2} \quad (26)$$

$$e_{RSS,\Delta T}(\%) = \sqrt{\left(e_{I_{OS,\Delta T}} + e_{PSRR} + e_{CMRR}\right)^2 + e_{V_{REF}}{}^2 + e_{B_{EXT}}{}^2 + e_{S,\Delta T}{}^2 + e_{NL}{}^2} \quad (27)$$

The total error calculation has a strong dependence on the actual input current; therefore, always calculate total error across the dynamic range that is required. These curves asymptotically approach the sensitivity and nonlinearity error at high current levels, and approach infinity at low current levels due to offset error terms with input current in the denominator. Key figures of merit for any current-measurement system include the total error percentage at full-scale current, as well as the dynamic range of input current over which the error remains below some key level. Figure 9-1 illustrates the RSS maximum total error as a function of input current for a TMCS1100A2 at room temperature and across the full temperature range with V_S of 5V.

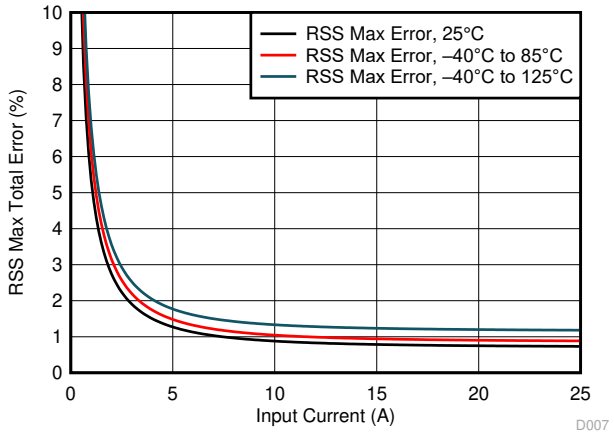


Figure 9-1. RSS Error vs. Input Current

9.1.1.1 Room Temperature Error Calculations

For room-temperature total-error calculations, specifications across temperature and drift are ignored. As an example, consider a TMCS1100-Q1 A1 with a supply voltage (V_S) of 3.3V, a V_{REF} of 1.5V, and a worst-case common-mode excursion of 600V to calculate operating-point-specific parameters. Consider a measurement error due to an external magnetic field of 30µT, roughly the magnetic field strength of the Earth. The full-scale current range of the device in specified conditions is slightly greater than 28A; therefore, calculate error at both 25A and 12.5A to highlight error dependence on the input-current level. Table 9-1 shows the individual error components and RSS maximum total error calculations at room temperature under the conditions specified. Relative to other errors, the additional error from CMRR is negligible, and can typically be ignored for total error calculations.

Table 9-1. Total Error Calculation: Room Temperature Example

ERROR COMPONENT	SYMBOL	EQUATION	% MAX TOTAL ERROR AT I_{IN} = 25A	% MAX TOTAL ERROR AT I_{IN} = 12.5A
Input offset error	e_{Ios}	$e_{I_{OS}}(\%) = \frac{I_{OS}}{I_{IN}}$	0.24%	0.48%
PSRR error	e_{PSRR}	$e_{PSRR}(\%) = \left\lvert \frac{\frac{PSRR * (V_S - 5)}{S}}{I_{IN}} \right\rvert$	0.27%	0.54%
CMRR error	e_{CMRR}	$e_{CMRR}(\%) = \left\lvert \frac{CMRR * V_{CM}}{I_{IN}} \right\rvert$	0.01%	0.02%
V_{REF} error	e_{VREF}	$e_{V_{REF}}(\%) = \frac{\left\lvert \frac{RVRR * (V_{REF} - \frac{V_S}{2})}{S} \right\rvert}{I_{IN}}$	0.04%	0.08%
External Field error	e_{Bext}	$e_{B_{EXT}}(\%) = \frac{\left\lvert \frac{B_{EXT}}{G} \right\rvert}{I_{IN}}$	0.11%	0.22%
Sensitivity error	e_S	Specified in *Electrical Characteristics*	0.7%	0.7%
Nonlinearity error	e_{NL}	Specified in *Electrical Characteristics*	0.05%	0.05%
RSS total error	e_{RSS}	$e_{RSS}(\%) = \sqrt{\left(e_{I_{OS}} + e_{PSRR} + e_{CMRR}\right)^2 + e_{V_{REF}}^2 + e_{B_{EXT}}^2 + e_S^2 + e_{NL}^2}$	0.88%	1.28%

9.1.1.2 Full Temperature Range Error Calculations

To calculate total error across any specific temperature range, Equation 26 and Equation 27 must be used for RSS maximum total errors, similar to the example for room temperatures. Conditions from the example in *Room Temperature Error Calculations* have been replaced with the respective equations and error components for a –40°C to 85°C temperature range below in Table 9-2.

Table 9-2. Total Error Calculation: –40°C to 85°C Example

ERROR COMPONENT	SYMBOL	EQUATION	% MAX TOTAL ERROR AT I_{IN} = 25A	% MAX TOTAL ERROR AT I_{IN} = 12.5A
Input offset error	$e_{Ios,\Delta T}$	$e_{I_{OS},\Delta T}(\%) = \frac{I_{OS,25°C} + I_{OS,drift}\left(\frac{\mu A}{°C}\right) \times \Delta T}{I_{IN}}$	0.28%	0.56%

Table 9-2. Total Error Calculation: –40°C to 85°C Example (continued)

ERROR COMPONENT	SYMBOL	EQUATION	% MAX TOTAL ERROR AT I_{IN} = 25A	% MAX TOTAL ERROR AT I_{IN} = 12.5A
PSRR error	e_{PSRR}	$e_{PSRR}(\%) = \left\lvert \frac{\frac{PSRR * (V_S - 5)}{S}}{I_{IN}} \right\rvert$	0.27%	0.54%
CMRR error	e_{CMRR}	$e_{CMRR}(\%) = \left\lvert \frac{CMRR * V_{CM}}{I_{IN}} \right\rvert$	0.01%	0.02%
V_{REF} error	e_{VREF}	$e_{V_{REF}}(\%) = \frac{\left\lvert \frac{RVRR * (V_{REF} - \frac{V_S}{2})}{S} \right\rvert}{I_{IN}}$	0.04%	0.08%
External Field error	e_{Bext}	$e_{B_{EXT}}(\%) = \frac{\left\lvert \frac{B_{EXT}}{G} \right\rvert}{I_{IN}}$	0.11%	0.22%
Sensitivity error	$e_{S,\Delta T}$	Specified in *Electrical Characteristics*	0.85%	0.85%
Nonlinearity error	e_{NL}	Specified in *Electrical Characteristics*	0.05%	0.05%
RSS total error	$e_{RSS,\Delta T}$	$e_{RSS,\Delta T}(\%) = \sqrt{\left(e_{IOS,\Delta T} + e_{PSRR} + e_{CMRR}\right)^2 + e_{V_{REF}}^2 + e_{B_{EXT}}^2 + e_{S,\Delta T}^2 + e_{NL}^2}$	1.03%	1.43%

9.2 Typical Application

Inline sensing of inductive load currents, such as motor phases, provides significant benefits to the performance of a control systems, allowing advanced control algorithms and diagnostics with minimal post-processing. A primary challenge to inline sensing is that the current sensor is subjected to full HV supply-level PWM transients driving the load. The inherent isolation of an in-package Hall-effect current sensor topology helps overcome this challenge, providing high common-mode immunity, as well as isolation between the high-voltage motor drive levels and the low-voltage control circuitry. Figure 9-2 illustrates the use of the TMCS1100-Q1 in such an application, driving the inductive load presented by a three phase motor.

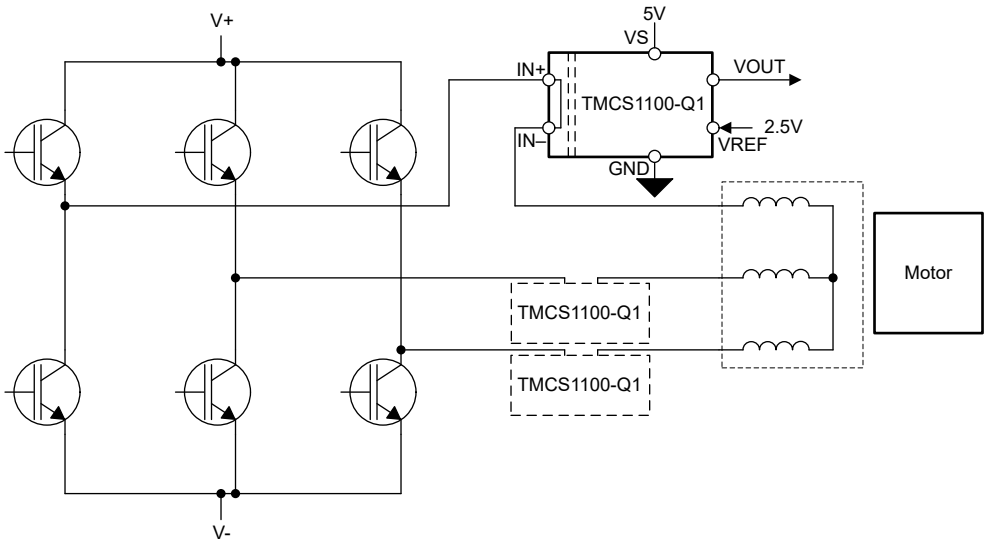


Figure 9-2. Inline Motor Phase Current Sensing

9.2.1 Design Requirements

For current sensing of a three-phase motor application, make sure to provide linear sensing across the expected current range, and make sure that the device remains within working thermal constraints. A single TMCS1100-Q1 for each phase can be used, or two phases can be measured, and the third phase calculated on the motor-controller host processor. For this example, consider a nominal supply of 5V but a minimum of 4.9V to include for some supply variation. Maximum output swings are defined according to TMCS1100-Q1 specifications, and a full-scale current measurement of ±20 A is required.

Table 9-3. Example Application Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
$V_{S,nom}$	5V
$V_{S,min}$	4.9V
$I_{IN,FS}$	±20A

9.2.2 Detailed Design Procedure

The TMCS1100-Q1 application design procedure has two key design parameters: the sensitivity version chosen (A1-A4) and the reference voltage input. Further consideration of noise and integration with an ADC can be explored, but is beyond the scope of this application design example. The TMCS1100-Q1 transfer function is effectively a transimpedance with a variable offset set by V_{REF}, defined by Equation 28.

$$V_{OUT} = I_{IN} \times S + V_{REF} \tag{28}$$

Design of the sensing device first focuses on maximizing the sensitivity while maintaining linear measurement over the expected current input range. The linear output voltage range is constrained by the TMCS1100-Q1 linear swing to ground, $Swing_{GND}$, and swing to supply, $Swing_{VS}$. With the previous parameters, the maximum linear output voltage range is the range between $V_{OUT,max}$ and $V_{OUT,min}$, as defined by Equation 29 and Equation 30.

$$V_{OUT,max} = V_{S,min} - Swing_{V_S} \tag{29}$$

$$V_{OUT,min} = Swing_{GND} \tag{30}$$

For a bidirectional current-sensing application, a sufficient linear output voltage range is required from V_{REF} to both ground and the power supply. Design parameters for this example application are shown in Table 9-4 along with the calculated output range.

Table 9-4. Example Application Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$Swing_{VS}$	0.2V
$Swing_{GND}$	0.05V
$V_{OUT,max}$	4.7V
$V_{OUT,min}$	0.05V
$V_{OUT,max}$ - $V_{OUT,min}$	4.65V

These design parameters result in a maximum linear output voltage swing of 4.65V. To determine which sensitivity variant of the TMCS1100-Q1 most fully uses this linear range, calculate the maximum current range by Equation 31 for a unidirectional current ($I_{U,MAX}$), and Equation 32 for a bidirectional current ($I_{B,MAX}$).

$$I_{U,MAX} = \frac{V_{OUT,max} - V_{OUT,min}}{S_{A<x>}} \tag{31}$$

$$I_{B,MAX} = \frac{V_{OUT,max} - V_{OUT,min}}{2 \times S_{A<x>}} \tag{32}$$

where

- $S_{A<x>}$ is the sensitivity of the relevant A1-A4 variant.

Table 9-5 shows such calculation for each gain variant of the TMCS1100-Q1 with the appropriate sensitivities.

Table 9-5. Maximum Full-Scale Current Ranges With 4.65V Output Range

SENSITIVITY VARIANT	SENSITIVITY	$I_{U,MAX}$	$I_{B,MAX}$
TMCS1100A1-Q1	50mV/A	93A	±46.5A
TMCS1100A2-Q1	100mV/A	46.5A	±23.2A
TMCS1100A3-Q1	200mV/A	23.2A	±11.6A
TMCS1100A4-Q1	400mV/A	11.6A	±5.8A

In general, select the highest sensitivity variant that provides for the desired full-scale current range. For the design parameters in this example, the TMCS1100A2-Q1 with a sensitivity of 0.1V/A is the proper selection because the maximum-calculated ±23.2A linear measurable range is sufficient for the desired ±20A full-scale current.

After selecting the appropriate sensitivity variant for the application, the zero-current reference voltage defined by the V_{REF} input pin is defined. Manipulating Equation 28 and using the linear range defined by $V_{OUT,max}$, $V_{OUT,min}$, and the full-scale input current, $I_{IN,FS}$, calculate the maximum and minimum V_{REF} voltages allowed to remain within the linear measurement range, shown in Equation 33 and Equation 34.

$$V_{REF,max} = V_{OUT,max} - \left|I_{IN,FS}\right| \times S \tag{33}$$

$$V_{REF,min} = V_{OUT,min} + \left|I_{IN,FS}\right| \times S \tag{34}$$

Any value of V_{REF} can be chosen between $V_{REF,max}$ and $V_{REF,min}$ to maintain the required linear sensing range. If the allowable V_{REF} range is not wide enough or does not include a desired V_{REF} voltage, the analysis must be repeated with a lower sensitivity variant of the TMCS1100-Q1. Equation 28 can be manipulated to solve for the maximum allowable current in either direction by using the selected V_{REF} voltage and the maximum linear voltage ranges as in Equation 35 and Equation 36.

$$I_{MAX+} = \frac{V_{OUT,max} - V_{REF}}{S} \tag{35}$$

$$I_{MAX-} = \frac{V_{OUT,min} - V_{REF}}{S} \tag{36}$$

Table 9-6 shows the respective values for the example design parameters in Table 9-4. In this case, a V_{REF} of 2.5V has been selected such that the zero current output is half of the nominal power supply. This example V_{REF} design value provides a linear input current-sensing range of –24.5A to +22A, with the positive current defined as current flowing into the IN+ pin.

Table 9-6. Example VREF Limits and Associated Current Ranges

REFERENCE PARAMETER	EXAMPLE VALUE	MAXIMUM LINEAR CURRENT SENSING RANGE	
		I_{MAX+}	I_{MAX-}
$V_{REF,min}$	2.05V	26.5A	–20A
$V_{REF,max}$	2.7V	20A	–26.5A
Selected V_{REF}	2.5V	22A	–24.5A

After selecting a V_{REF} for the application design, an appropriate source must be defined. Multiple implementations are possible, but can include:

- Resistor divider from the supply voltage
- Resistor divider from an ADC full-scale reference
- Dedicated or preexisting voltage reference IC
- DAC or reference voltage from a system microcontroller

Each of these options has benefits, and the error terms, noise, simplicity, and cost of each implementation must be weighed. In the current design example, any of these options are potentially available as a 2.5V V_{REF} is midrail of the power supply, a common IC reference voltage, and can already be available in the system. If the primary consideration for the current application design is to maximize precision while minimizing temperature drift and noise, a dedicated voltage reference must be chosen. For this case, the LM4030C-2.5 can be chosen for to optimize system accuracy without significant cost addition. Figure 9-3 depicts the current-sense system design as discussed.

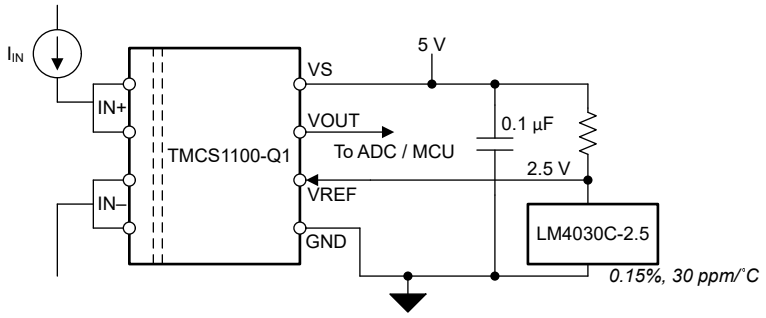


Figure 9-3. TMCS1100-Q1 Example Current-Sense System Design

9.3 Power Supply Recommendations

The TMCS1100-Q1 only requires a power supply (V_S) on the low-voltage isolated side, which powers the analog circuitry independent of the isolated current input. V_S determines the full-scale output range of the analog output V_{OUT}, and can be supplied with any voltage between 3V and 5.5V. To filter noise in the power-supply path, place a low-ESR decoupling capacitor of 0.1µF between V_S and GND pins as close as possible to the supply and ground pins of the device. To compensate for noisy or high-impedance power supplies, add more decoupling capacitance.

The TMCS1100-Q1 power supply V_S can be sequenced independently of current flowing through the input. However, there is a typical 25ms delay between V_S reaching the recommended operating voltage and the analog output being valid. Within this delay V_{OUT} transfers from a high impedance state to the active drive state, during which time the output voltage can transition between GND and V_S. If this behavior must be avoided, a stable supply voltage to V_S must be provided for longer than 25ms prior to applying input current.

9.4 Layout

9.4.1 Layout Guidelines

The TMCS1100-Q1 is specified for a continuous current handling capability on the TMCS1100EVM, which uses 3oz copper pour planes. This current capability is fundamentally limited by the maximum device junction temperature and the thermal environment, primarily the PCB layout and design. To maximize current-handling capability and thermal stability of the device, take care with PCB layout and construction to optimize the thermal capability. Efforts to improve the thermal performance beyond the design and construction of the TMCS1100EVM can result in increased continuous-current capability due to higher heat transfer to the ambient environment. Keys to improving thermal performance of the PCB include:

- Use large copper planes for both input current path and isolated power planes and signals.
- Use heavier copper PCB construction.
- Place thermal via *farms* around the isolated current input.

- Provide airflow across the surface of the PCB.

The TMCS1100-Q1 senses external magnetic fields, so make sure to minimize adjacent high-current traces in close proximity to the device. The input current trace can contribute additional magnetic field to the sensor if the input current traces are routed parallel to the vertical axis of the package. Figure 9-4 illustrates the most optimal input current routing into the TMCS1100-Q1. As the angle that the current approaches the device deviates from 0° to the horizontal axis, the current trace contributes some additional magnetic field to the sensor, increasing the effective sensitivity of the device. If current must be routed parallel to the package vertical axis, move the routing away from the package to minimize the impact to the sensitivity of the device. Terminate the input current path directly underneath the package lead footprint, and use a merged copper input trace for both the IN+ and IN– inputs.

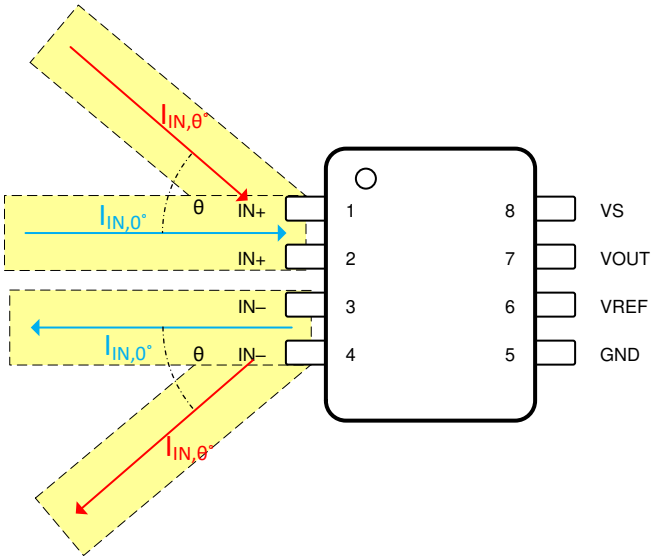


Figure 9-4. Magnetic Field Generated by Input Current Trace

In addition to thermal and magnetic optimization, make sure to consider the PCB design required creepage and clearance for system-level isolation requirements. Maintain required creepage between solder stencils, as shown in Figure 9-5, if possible. If not possible to maintain required PCB creepage between the two isolated sides at board level, add additional slots or grooves to the board. If more creepage and clearance is required for system isolation levels than is provided by the package, the entire device and solder mask can be encapsulated with an overmold compound to meet system-level requirements.

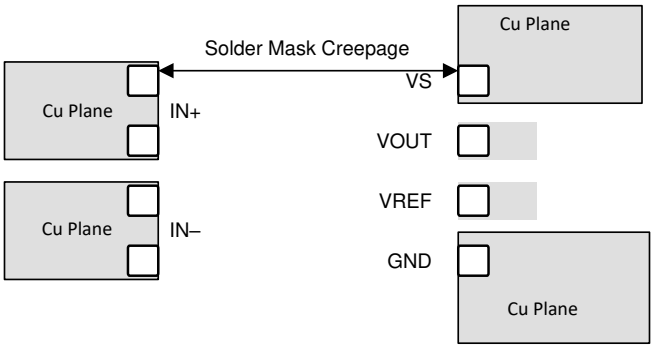


Figure 9-5. Layout for System Creepage Requirements

9.4.2 Layout Example

An example layout, shown in Figure 9-6, is from the TMCS1100EVM. Device performance is targeted for thermal and magnetic characteristics of this layout, which provides optimal current flow from the terminal connectors to the device input pins while large copper planes enhance thermal performance.

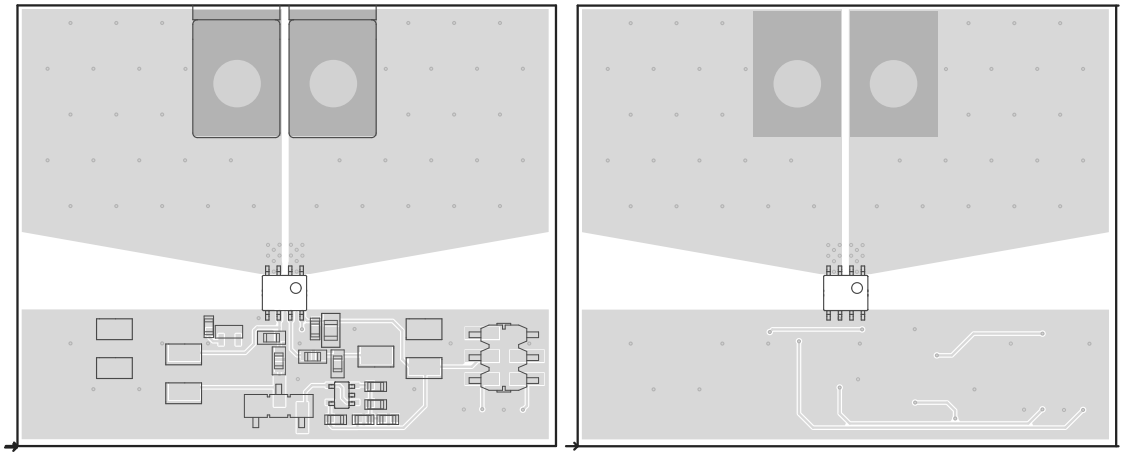


Figure 9-6. Recommended Board Top (Left) and Bottom (Right) Plane Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

For development tool support see the following:

- TMCS1100EVM
- TMCS1100 TI-TINA Model
- TMCS1100 TINA-TI Reference Design

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMCS1100EVM User's Guide*
- Texas Instruments, *Enabling Precision Current Sensing Designs with Nonratiometric Magnetic Current Sensors*
- Texas Instruments, *Low-Drift, Precision, In-Line Isolated Magnetic Motor Current Measurements*
- Texas Instruments, *Isolation Glossary*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2021) to Revision A (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *Startup Transient Response* graph X-axis from: Time (5µs/div) to: Time (5ms/div)	10

12 Mechanical, Packaging, and Orderable Information

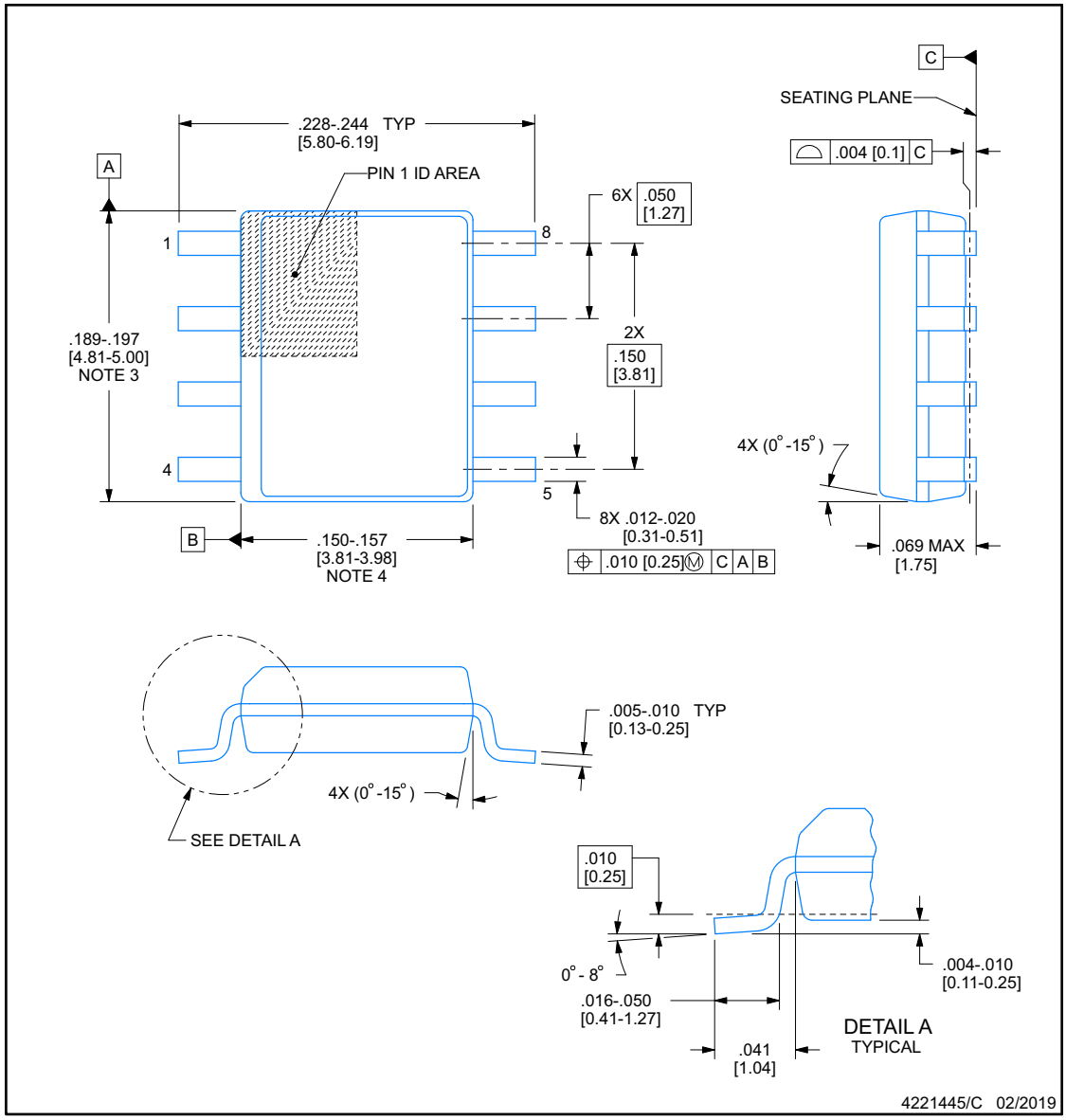
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

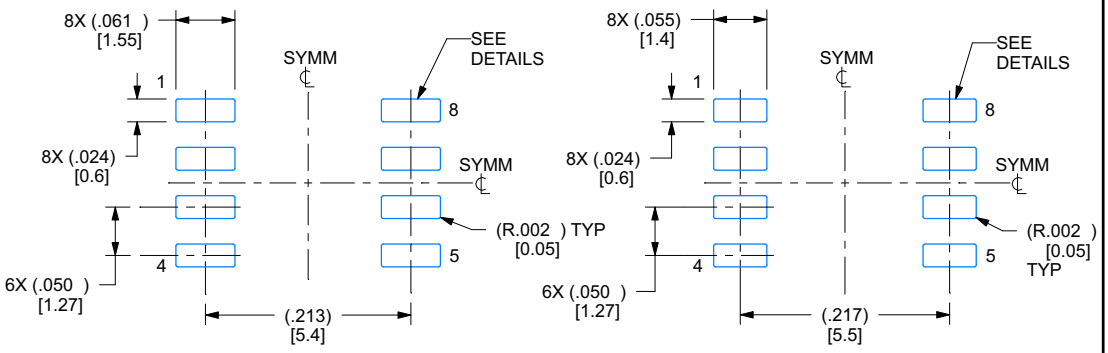
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

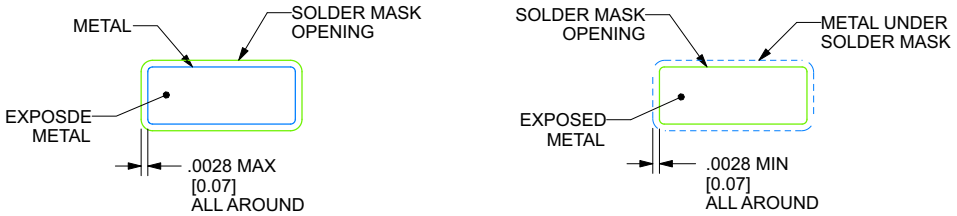
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

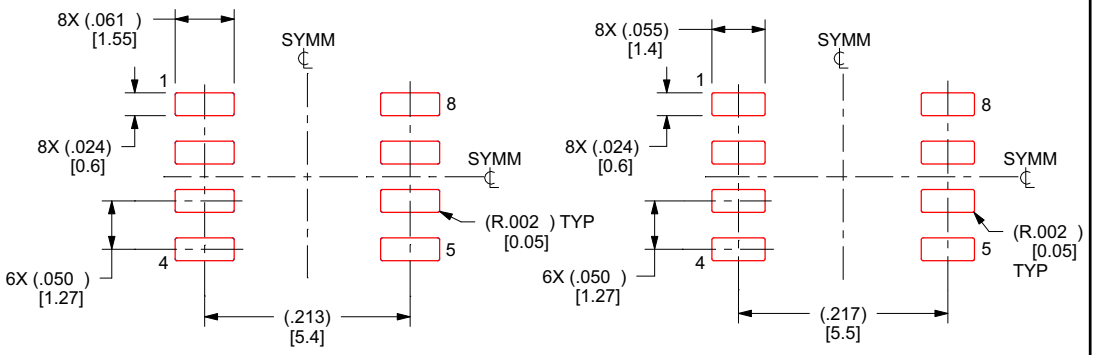
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMCS1100A1QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A1
TMCS1100A1QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A1
TMCS1100A2QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A2
TMCS1100A2QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A2
TMCS1100A3QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A3
TMCS1100A3QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A3
TMCS1100A4QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A4
TMCS1100A4QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	Q100A4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMCS1100-Q1 :

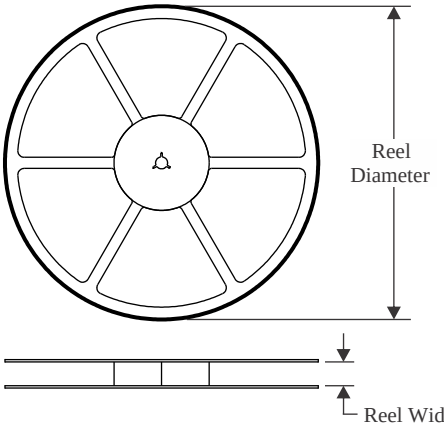
- Catalog : TMCS1100

NOTE: Qualified Version Definitions:

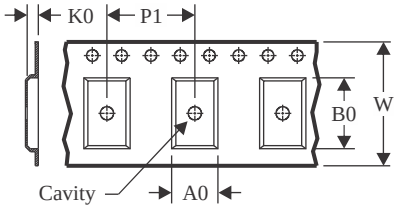
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

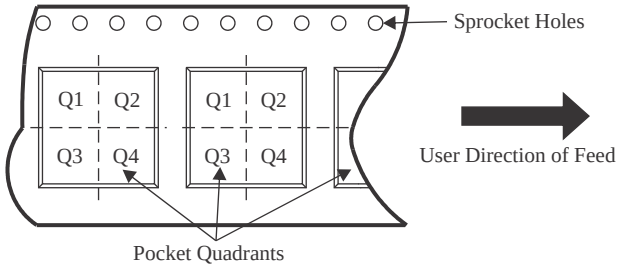


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

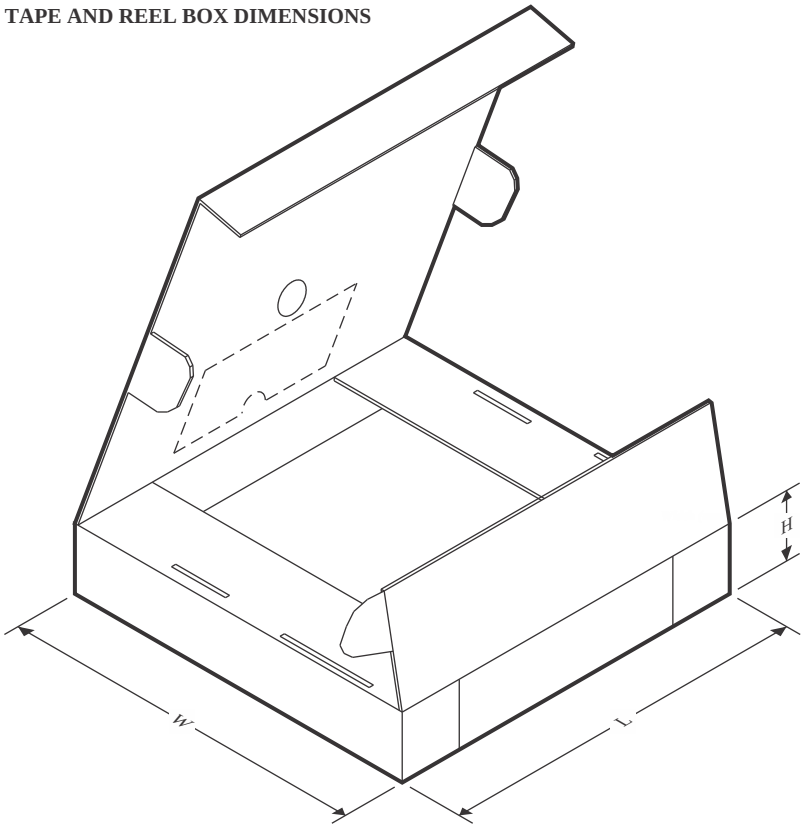
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMCS1100A1QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMCS1100A2QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMCS1100A3QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMCS1100A4QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMCS1100A1QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
TMCS1100A2QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
TMCS1100A3QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
TMCS1100A4QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

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