# *TMS320DM644x DMSoC Peripherals Overview*

# *Reference Guide*

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# Contents

# Read This First

## About This Manual

This document provides an overview and briefly describes the peripherals available on the TMS320DM644x Digital Media System-on-Chip (DMSoC).

## Related Documentation From Texas Instruments

The following documents describe the TMS320DM644x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM644x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

**SPRUE14** — ***TMS320DM644x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsystem in the TMS320DM644x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem, the video processing subsystem, and a majority of the peripherals and external memories.

**SPRUE15** — ***TMS320DM644x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM644x Digital Media System-on-Chip (DMSoC).

**SPRAA84** — ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

**SPRU732** — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

**SPRU871** — ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

## Trademarks

TMS320C64x+ is a trademark of Texas Instruments.

# TMS320DM644x DMSoC Peripherals Overview

## 1 Overview

The TMS320DM644x Digital Media System-on-Chip (DMSoC) is a highly-integrated hardware and software platform, designed to meet the application processing needs of next-generation embedded devices. The DM644x DMSoC enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high-processing performance, and long battery life through the maximum flexibility of a fully-integrated mixed-processor solution.

The dual-core architecture of the DM644x DMSoC provides benefits of both a digital signal processor (DSP) and reduced instruction set computer (RISC) technologies, incorporating a high-performance TMS320C64x+™ DSP core and an ARM926EJ-S core.

The user-accessible peripherals available on the DM644x DMSoC are configured using a set of memory-mapped control registers. The peripheral bus controller performs the arbitration for accesses of on-chip peripherals. Peripherals available on the DM644x DMSoC and their associated literature number are listed in Table 1.

**Table 1. TMS320DM644x DMSoC Peripherals Documentation**

| Peripheral/Module | Acronym | Lit # |
|---|---|---|
| Asynchronous External Memory Interface | EMIF | SPRUE20 |
| ATA Controller | ATA | SPRUE21 |
| Audio Serial Port | ASP | SPRUE29 |
| DDR2 Memory Controller | DDR2 | SPRUE22 |
| Enhanced Direct Memory Access Controller | EDMA | SPRUE23 |
| Ethernet Media Access Controller/Management Data Input/Output Module | EMAC/MDIO | SPRUE24 |
| General-Purpose Input/Output | GPIO | SPRUE25 |
| Host Port Interface | HPI | SPRUE97 |
| Inter-Integrated Circuit Module | I2C | SPRUE27 |
| Internal Direct Memory Access Controller | IDMA | SPRU871 |
| Interrupt Controller | INTC | SPRUE14 |
| Multimedia Card/Secure Digital Card Controller | MMC/SD | SPRUE30 |
| Phase-Locked Loop Controller | PLLC | SPRUE14 |
| Power-Down Controller | PDC | SPRU871 |
| Power and Sleep Controller | PSC | SPRUE14 |
| Pulse-Width Modulator | PWM | SPRUE31 |
| Serial Peripheral Interface | SPI | SPRUE32 |
| 64-Bit Timer | Timer | SPRUE26 |
| Universal Asynchronous Receiver/Transmitter | UART | SPRUE33 |
| Universal Serial Bus | USB | SPRUE35 |
| VLYNQ Port | VLYNQ | SPRUE36 |
| Video Processing Back End | VPBE | SPRUE37 |
| Video Processing Front End | VPFE | SPRUE38 |

## 2 Asynchronous External Memory Interface (EMIF)

The asynchronous external memory interface (EMIF) provides a means to connect to a variety of external devices including:

- NAND Flash
- Asynchronous devices including Flash and SRAM
- Host processor interfaces such as the host port interface (HPI) on a Texas Instruments DSP

The most common use for the EMIF is to interface with both Flash devices and SRAM devices. The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous devices. The EMIF features includes support for:

- 4 addressable chip select spaces of up to 32MB each
- 8-bit and 16-bit data bus widths
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- NAND Flash ECC generation
- Connecting as a host to a TI DSP HPI interface
- Data Bus Parking

## 3 Audio Serial Port (ASP)

The audio serial port (ASP) is used for audio interface purposes. The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface. The ASP can be controlled by the ARM CPU or the DSP CPU.

The ASP provides the following functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer

In addition, the ASP has the following capabilities:

- Direct interface to:
  - AC97 compliant devices (the necessary multiphase frame synchronization capability is provided)
  - IIS compliant devices
- A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
- μ-Law and A-Law companding
- 8-bit data transfers with the option of LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation

## 4 ATA Controller

The AT attachment/ATA packet interface (ATA/ATAPI) is an interface that is most commonly used by portable computers (PCs) and portable devices to interface a host processor with data storage or audio devices. The ATA interface debuted in the mid 1980s as an interface between a hard-disk drive and a PC by way of a ribbon cable. Ever since then, other devices, mostly storage, including compact Flash and compact disks have widely adopted the ATA/ATAPI interface, leveraging from its proven capability as the means for connecting to a host processor. These allowed device manufacturers to avoid building and supporting a proprietary interface that would significantly limit the use of their devices. The ATA/ATAPI interface is popular due to its simplicity, low cost, reliability, compatibility, as well as its wide acceptance and long history of use within the PC industry market.

The DM644x DMSoC supports an onboard ATA/ATAPI host controller module (IDE controller) allowing it to exploit access to a vast majority of available data storage and audio devices. The onboard IDE host controller performs PIO, multiword, and ultra-DMA transactions with ATA and ATAPI compliant devices. Hard-disk drive, compact disk (CD), compact Flash (CF), and DVD are some ATA/ATAPI-compliant devices that the IDE host controller is destined to interface with. This allows applications like streaming media and digital still cameras the means for easy access to commonly used external storage devices.

## 5 DDR2 Memory Controller

The DDR2 memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices. Memory types such as DDR1 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR2 memory controller is the major memory location for program and data storage.

The DDR2 memory controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- 256M-byte memory space
- Data bus width of 32 or 16 bits
- CAS latencies: 2, 3, 4, and 5
- Internal banks: 1, 2, 4, and 8
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little-endian mode

## 6 Enhanced Direct Memory Access (EDMA) Controller

The enhanced direct memory access (EDMA) controller handles all user-programmed data transfers between two slave endpoints on the device. The EDMA enables movement of data to/from any addressable memory spaces (internal/external), slave peripherals. The EDMA on the TMS320DM644x DMSoC has a different architecture from previous EDMA controllers on the C621x/C671x and C64x devices, it includes several enhancements over the previous EDMA controller and provides enhanced debug visibility and error reporting.

The EDMA controller has two principal blocks:

- EDMA channel controller
- EDMA transfer controller(s)

The EDMA channel controller primarily serves as the user interface for the EDMA controller. It also serves as event interface for the EDMA controller and is responsible for event latch-up, event prioritization, queue management, and transfer request (TR) submission to the EDMA transfer controllers. The EDMA transfer controllers are primarily responsible for data movement. The transfer controller is responsible for issuing read/write commands to the slaves.

## 7 Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module

The ethernet media access controller (EMAC) and physical layer (PHY) device management data input/output (MDIO) module is used to move data between the TMS320DM644x DMSoC and another host connected to the same network, in compliance with the Ethernet protocol. The EMAC is controlled by the ARM CPU of the device; control by the DSP CPU is not supported. The EMAC controls the flow of packet data from the system to the PHY and the MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the system core through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module and is considered integral to the EMAC/MDIO peripheral.

## 8 General-Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

The GPIO peripheral has the following features:

- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers:
  - Output register can be read to reflect output drive status.
  - Input register can be read to reflect pin status.
- Some GPIO signals can be used as interrupt sources with configurable edge detection.

## 9 Host Port Interface (HPI)

The host port interface (HPI) provides a parallel port interface through which an external host processor can directly access the TMS320DM644x DMSoC processor's resources (configuration and program/data memories). The external host device is asynchronous to the CPU clock and functions as a master to the HPI interface. The HPI enables a host device and the DM644x DMSoC processor to exchange information via internal or external memory. Dedicated address (HPIA) and data (HPID) registers within the HPI provide the data path between the external host interface and the processor resources. An HPI control register (HPIC) is available to the host and the CPU for various configuration and interrupt functions.

## 10 Inter-Integrated Circuit (I2C) Module

The inter-integrated circuit (I2C) module provides an interface between the TMS320DM644x DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DM644x DMSoC through the I2C module.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers mode
  - Support for multiple slave-transmitters and master-receivers mode
  - Combined master transmit/receive and receive/transmit mode
  - I2C data transfer rate of from 10 kbps up to 400 kbps (Philips I2C rate)
- 2 to 7 bit format transfer
- Free data format mode
- One read DMA event and one write DMA event that can be used by the DMA
- Seven interrupts that can be used by the CPU
- Interface to V-bus (32-bit synchronous slave bus)
- Module enable/disable capability

## 11 Internal Direct Memory Access (IDMA) Controller

The internal direct memory access (IDMA) controller in the TMS320C64x+ megamodule allows rapid data transfers between all local memories. It provides a fast way to page code and data sections into any memory-mapped RAM local to the C64x+ megamodule. The key advantage of the IDMA controller is that it allows for transfers between slower (level 2: L2) and faster (level 1: L1D, L1P) memory. The IDMA controller can provide lower latency than the cache controller since the transfers take place in the background of CPU operation, thereby removing stalls due to cache.

In addition, the IDMA controller facilitates rapid programming of peripheral configuration registers accessed through the external configuration space (CFG) port of the C64x+ megamodule. The IDMA controller view of the external configuration space that has a 32-word granularity and allows any register within a 32-word block to be individually accessed.

In summary, the IDMA controller is:

- Optimized for burst transfers of memory blocks (contiguous data).
- Allows access to and from any local memory (L1P, L1D, L2 (pages 0 and 1), and external CFG (but, source and destination cannot both be in CFG). CFG is accessible to channel 0 only. No CFG-to-CFG transfers.
- Supports the full data rate to and from the L2 memory controllers (256-bit data every extended memory controller (EMC) clock cycle):
  - Maximum throughput only achieved when source and destination are two different memories (L1P, L1D, and L2).
  - 50% throughput when source and destination are the same memory.
- Indicates transfer completion through programmable interrupts to the CPU.

The internal direct memory access (IDMA) controller is described in the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

## 12 Interrupt Controller (AINTC)

The TMS320DM644x DMSoC ARM interrupt controller (AINTC) has the following features:

- Supports up to 64 interrupt channels (16 external channels)
- Interrupt mask for each channel
- Each interrupt channel is mappable to a Fast Interrupt Request (FIQ) or to an Interrupt Request (IRQ) type of interrupt.
- Hardware prioritization of simultaneous interrupts
- Configurable interrupt priority (2 levels of FIQ and 6 levels of IRQ)
- Configurable interrupt entry table (FIQ and IRQ priority table entry) to reduce interrupt processing time

The ARM core supports two interrupt types: FIQ and IRQ. See the ARM926EJ Technical Reference Manual for detailed information about the ARM's FIQ and IRQ interrupts. Each interrupt channel is mappable to an FIQ or to an IRQ type of interrupt, and each channel can be enabled or disabled. The AINTC supports user-configurable interrupt-priority and interrupt entry addresses. Entry addresses minimize the time spent jumping to interrupt service routines (ISRs). When an interrupt occurs, the corresponding highest priority ISR's address is stored in the AINTC's ENTRY register. The IRQ or FIQ interrupt routine can read the ENTRY register and jump to the corresponding ISR directly. Thus, the ARM does not require a software dispatcher to determine the asserted interrupt.

The ARM interrupt controller (AINTC) is described in the *TMS320DM644x DMSoC ARM Subsystem Reference Guide* (SPRUE14).

## 13 Multimedia Card (MMC)/Secure Digital (SD) Card Controller

The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards. The communication between the MMC/SD card controller and MMC/SD card(s) is performed by the MMC/SD protocol.

The MMC/SD card controller has the following features:

- Supports interface to multimedia cards (MMC)
- Supports interface to Secure Digital (SD) memory cards
- Ability to use the MMC/SD protocol and Secure Digital Input Output (SDIO) protocol
- Programmable frequency of the clock that controls the timing of transfers between the MMC/SD card controller and memory card
- 256-bit read/write FIFO to lower system overhead
- Signaling to support enhanced direct memory access (EDMA) transfers (slave)
- 50 MHZ maximum clock to SD (specification version 1.1)

## 14 Phase-Locked Loop Controller (PLLC)

The TMS320DM644x DMSoC has two PLL controllers that provide clocks to different parts of the system. PLL1 provides clocks (though various dividers) to most of the components of the DM644x DMSoC. PLL2 is dedicated to the DDR2 port and components for the VPSS. The reference clock is the 27 MHZ crystal, as mentioned in the data manual.

The PLL controller provides the following:

- Glitch-Free Transitions (on changing clock settings)
- Domain Clocks Alignment
- Clock Gating
- PLL power down

The various clock outputs given by the controller are as follows:

- Domain Clocks: SYSCLK[1:*n*]
- Auxiliary Clock from reference clock source: AUXCLK
- Bypass Domain clock: SYSCLKBP

Various dividers that can be used are as follows:

- Post-PLL Divider: POSTDIV
- SYSCLK Divider: D1, ... D*n*
- SYSCLKBP Divider: BPDIV

Various other controls supported are as follows:

- PLL Multiplier Control: PLLM
- Software-programmable PLL Bypass: PLLEN

The PLL controller (PLLC) is described in the *TMS320DM644x DMSoC ARM Subsystem Reference Guide* (SPRUE14).

## 15 Power-Down Controller (PDC)

The TMS320C64x+ megamodule supports the ability to power-down various parts of the C64x+ megamodule. Using the power-down controller (PDC) in the C64x+ megamodule, the entire C64x+ megamodule can be powered-down. These power-down features can be used to design systems for lower overall system power requirements.

The power-down controller (PDC) is described in the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

## 16 Power and Sleep Controller (PSC)

The power and sleep controller (PSC) provides a standard method for controlling device power by gating clocks to individual modules. The PSC is described in the *TMS320DM644x DMSoC ARM Subsystem Reference Guide* (SPRUE14).

## 17 Pulse-Width Modulator (PWM)

The pulse-width modulator (PWM) peripheral is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. This PWM peripheral is basically a timer with a period counter and a first-phase duration comparator, where bit width of the period and first-phase duration are both programmable.

The PWM peripheral has the following features:

- 32-bit period counter
- 32-bit first-phase duration counter
- 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value.
- Configurable to operate in either one-shot or continuous mode.
- One-shot operation can be triggered by the CCD VSYNC output of the video processing subsystem to allow any of the PWM instantiations to be used as a CCD timer.
- Configurable PWM output pin inactive state.
- Interrupt and enhanced direct memory access (EDMA) synchronization events.

## 18 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the TMS320DM644x DMSoC at a programmed bit-transfer rate. The SPI is normally used for communication between the DM644x DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

The SPI allows serial communication with other SPI devices through a 3-pin or 4-pin mode interface. The DM644x DMSoC implementation supports multichip-select operation for up to two SPI slave devices. The SPI operates as a master SPI device only.

The SPI has the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit clock prescaler
- Programmable SPI clock frequency range
- Programmable character length (2 to 16 bits)
- Programmable clock phase (delay or no delay)
- Programmable clock polarity (high or low)

## 19 64-Bit Timer

TheTMS320DM644x DMSoC processor contains three software-programmable 64-bit timers (Timer 0, Timer 1, and Timer 2) that can be operated by either the ARM or the DSP. Timer 0 and Timer 1 are used as general-purpose timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

The 64-bit timer has the following features:

- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit general-purpose timer mode
  - Watchdog timer mode
- 2 possible clock sources:
  - Internal clock
  - External clock input via timer input pin TIN0 (Timer 0 only)
- 2 possible operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)
- Generates periodic interrupts to both the DSP and the ARM CPUs
- Generates synchronization event to EDMA

## 20 Universal Asynchronous Receiver/Transmitter (UART)

This universal asynchronous receiver/transmitter (UART) peripheral performs serial-to-parallel conversion on data received from a peripheral device or modem, and parallel-to-serial conversion on data received from the TMS320DM644x DMSoC processor CPU or DMA. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The UART peripheral has the following features:

- Programmable baud rates (frequency pre-scale values from 1 to 65535)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no PARITY bit generation and detection
  - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
  - The UART can be operated with or without the FIFOs
  - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using RTS and CTS signals for UART2
- Modem control functions (CTS, RTS) for UART2. No Modem control functions are available for UART0 and UART1.

## 21 Universal Serial Bus (USB)

The universal serial bus (USB) controller in the TMS320DM644x DMSoC supports high-speed USB device mode and high-speed limited host mode operations. The USB controller can be operated by the ARM through the memory-mapped registers.

The USB has the following features:

- Supports USB 2.0 peripheral at high speed (480 Mbps) and full speed (12 Mbps)
- Supports USB 2.0 host at high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps)
- Supports 4 simultaneous transmit (TX) and 4 receive (RX) endpoints, more can be supported by dynamically switching
- Each endpoint can support all transfer types (control, bulk, interrupt, and isochronous)
- Supports USB extensions for session request (SRP) and host negotiation (HNP)
- Includes a 4K endpoint FIFO RAM, and supports programmable FIFO sizes
- External 5V power supply for VBUS can be controlled through I2C
- Includes a DMA controller that supports 4 transmit (TX) and 4 receive (RX) DMA channels
- Includes RNDIS mode of DMA for accelerating RNDIS-type protocols using short packet termination over USB

## 22 VLYNQ Port

The VLYNQ peripheral provides a high-speed serial communications interface with the following features.

- Scalable performance/support
- Simple packet-based transfer protocol for memory-mapped access:
  - Write request/data packet
  - Read request packet
  - Read response data packet
  - Interrupt request packet
- Supports both symmetric and asymmetric operation:
  - Transmit (TX) pins on first device connect to receive (RX) pins on second device and conversely
  - Data pin widths are automatically detected after reset
  - Request packets, response packets, and flow control information are all multiplexed and sent across the same physical pins
  - Supports both host/peripheral and peer-to-peer communication
- Simple block code packet formatting (8b/10b)
- In-band flow control:
  - Allows receiver to momentarily throttle back transmitter when overflow is about to occur
  - Uses built-in special code capability of block code to seamlessly interleave flow control information with user data
- Multiple outstanding transactions
- Automatic packet formatting optimizations
- Internal loop-back mode

# 23 Video Processing Back End (VPBE)

The video processing back end (VPBE) in the video processing subsystem consists of the on-screen display (OSD) module, video encoder (VENC), and digital LCD controller (DLCD).

## 23.1 On-Screen Display (OSD) Module

The major function of the on-screen display (OSD) module is to gather and blend video data and display/bitmap data before feeding it to the video encoder (VENC) in YCbCr format. The video and display data is read from an external memory, typically DDR2. The OSD is programmed via control and parameter registers. The OSD has the following features:

- Simultaneous display of two video windows and two OSD windows.
- Support for a rectangular cursor window and a programmable background color selection.
- Support for attenuation of the YCbCr values for the REC601 standard.

## 23.2 Video Encoder (VENC)

The video encoder (VENC) generates analog video output. The VENC supports the following features:

- Master Clock Input - 27 MHZ (×2 Up-sampling)
- SDTV support
- HDTV support
- 4 10-bit over-sampling D/A converters
- Optional 7.5% pedestal
- 16-235/0-255 input amplitude selectable
- Programmable luma delay
- Master/slave operation
- Internal color bar generation (100%/75%)

## 23.3 Digital LCD Controller (DLCDC)

The digital LCD controller (DLCDC) generates digital RGB/YCbCr data output and timing signals. The DLCD supports the following features:

- Programmable DCLK
- Various output formats:
  - YCbCr 16bit
  - YCbCr 8bit
  - ITU-R BT. 656
  - Parallel RGB 24bit
  - Serial RGB
  - DisplayTech QVGA (MicroDisplay)
  - STN
- Low-pass filter for digital RGB output
- Programmable timing generator
- Built-in timing generators for EPSON/CASIO1G LCD panels
- Master/slave operation
- Internal color bar generation (100%/75%)

# 24 Video Processing Front End (VPFE)

The video processing front end (VPFE) in the video processing subsystem consists of the CCD controller (CCDC), preview engine, resizer, hardware 3A (H3A) statistic generator and histogram modules. Together these modules provide a powerful and flexible front-end interface. These modules are briefly described below:

## 24.1 CCD Controller (CCDC)

The CCD controller (CCDC) provides an interface to image sensors and digital video sources. The CCDC receives raw image/video data from sensors (CMOS or CCD) or YUV video data in numerous formats from video decoder devices. The CCDC output requires additional image processing to transform raw input images to final processed images. This processing can be done either on-the-fly in the preview engine or in software on the DSP and image coprocessor subsystem. Simultaneously, while processing, raw data input to the CCDC can be used for computing various statistics (H3A and histogram) for use in control of image/video tuning parameters.

## 24.2 Preview Engine

The preview engine is an image processing module that is configurable for various sensor types, image quality, and video frame rates for digital still camera preview and video recording. The preview engine transforms raw unprocessed image/video data from a sensor (CMOS or CCD) into YCbCr 422 data. The output of the preview engine is used for both video compression and external display devices such as an NTSC/PAL analog encoder or a digital LCD.

## 24.3 Resizer

The resizer module resizes the input image data to the desired display or video encoding resolution, including the ability to zoom up to 10×. The resizer module can accept input image/video data from either the preview engine or DDR2. The output of the resizer module is sent to DDR2.

## 24.4 Hardware 3A (H3A)

The hardware 3A (H3A) module provides control loops for auto focus (AF), auto white balance (AWB) and auto exposure (AE). There are 2 main components of the H3A module:

- Auto focus (AF) engine
- Auto exposure (AE) and auto white balance (AWB) engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a “paxel” for the case of AF.

The AE/AWB engine accumulates the values and checks for saturated values in a sub-sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a “window”. Thus, other than referring to them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

## 24.5 Histogram

The histogram module accepts raw image/video data (either 3 or 4 colors) and bins input color pixels, depending on the amplitude value and color, and provides statistics required to implement various hardware 3A (AF and AE/AWB) algorithms and tune the final image/video output. The value of the pixel is not stored, but each bin contains the number of pixels that are within the appropriate set range. The source of the raw data for the histogram is typically a CCD/CMOS sensor (via the CCD controller) or optionally from DDR2.

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