User's Guide

Hardware Design Considerations for Custom Board Using AM6442 , AM6422 , AM6412 and AM2434 Processors

ABSTRACT

This *Hardware Design Considerations for Custom Board* document gives an overview of the design considerations to be followed by the board designers while designing custom boards using any of the AM6442, AM6441, AM6422, AM6421, AM6412, AM6411, AM2434, AM2432, and AM2431 processors. This document is intended to be used as a guideline at different stages of custom board design by board designers.

Note

The Hardware Design Considerations document can be referenced for AM64x ALV (FCBGA, 441 pin) and AM243x ALV FCBGA [Lidded] (441 pin) packages or for AM243x ALX FC/CSP [SiP] (293 pin). See the *Device Comparison* table in the AM243x data sheet for differences and leverage the hardware design considerations for commonly supported peripherals.

Additionally, links are provided for processor product page, related collaterals, E2E FAQs, and other commonly referenced documents that can help the board designers optimize the design efforts and schedule during custom board design.

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1 Introduction

The Hardware Design Considerations for Custom Board Using AM6442, AM6441, AM6422, AM6421, AM6412, AM6411, AM2434, AM2432, and AM2431 Processors user's guide (document) provides a starting point for the board designers designing with any of these processors. This document provides an overview of the recommended design flow at different board design stages and highlights important design requirements that must be addressed. This document does not include all of the information required to complete the custom board design. In many cases, this document refers to the device-specific collaterals and various other documents as sources for specific information.

This document is organized in a sequential manner. The guide begins with decisions that must be made during the initial planning stages of the custom board design, through the selection of processor and key attached devices, electrical and thermal requirements. For providing a successful board design, address recommendations discussed in each section before moving to the next section.

Note

This document does not cover every aspect of custom board design.

Note

The processor family has capabilities to address safety requirements.

The focus of this document is non-safety applications.

1.1 Before Getting Started With the Custom Board Design

The processor family includes a wide variety of peripherals and processing capabilities, not all of which are used in every design. Consequently, the requirements for different designs using the same processor can vary widely depending on the target application. Board designers must understand the requirements before selecting the processor and determining the board-level implementation details. In addition, the custom board design can require additional circuitry to operate correctly in the target environment. See the latest collaterals on TI.com, including the device-specific data sheet, silicon errata, Technical Reference Manual (TRM), and EVM or SK user's guide for selecting the processor, and to determine the following:

- Expected environmental conditions for the processor operation, target boot mode, storage type, and interfaces
- Processing (Performance) requirements for each of the cores in the selected processor
- External DDR memory type (DDR4 or LPDDR4), speed, size that is used
- Processor peripherals used for the attached devices

1.2 Processor Selection

Selection of the processor is the most important stage of custom board design. To get an overview of the processor architecture and for selecting the processor variant, features, and speed grade, see the *Functional Block Diagram* and *Device Comparison* sections in the device-specific data sheet.

1.2.1 Availability of Tightly Coupled Memory (TCM)

See the device-specific data sheet for the R5F Tightly Coupled Memory (TCM) size information. Irrespective of the number of cores available, the TCM remains in the subsystem and can be used by the processor.

For AM642x, one core from each subsystem (cluster) is available resulting in 256K.

Lockstep is not supported on AM64x processors. See the device-specific TRM.

1.3 Technical Documentation

A number of documents relevant to the selected processor are available on the processor product page on TI.com. Read through these documents before starting the custom board design.

The following link summarizes the collaterals that can be referred to when starting the custom board design.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Collaterals to Get started.

1.3.1 Updated EVM or SK Schematics With Design, Review, and CAD Notes Added

During custom board design, customers tend to reuse the EVM or SK design files and make edits to the design file. Alternatively customers reuse some of the common implementations including the processor, memory, and communication interfaces. Since the EVM and SK are expected to have additional functionalities, customers optimize the EVM and SK implementation to suit the board design requirements. While optimizing the EVM or SK schematics, errors get introduced into the custom design that can cause functional, performance, or reliability issues. When optimizing, customers have queries regarding the EVM or SK implementation resulting in design errors. Many of the optimization and design errors are common across designs. Based on the learning and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note:), Review Notes (R-Note:), and CAD Notes (Cad Note:) were added near each section of the EVM or SK schematic so that customers can review and follow the notes to minimize errors. Additional files as part of the design downloads are included to support customer evaluation.

- **TMDS64EVM:** https://www.ti.com/lit/zip/sprr462
- **SK-AM64B:** https://www.ti.com/lit/zip/sprr460

The list of available documents in the single big zip files is listed in the following product overview documents.

- ***TMDS64EVM** Design Package Folder and Files List*
- ***SK-AM64B** Design Package Folder and Files List*

See also the following FAQs that include the PDF schematics and additional information related to starter kits:

[FAQ] AM6442 / AM6441 / AM6422 / AM6421 / AM6412 / AM6411 Custom board hardware design - Design and Review notes for Reuse of **TMDS64EVM** Schematics

[FAQ] AM6442 / AM6441 / AM6422 / AM6421 / AM6412 / AM6411 Custom board hardware design - Design and review notes for Reuse of **SK-AM64B** Schematics

1.3.2 FAQs to Support Custom Board Design

Based on customer interactions Texas Instruments continually adds FAQs for customer use.

The FAQ includes generic guidelines, learning based on customer interaction, and some of the commonly asked queries related to the processor peripherals.

A comprehensive list that links to all available FAQs for the Sitara™ processor families follows:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM64x, AM243x, AM335x) families

The list of FAQs is also listed by processor family in the following link:

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM/Starter kit

Note

The FAQs are updated frequently. Review the FAQs of interest on a regular basis for the most up-to-date information.

1.4 Design Documentation

Update the design documents periodically to capture all the requirements and design updates, observations during different stages of the custom board design.

Note

This updated information provides the basis for the documentation package and the *design document is required* when requesting external review support.

2 Block Diagram

A detailed block diagram, covering all the required functional blocks and interfaces is key to a successful custom board design.

2.1 Constructing the Block Diagram

Preparing a detailed block diagram is an important stage during the custom board design. The block diagram must include all major functional blocks, associated devices for processor functioning – PMIC, for example – and attached devices. The block diagram must illustrate the interfaces and IOs used for interconnecting the processor and attached devices.

Use the following resources as supporting documents when preparing the detailed block diagram:

- The SK-AM64B (AM64B starter kit for AM64x Sitara processors), TMDS64EVM (AM64x evaluation module for Sitara processors), TMDS243EVM (AM243x evaluation module for Arm® Cortex®-R5F based MCUs) and any other available EVMs or SKs are a good source to start with the custom board design.

- Use the following links for the processor product folder on TI.com. Each product folder provides device-specific Functional Block Diagrams, Data Sheet, TRM, User Guides, Silicon Errata, Application Notes, design considerations, and other related information for different applications. The design and development section includes EVM or SK information, design tools, simulation models, and software information. As part of the information related to support and training, links to commonly applicable E2E threads and FAQs are available.
  - AM6442 Product Folder
  - AM6441 Product Folder
  - AM6422 Product Folder
  - AM6421 Product Folder
  - AM6412 Product Folder
  - AM6411 Product Folder
  - AM2434 Product Folder
  - AM2432 Product Folder
  - AM2431 Product Folder

2.2 Configuring the Boot Mode

It is recommended to indicate the configured boot mode in the block diagram. This includes the primary boot and the backup boot.

The processor family includes multiple peripheral interfaces that support boot mode. Refer the device-specific TRM for the available boot mode configuration and supported peripherals. The processor family supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, then the ROM moves on to the backup mode.

The boot mode resistors connected to the processor boot mode input pins provide information on the boot mode to be used by the ROM code during boot. The boot mode inputs are sampled at power-on-reset (PORz_OUT). The boot mode configuration inputs must be stable before releasing (deassertion) the cold reset (MCU_PORz).

Boot mode configurations provide the below information:

- **PLL Config: BOOTMODE [02:00]** – Indicates the system clock (PLL reference clock selection) frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration
- **Primary Boot Mode: BOOTMODE [06:03]** – Configure the required primary boot mode, that is, the peripheral or memory to boot from
- **Primary Boot Mode Config: BOOTMODE [09:07]** – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected
- **Backup Boot Mode: BOOTMODE [12:10]** – Configure the required backup boot mode, that is, the peripheral or memory to boot from, in case the primary boot fails
- **Backup Boot Mode Config: BOOTMODE [13]** – This pin provides additional configuration options (optional - depends on the selected backup boot mode) for the backup boot devices
- **Reserved: BOOTMODE [15:14]** – Reserved pins

Key considerations for boot mode configuration:

- It is recommended to always include a provision to configure boot modes used during development, such as USB boot, UART boot or no-boot, or Dev boot mode for JTAG debug.
- Boot mode pins have alternate functions after latching of boot mode configuration. Ensure the board design takes this into account when choosing pullup or pulldown resistors for the boot mode pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the processor is reset (indicated by the PORz_OUT pin) to enable the processor to boot properly.
- Some boot mode pins functionalities are reserved. Any boot mode pins marked as *Reserved* or not used must not be left floating. It is recommended to pull the input high or low using a resistor. For details regarding connection of reserved boot mode pins, refer to the *BOOTMODE Pin Mapping* section of the *Initialization* chapter of the device-specific TRM.

For details regarding supported boot modes, refer to the *Initialization* chapter of the device-specific TRM.

Note

The board designer is responsible for providing a provision to set the required boot mode configuration (using pullups or pulldowns, and optionally jumpers or switches and external ESD) depending on the required boot configuration. Provide a provision for pullup and pulldown for the boot mode pins that have configuration capability.

Shorting the boot mode pins together, leaving any of the boot mode pins unconnected, or shorting of the boot mode inputs directly to supply or ground is not allowed or recommended.

Note

For updates related to supported boot modes and available boot mode functionality, see the device-specific silicon errata.

The following FAQ captures one of the boot mode implementation approaches when boot mode buffers are not used.

[FAQ] AM625 / AM623 / AM644x / AM243x / AM62A / AM62P - Bootmode implementation without buffers.

2.3 Confirming PinMux (PinMux Configuration)

The processor family supports a number of peripheral interfaces. To optimize size, pin count, and package while maximizing functionality, many of the processor pads (pins) have a provision to multiplex up to eight signal functions. Thus, not all peripheral interface instances are available or can be used simultaneously.

TI provides the SysConfig-PinMux Tool that helps the board designer configure the required function using PinMux for the AM64x or AM243x family of processors.

Note

Recommendation is to save the PinMux configuration generated using the SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

After completion of the processor selection and block diagram updates, the next stage of the custom board design is to determine the power supply architecture for the selected processor.

3.1 Power Supply Architecture

The power supply architecture that can be considered are listed below:

3.1.1 Integrated Power

The power architecture can be based on Multichannel ICs (PMIC), such as the TPS65219 or TPS65220 devices.

For the full application note and operational details, see the following documents:

- *Powering the AM64x with the TPS65220 or TPS65219 PMIC*
- *Powering the AM243x With the TPS65219 PMIC*

3.1.2 Discrete Power

The power architecture can be based on DC-DC converters and LDOs, refer to the *TMDS64EVM (AM64x evaluation module for Sitara processors)* EVM schematic.

When custom discrete power architecture is used, take note of the delay `MCU_PORz L->H` delay requirement for oscillator start-up after all the supplies ramp.

3.2 Power (Supply) Rails

For the complete list of processor power supply rails and the allowed supply range, see also the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details for some select power rails.

Note

Make sure the power supplies connected to the processor supply rails are within the *Recommended Operating Conditions* of the device-specific data sheet.

3.2.1 Core Supply

For the AM64x family of processors, core supply VDD_CORE is specified to operate at 0.75V or 0.85V (specified operating ranges defined in the *Recommended Operating Conditions* (ROC) table).

For the AM243x family of processors, core supply VDD_CORE is specified to operate only at 0.85V (specified operating ranges defined in the ROC table).

VDDR_CORE is specified to operate only at 0.85V (specified operating ranges defined in the ROC table).

When VDD_CORE is configured to operate at 0.75V, it is recommended to ramp 0.75V prior to all 0.85V supplies. When VDD_CORE is configured to operate at 0.85V, VDD_CORE and VDDR_CORE are recommended to be ramped together (powered from the same source).

Peripheral core supplies VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_0P85_USB0 are specified to operate only at 0.85V.

Peripheral core supplies VDD_MMC0 and VDD_DLL_MMC0 are specified to operate only at 0.85V when the MMC0 peripheral is used. It is recommended to connect VDD_MMC0 and VDD_DLL_MMC0 to the same power source as VDD_CORE when MMC0 peripheral is not used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

Note

AM64x supports 0.75V or 0.85V core voltage. The *Operating Performance Point (OPP)* is not tied to the core voltage. There is no change in performance between 0.75V or 0.85V core voltage. The 0.75V supply provides an option to optimize power and the 0.85V supply optimizes the number of power rails without change in performance.

Note

Setting the core supply to 0.8V is not an allowed option.

3.2.2 Peripheral Power Supply

The processor family supports dedicated peripheral supplies for USB0, MMC0, PLLs, ADC0, and SERDES0. The specified operating voltage is 1.8V. An additional 3.3V analog supply is required for USB.

Depending on the memory selected, DDR PHY IO (VDDS_DDR) and DDR clock IO (VDDS_DDR_C) supply rails are specified to be 1.1V (LPDDR4) or 1.2V (DDR4).

For more information, refer to the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Dynamic Switching Dual-Voltage IO Supply LDO

The processor family supports an integrated LDO (SDIO_LDO) to power the SDIO interface IO supply group and SD interface pullups, capable of dynamically switching between 1.8V and 3.3V voltage. The recommended output capacitor must be connected close to the LDO output pin (CAP_VDDSHV_MMC1). For guidance on recommended capacitance and connection, refer to the *Power Supply* subsection in the *Signal Descriptions* section of the device-specific data sheet.

V1P8_SIGNAL_ENA bit is used to control the LDO output level used for controlling the SD card interface IO (signaling). The output of the LDO is connected to the processor IO supply group used for the SD card interface (VDDSHV5 for UHS-I speed support).

VDDSHV5 IO supply group for MMC1 was designed to support the power-up, power-down, or dynamic supply voltage change without any dependency on other supplies. This capability is required to support UHS-I speed.

Refer the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the LDO (SDIO_LDO) when not used.

For more details, refer to the *Integrated Low-dropout Regulator (LDO)* section in the *Power* chapter of the device-specific TRM.

3.2.4 Internal LDOs for IO Groups (Processor)

The processor family supports eight internal LDOs (CAP_VDDSx [x = 0..5], CAP_VDDSHV_MMC1 and CAP_VDDS_MCU) and each of the LDO output connects to a separate ball (pin) for connecting an external capacitor. For guidance on recommended capacitance and connections, refer to the *Power Supply* subsection in the *Signal Descriptions* section of the device-specific data sheet. Follow the SK design for selection of the capacitor package. Not following the CAP_VDDSx recommended guidelines can affect the processor performance.

3.2.5 Dual-Voltage IOs (for Processor IO Groups)

The processor family supports seven dual-voltage IO groups (VDDSHVx [x = 0..5] and VDDSHV_MCU), where each IO group provides power to a predefined set of IOs. Each IO group can be individually configured for 3.3V or 1.8V. This supply powers all the predetermined IOs in the IO supply group. All IOs (attached devices) connected to these IO groups must be powered from the same power source that is being used to power the respective processor Dual-voltage IO groups (VDDSHVx supply rail).

Most of the processor IOs are not fail-safe. For information on available fail-safe IOs, see the device-specific data sheet. It is recommended to power the IO supply of the attached devices from the same power source as the respective processor dual-voltage IO groups (VDDSHVx supply rail) to make sure the system or board never applies potential to an IO that is not powered. This is needed to protect the IOs of the processor and the attached devices.

For more information, see [FAQ] AM625 / AM623 Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe). This is a generic FAQ and can also be used for the AM64x or AM243x family of processors.

The available IO group information is summarized in the following list:

- VDDSHV0 – Dual-voltage IO supply for Main reset and General interface IO group
- VDDSHV1 – Dual-voltage IO supply for PRG0 IO group
- VDDSHV2 – Dual-voltage IO supply for PRG1 IO group
- VDDSHV3 – Dual-voltage IO supply for GPMC0 IO group
- VDDSHV4 – Dual-voltage IO supply for OSPI0 IO group
- VDDSHV5 – Dual-voltage IO supply for MMC1 IO group
- VDDSHV_MCU – Dual-voltage IO supply for MCU General IO group

3.2.6 VPP (eFuse ROM Programming) Supply

The VPP supply can be sourced on-board or externally.

The VPP pin can be left floating (HiZ) or pulled down to ground through a resistor during processor power-up, power-down, and during normal processor operation.

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must applied only after completion of processor power-up sequence.
- It is recommended to use a fixed LDO with higher input supply (2.5V or 3.3V) and enable input. The enable input is required to be controlled by the processor GPIO for timing.

- The VPP power supply is expected to see high load current transients and local bulk capacitors are likely required near the VPP pin to support the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor.
- A maximum current of 400mA is specified during programming.
- When an external power supply is used, the supply is recommended to be applied after the processor power supplies ramp and are stable.
- When an external power supply is used, add an onboard bulk capacitor, decoupling capacitor, and discharge resistor near to the processor VPP supply pin. Add a test point to connect the external power supply and provision to connect one of the processor GPIOs to control the timing of the external supply.
- It is recommended to disable the VPP supply (left floating (HiZ) or grounded) when not programming the OTP eFuses.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application. This is a generic FAQ and can also be used for AM64x or AM243x family of processors.

For more information, refer to the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining Board Power Requirements

The current (maximum and minimum) requirements for each of the supply rails are not provided in the device-specific data sheet. These requirements are highly application dependent and must be estimated using TI provided tools for a specific use case.

3.4 Power Supply Filters

The processor family supports multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x = 0..2], VDDA_1P8_SERDES0, VDDA_1P8_USB0, and VDDA_ADC0. See also device-specific EVM or SK for implementation of power-supply filtering.

For more information, see [FAQ] AM625 / AM623 Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails. This is a generic FAQ and can also be used for the AM64x or AM243x family of processors.

3.5 Power Supply Decoupling and Bulk Capacitors

To decouple the processor and attached device supplies from board noise, use decoupling and bulk capacitors are recommended. Refer *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)*, *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* and other EVM or SK schematics for implementing the decoupling and bulk capacitors.

For guidance on optimizing and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

3.5.1 Note on PDN Target Impedance

The PDN target impedance values are provided for the specific supplies. The PDN target impedance values are not provided for all supply rails since the target impedance calculation includes reference to the maximum current on the power rails and is dependent on use case.

For updates on the PDN target impedance supplies and values, see [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Collaterals to Get started. Look for PDN target impedance values (VDD_CORE and VDDS_DDR).

3.6 Power Supply Sequencing

A detailed diagram of the required *Power Supply Sequencing* (Power-Up and Power-Down) are provided in the device-specific data sheet. All power supplies associated with the processor allow for a controlled supply ramp (refer to the supply slew rate) and supply sequencing (using a PMIC-based power supply or using onboard logic when discrete power solution is used).

For more information, see the *Power Supply Requirements, Power Supply Slew Rate Requirement*, and *Power Supply Sequencing* sections of the device-specific data sheet.

For more information, see [FAQ] AM625/AM623 Custom board hardware design – Processor power-sequencing requirements for power-up and power-down. This is a generic FAQ and can also be used for the AM64x or AM243x family of processors.

3.7 Supply Diagnostics

The processor family supports the following voltage monitors:

- VMON_VSYS (Recommend provisioning the external resistor voltage divider for early supply failure detection irrespective of the software implementation): For connecting the system voltage (main supply voltage such as 5V or higher voltage levels) through an external resistor voltage divider, refer to the *System Power Supply Monitor Design Guidelines* section of the device-specific data sheet. It is recommended to implement a noise filter (capacitor) across the resistor voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients. It is recommended to always provide resistor divider provision for early detection.
- VMON_1P8_SOC, VMON_1P8_MCU and VMON_3P3_SOC, VMON_3P3_MCU (Monitoring): These pins are recommended to be connected directly to the respective 1.8V and 3.3V supplies. For the allowed supply voltage range, refer to the *Recommended Operating Conditions* section of the device-specific data sheet.

Refer the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the voltage monitoring pins when not used.

3.8 Power Supply Monitoring

For optimizing the custom board performance, provide a provision for external monitoring of supply rails and load currents.

For more information, see the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)*, and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* schematics for implementation.

Now that the power supply architecture and the devices for generating the supply rails are finalized, update the block diagram to include the power supply rails and interconnection. It is also recommended to create a power supply sequence (Power-Up and Power-Down) diagram and verify the sequence with the device-specific data sheet.

4 Processor Clocking

The next stage of the custom board design is proper clocking of the processor and attached devices. The processor clock can be generated internally using an external crystal or an LVCMOS-compatible clock input can be used. Follow the connection recommendations in the device-specific data sheet when using an external clock. This section describes the available processor clock sources and the requirements.

4.1 Unused Clock Input

Not Applicable.

4.2 Processor External Clock Source

The recommended processor clock source and recommended connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

A 25MHz external crystal interface pin connected to the internal high-frequency oscillator (MCU_HFOSC0) or MCU_OSC0 LVCMOS digital clock is the default clock source for the internal reference clock HFOSC0_CLKOUT.

4.2.1 LVCMOS Digital Clock Source

The MCU_OSC0_XI clock input can be sourced from a 1.8V LVCMOS square-wave digital clock source. For more details, refer to the *Timing and Switching Characteristics, Clock Specifications, Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to connect the MCU_OSC0_XO pin as per the device-specific data sheet recommendation.

4.2.2 Crystal Selection

When selecting a crystal, the board designer must consider the temperature and aging characteristics based on the worst-case operating environment and expected life expectancy of the board. Verify the crystal load and the crystal load capacitor value including the PCB capacitance (for MCU_OSC0) used matches the data sheet recommendations. The selection of crystal load can allow for selection of a standard capacitor value. A mismatch in these values can introduce clock frequency PPM errors.

For more information, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Queries regarding Crystal selection.

For more information, see the *MCU_OSC0 Crystal Circuit Requirements* table of the device-specific data sheet.

It is recommended to verify the crystal selection with the crystal manufacturer, as required.

4.3 Processor Clock Output

The processor IO (pin) named CLKOUT0 can be configured as clock output. The clock output can be used as clock source for the attached devices (Example: Ethernet PHY).

For more details, refer to the device-specific data sheet and TRM.

5 JTAG (Joint Test Action Group)

TI supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support.

Refer [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1/ AM6442 / AM2432 Custom board hardware design – JTAG.

Although JTAG is not required for operation, it is recommended to include the JTAG connection in the custom board design.

5.1 JTAG and Emulation

Relevant documentation for the JTAG and Emulation includes:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG and Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the processor configuration.

As an emulation interface, the JTAG port can be used in different modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 or EMU1 (or both). EMU0 or EMU1 (or both) are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the processor configuration.

For supported JTAG clocking rates, see the device-specific TRM.

The required BSDL model for boundary scan testing can be downloaded from the following sections.

5.1.1.1 AM64x

- AM64x SR2.0 BSDL Model

5.1.1.2 AM243x [ALV]

- AM243x SR2.0 BSDL Model

5.1.1.3 AM243x [ALX]

- AM243x BSDL Model

5.1.2 Implementation of JTAG and Emulation

The JTAG and Emulation signals are referenced to the same IO group supply. The TDI, TDO, TCK, TMS, TRSTn, EMU0, and EMU1 signals are powered from the VDDSHV_MCU (Dual-voltage IO) supply rail (IO supply for IO group MCU). VDDSHV_MCU can be configured either 1.8V or 3.3V.

For proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and *XDS Target Connection Guide*.

5.1.3 Connection of JTAG Interface Signals

To connect the JTAG interface signals, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

In case a JTAG interface is not used, it is recommended to always provide a provision for connecting the JTAG interface signals using test points for development testing and the required pulls as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

6 Configuration (Processor) and Initialization (Processor and Device)

It is recommended to deassert (release) the processor cold reset input (MCU_PORz) only after all the processor supplies ramp and delay of recommended hold time (in ms) for the crystal or oscillator to start-up and stabilize (refer to the device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor family supports three external reset input pins (MCU and Main Domain cold reset request input (MCU_PORz), MCU and Main Domain warm reset request input (MCU_RESETz) and Main Domain warm reset request input (RESET_REQz)).

Be sure to make the recommended connections as per *Pin Connectivity Requirements* section of the device-specific data sheet.

The supported reset configurations are described in detail in the device-specific data sheet and TRM.

The processor provides three reset status output pins including Main Domain POR (cold reset) status (PORz_OUT) output, MCU Domain warm reset status (MCU_RESETSTATz) output, and Main Domain warm reset status (RESETSTATz) output.

Use of reset status outputs are application-dependent. Reset status outputs when not used can be left unconnected. It is recommended to provide a provision for a test point for testing or future enhancements. An optional pulldown is recommended.

For MCU_PORz (3.3V tolerant, fail-safe input), a 3.3V input can be applied. The input thresholds are a function of the 1.8V IO supply voltage (VDDS_OSC).

It is recommended to hold the MCU_PORz low during the supply ramp-up and crystal or oscillator start-up. Follow the recommended MCU_PORz timing requirement in the *Power-Up Sequencing* diagram of the device-specific data sheet.

Additional reset modes are available through processor internal registers and emulation.

6.2 Latching of the Boot Mode Configuration

For more details about the processor boot mode options, see Section 2.2.

Boot mode configurations for the processor are latched at the rising edge of PORz_OUT. The device configuration and boot mode input pins have alternate multiplexed functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for the alternate functions. The PORz_OUT reset status output indicates latching of boot mode configuration. PORz_OUT optionally can be used for latching the pin strap configuration for attached devices.

6.3 Resetting the Attached Devices

Using an ANDing logic to reset the attached devices as applicable (onboard media and data storage devices, and other peripherals) is recommended. The processor general purpose input/output (GPIO) pin is connected to one of the AND gate inputs with a provision for 0Ω to isolate the GPIO input for testing or debug. The processor IO buffers are off during reset. It is recommended to place a pullup near to the AND gate input to prevent the AND gate input from floating and enabling the reset logic controlled by the processor IO during power-up. Main Domain POR (cold reset) status output (PORz_OUT) or Main Domain warm reset status output (RESETSTATz) signal can be connected as the other input to the AND gate. Make sure the processor IO supply and the pullup supply used near to the AND logic input are sourced from the same power source.

The choice of reset status output is application-dependent. Make sure the attached device reset inputs are pulled as per the device recommendations.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, make sure the IO voltage level of RESETSTATz matches IO voltage level of the attached device. A level translator is recommended to match the IO voltage level.

It is recommended to provision for a software-enabled (controlled) power switch (load switch) that sources the SD Card power supply (VDD). A fixed 3.3V supply (IO supply connected to the processor) is connected as input to the power switch.

Use of the power switch allows power cycling of the SD Card (since this is the only way to reset the SD Card) and resetting the SD Card back to default state.

For more information on implementing reset logic for the attached devices and power switch enable logic for SD Card, see also *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)*, and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* and other EVM or SK schematics.

6.4 Watchdog Timer

Use of watchdog timer is based on the application requirement. Consider using internal or external watchdog timer.

7 Processor Peripherals

This section covers the processor peripherals and modules, and is intended to be used in addition to the information provided in the device-specific data sheet, TRM, and relevant application notes. The three types of documents available are:

- Data Sheet: Pin Description, Device operational modes, AC Timings, Guidance on pin functions, Pin mapping
- TRM: Functional Description, Programming Guide, Information regarding registers and configuration
- Application Notes: Board-level understanding and resolving commonly observed issues

7.1 Selecting Peripherals Across Domains

The processor architecture includes two domains, each domain includes specific processing cores and peripherals:

- MAIN Domain
- Microcontroller (MCU) Domain

For most use cases, peripherals from any of the domains can be used by any of the core. All peripherals, regardless of the domain, are memory mapped, and the Arm® Cortex®-A53 cores can detect and access most of the peripherals in the MCU Domain. Similarly, the MCU can access most of the peripherals in the Main Domain.

7.2 Memory (DDRSS)

DDR Subsystem supports LPDDR4 or DDR4 memory interface. See the *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter of device-specific data sheet for data bus width, inline ECC support, speed and max addressable range selection.

The allowed memory configurations are 1 × 16-bit or 2 × 8-bit.

1 × 8-bit memory configuration is not a valid configuration.

See the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the DDRSS signals when not used and DDR design guide for signals when LPDDR4 or DDR4 is used.

For more details, see the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

For more information on DDR4 or LPDDR4 memory interface, see the [FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDR4 / LPDDR4 MEMORY Interface.

7.2.1 Processor DDR Subsystem and Device Register Configuration

The DDR controller and DDR PHY have a large number of parameters to configure. To facilitate the configuration, an online tool (SysConfig tool) is provided that generates an output file that is consumed by the driver. Choose DDR Subsystem Register Configuration from the *Software Product* drop-down menu and choose the required processor. This tool takes board information, timing parameters from DDR device data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then initiates the full training sequence.

The SDK has an integrated configuration file for the memory (DDR4, LPDDR4) device mounted on the EVM or SK. If a configuration file is needed for a different memory (DDR4, LPDDR4) device, a new configuration file has to be generated using the DDR Register Configuration tool.

For more information, see [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration. This is a generic FAQ and can also be used for AM64x or AM243x family of processors.

7.2.2 Calibration Resistor Connection for DDRSS

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations in the device-specific data sheet.

7.2.3 Attached Memory Device ZQ and Reset_N Connection

Follow the device-specific EVM or SK schematics for connecting the recommended resistors (ZQ (Impedance calibration) and Reset_N (Memory reset input)) to the memory devices and the values.

7.3 Media and Data Storage Interfaces

Media and Data Storage interface supports 2 × Multimedia Card/Secure Digital (MMC/SD/SDIO) (8b + 4b).

MMC0 supports 8-bit eMMC interface (See the *MMC0 - eMMC Interface* section of device-specific data sheet for speed). EMMCPHY is a dedicate hard PHY implementation. The required pulls for the eMMC interface are implemented internal to the eMMC PHY and are JEDEC compliant. See the *Pin Connectivity Requirements* section of device-specific data sheet for MMC0 interface signals connection recommendations when the MMC0 interface is not used.

MMC1 supports a 4-bit SD or 4-bit SDIO interface (See also the *MMC1 - SD/SDIO Interface* section of device-specific data sheet for speed).

Additionally 1 × General-Purpose Memory Controller (GPMC) and 1 × OSPI or 1 × QSPI are supported.

For more information on eMMC memory interface, see [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface.

For more information on OSPI and QSPI memory interface, see [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface.

For information related to OSPI or QSPI, see the [FAQ] OSPI FAQ for Sitara/Jacinto devices.

For more details, see the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Ethernet Interface

The processor family supports up to five concurrent external Ethernet ports. Pinmuxing overlaps one of the CPSW3G and PRU1_ICSSG.

The processor family provides three MDIO interfaces and the recommendation is to connect CPSW MDIO to CPSW ports, PRG0 MDIO port to ICSSG0 Ethernet ports, and the PRG1 MDIO port to ICSSG1 Ethernet ports.

Before configuring the MDIO interface, see the advisory in *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS) (AM64x / AM243x Processor Silicon Revision 1.0, 2.0)*.

For more information on the Ethernet interface, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - Ethernet.

7.4.1 Common Platform Ethernet Switch 3-port Gigabit Ethernet (CPSW3G)

The CPSW3G interface can either be configured as a three-port switch (interfaces to two external Ethernet ports (port 1 and 2)) or a dual independent MAC interface with a unique MAC address.

CPSW3G supports the RMII (10/100) or RGMII (10/100/1000) interface for each of the external Ethernet interface ports.

For RMII interface implementation, see the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G RMII interface supports interfacing to Ethernet PHY configured as controller (master) or device (slave).

CPSW3G peripheral interfaces to RMII EPHY configured for an external 50MHz (buffered external oscillator or processor clock out) clock input (one of the buffered clock output connects to processor MAC) or EPHY configured for external 25MHz crystal or clock input with 50MHz clock output from EPHY connected to the processor.

One of the CPSW3G ports is an internal Communications Port Programming Interface (CPPI) host port, which is a streaming interface to provide data from DMA to CPSW3G and vice versa.

CPSW3G allows using mixed RGMII/RMII interface topology for the 2 × external interface ports.

RGMII_ID is not timed, tested, or characterized. RGMII_ID is enabled by default for TDx (Transmit data) and the register bit is reserved. Internal delay is not implemented for the RDx (Receive data) path.

For more details on the supported Ethernet interfaces, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4.2 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)

The processor family supports two instances of PRU_ICSSG subsystems and each PRU_ICSSG contains 2 × Ethernet ports (MII (10/100) or RGMII (10/100/1000)). See the device-specific TRM for information on support for SGMII mode. PRU_ICSSG supports industrial protocols and the supported protocols depends on processor selection.

For selecting the processor with PRU_ICSSG functionality, see [FAQ] AM6442: What PRU_ICSSG functionality is on each AM64x device?

For more details, see the *Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section in the *Processors and Accelerators* chapter of the device-specific TRM.

7.5 Universal Serial Bus (USB) Subsystem

The processor family supports 1 × USB 3.1 Dual-Role Device (DRD) Subsystem. This port is configurable as USB host (SuperSpeed Gen 1 (5Gbps), High-speed (480Mbps), Full-speed (12Mbps), and Low-speed (1.5Mbps)), USB device (High-speed (480Mbps), and Full-speed (12Mbps)), or USB Dual-Role device. USB 3.0 in device mode is not supported, only USB 2.0 in device mode is supported.

Follow the *USB VBUS Design Guidelines* section of the device-specific data sheet to scale the USB VBUS voltage (supply near the USB interface connector) before connecting to USB0_VBUS pin.

Connecting VBUS (VBUS supply input including Voltage Scaling Resistor Divider - Clamp) input is recommended to be connected when the USB interface is configured for device mode. Connection of VBUS (VBUS supply input including Voltage Scaling Resistor Divider - Clamp) is optional when the USB interface is configured for processor USB host mode.

A power switch with overcurrent (OC) output indication is recommended when the USB interface is configured as host for VBUS control. The USB DRVVBUS drives the power switch. It is recommended to connect the OC output to a processor GPIO (input) when the USB interface is configured as host.

For details related to USB connections and On-The-Go feature support, see the device-specific TRM.

For more details, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

When USB0 is not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the interface signals and USB supply pins.

For more information on USB2.0 interface, see [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – USB2.0 interface.

7.6 Peripheral Component Interconnect Express (PCIe) Subsystem

The processor family supports one PCI-Express Gen2 controller (PCIe) and supports Gen2 and Single Lane operation.

For more details, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

Note

No PCIe completion is generated as long as POWER_STATE_CHANGE_ACK is *0*. Configure POWER_STATE_CHANGE_ACK to *1* for generating PCIe completion.

Note

- The SerDes PHY (interface) of the processor is common for USB SuperSpeed and PCIe interface. Therefore, USB shall be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.
- The use of USB3 and PCIe is mutually exclusive for this family of processors so these (USB3 and PCIe) cannot be used at the same time.

For more information on the SERDES0 interface, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - SERDES - SERDES0 interface.

7.7 General Connectivity Peripherals

The processor family supports multiple instances of Inter-Integrated Circuit (I2C), Universal Asynchronous Receive-Transmit (UART), 12-bit Analog-to-Digital Converters (ADC), Multichannel Serial Peripheral Interfaces (MCSPI), Fast Serial Interface Receiver (FSI_RX) cores, Fast Serial Interface Transmitter (FSI_TX) cores, Enhanced Pulse-Width Modulator (EPWM), Enhanced Capture (ECAP), Enhanced Quadrature Encoder Pulse (EQEP), Modular Controller Area Network (MCAN) modules with or without full CAN-FD support and GPIO. All LVCMOS IOs can be configured as GPIO.

Note

For I2C interfaces with open-drain output type buffer (I2C0 and MCU_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration. See the *Pin Connectivity Requirements* section of device-specific data sheet.

When the open-drain output type buffer I2C interfaces are pulled to 3.3V supply, the inputs have slew rate limit specified. An RC is recommended used to limit the slew rate. See the device-specific EVM or SK for implementation.

An external pullup is recommended for the I2C interfaces (I2C1..3 and MCU_I2C1) with LVCMOS IOs emulated open-drain outputs when the IOs are configured for I2C interface. For the available LVCMOS IOs with emulated open-drain output I2C instances, see the device-specific data sheet.

For more information, see the following FAQs:

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – I2C interface

[FAQ] AM62A7-Q1: Internal pull configuration registers for MCU_I2C0 and WKUP_I2C0. This is a generic FAQ and can also be used for the AM64x or AM243x family of processors.

Additionally, PRU_ICSSG supports UART0, eCAP0, PWM, IEP0, and IEP1 peripheral modules.

The number of peripheral instances available depends on the processor selection. The required interfaces can be configured using the SysConfig-PinMux tool based on the application.

For more details, see the *Peripherals* chapter of the device-specific TRM.

7.8 Analog-to-Digital Converter (ADC)

The processor family supports 1 × 12-bit ADC, up to 4 MSPS, and 8 multiplexed analog inputs.

See the device-specific silicon errata (advisory i2287) for guidance on using SR2.0 processor on existing board or recommendations for a new custom board design.

For more details, see the *General Connectivity Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

Note that the processor family ADC inputs are not fail-safe. Do not apply external inputs before the processor supplies ramps.

7.8.1 Change Summary of AM64x, AM243x SR2.0 ADC Errata

One of the two pins assigned to the MMC0 PHY IO supply (VDDS_MMC0) in the SR1.0 processor is assigned as the ADC0_REFP pin in SR2.0. No compatibility issue is observed when installing a SR2.0 processor on a

PCB that was designed for the SR1.0 pin assignment since the ADC0_REFP operates at the same voltage as VDDS_MMC0. However, the ADC can have performance issues if trying to use the device when a SR2.0 processor is installed on a PCB designed for SR1.0 processors since noise from the MMC0 PHY IO supply can couple directly into the ADC0_REFP pin.

SR1.0 processor cannot be installed on a PCB designed for SR2.0 processors since this PCB has a dedicated ADC0_REFP source which gets shorted to VDDS_MMC0 when a SR1.0 processor is installed.

One of the VSS pin is re-assigned to be ADC0_REFN. Currently ADC0_REFN is connected to VSS in the package. This change eliminates any direct coupling of package ground bounce into the ADC reference. This pin change does not have any impact on the PCB design since the SR1.0 VSS pin is already connected to the PCB VSS plane and the new SR2.0 ADC0_REFN pin is expected to also be connected to the PCB VSS power plane.

7.9 Connection of Processor Power Supply Pins, Unused Peripherals and IOs

All the processor power supply pins must be supplied with the supply voltages specified in *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified.

The processor has pins (package balls) that have specific connectivity requirements and pins (package balls) that are recommended to be left unconnected or can be left unused.

For information on connecting the unused processor peripherals (MMC0, SERDES0, USB0, DDRSS0, and ADC0 (entire ADC or any of the ADC inputs are not used)) and IOs, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

For more information on processor unused peripherals and IOs, see the [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC Unused peripherals and IOs. This is a generic FAQ and can also be used for AM64x or AM243x family of processors.

7.9.1 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type buffer, fail-safe IO. It is recommended to connect an external pullup resistor when a PCB trace is connected to the pad and an external input is not being actively driven. Open-drain output type buffer IO has slew rate specified when the IO is pulled up to 3.3V. An RC is recommended for limiting the slew.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1/ AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection. This is a generic FAQ and can also be used for AM64x or AM243x family of processors.

7.9.2 Reserved (RSVD) Pins

Pins named RSVD are Reserved. Reserved pins must be left unconnected. It is recommended not to connect any PCB trace or test points to these pins.

8 Interfacing of Processor IOs (LVCMOS or Open-Drain or Fail-Safe Type IO Buffers) and Simulations

An important checkpoint during the custom board design before the schematic design and capture is to confirm electrical compatibility (DC and AC) between the processor and attached devices.

- The device-specific (processor and attached devices) data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, it is recommended to run simulations using the IBIS models provided.

For more information, see the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

The required IBIS model can be downloaded from the links provided in the following sections.

8.1 AM64x

- AM64x SR2.0 IBIS Model

8.2 AM243x [ALV]

- AM243x SR2.0 IBIS Model

8.3 AM243x [ALX]

- AM243x IBIS Model

9 Processor Current Rating and Thermal Analysis

The board power consumption depends on selected processor, peripherals connected, features implemented, application, operating temperature requirements, and temperature or voltage variations.

9.1 Power Estimation

For estimating the processor power, use *AM64x Power Estimation Tool*.

9.2 Maximum Current Rating for Different Supply Rails

For information on the maximum current rating for different supply rails, see the *AM64x Maximum Current Ratings*.

9.3 Power Modes

For more details on the available power modes, see the *Device Power States* section in the *Device Configuration* chapter of the device-specific TRM.

9.4 Thermal Design Guidelines

The *Thermal Design Guide for DSP and Arm Application Processors* application note provides guidance for successful implementation of a thermal solution for custom board designs using the Sitara family of processors. This application report provides background information on common terms and methods. Any needed follow-up design support is provided only for board designs that follow thermal design guidelines contained in the application report.

Download the required Thermal model from the following sections.

9.4.1 AM64x

- AM64x/AM243x Thermal Model

9.4.2 AM243x [ALV]

- AM64x/AM243x Thermal Model

9.4.3 AM243x [ALX]

- AM243x Thermal Model

9.4.4 VTM (Voltage Thermal Management Module)

Independent temperature sensors are located at different hotspots on the processor.

See also [FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – VTM.

10 Schematics:- Design, Capture, Entry and Review

At this stage of the custom board design, schematic design, capture and entry can be started.

The following FAQ summarizes key collaterals to reference during schematic design and review of the schematics.

[FAQ] AM64x, AM62x, AM62Ax, AM62Px Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

Refer below sections during the schematic design and capture stage:

10.1 Selection of Components and Values

Be sure to use the recommended values including the tolerance and voltage rating in the device-specific data sheet as applicable when selecting the passive components.

10.2 Schematic Design and Capture

During the schematic design and capture stage of the custom board design, the schematics can be drawn newly or EVM or SK schematics can be reused.

See the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)* and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* schematics.

When using the AM243x (ALX package), see the following link for the design files:

https://www.ti.com/tool/LP-AM243

During schematic design and capture, follow *AM6442, AM6422, AM6412 and AM2434 Schematic Design and Review Checklist* and device-specific silicon errata.

The following link summarizes the considerations board designers are required to be familiar when reusing TI EVM or SK design files.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - Reusing TI EVM design files.

Note

When EVM or SK schematics is reused, ensure completeness of functionality and change in net name due to redesign are reviewed. Read the notes added on the schematics pages near to the circuit implementation.

When EVM or SK schematics are reused, it is possible the DNI settings for the components were reset. Make sure the DNIs are reconfigured (populating DNIs can affect the functionality). Read the notes added on the schematics pages near to the circuit implementation.

10.3 Schematics Review

After completing the schematic design and capture, verify the custom board design against the *AM6442, AM6422, AM6412 and AM2434 Schematic Design and Review Checklist*.

For more information on used pins, unused pins, or peripherals handling, see [FAQ] AM62x, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals ? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSx, ...).

Plan a schematic review internally to review the schematics with reference to the *Schematic Design and Review Checklist*. Verify circuit implementation for design errors, value or connection inaccuracies, missing net connections, and so forth.

Be sure to verify the schematics follow the recommendations in the *Pin Connectivity Requirements* section of the device-specific data sheet.

11 Floor Planning, Layout, Routing Guidelines, Board Layers, and Simulation

After completing the schematic design, capture, entry and review (self, team, and external (devices suppliers)), the recommendation is to perform floor planning of the board to determine the interconnect distances between the different devices, board size, and outline.

The next stage in the custom board design is the board layout. Use the following sections for recommendations related to the board layout.

11.1 Escape Routing for PCB Design

The *AM64x and AM243x BGA Escape Routing* user's guide provides a sample PCB escape routing for the AM64x and AM243x family of processor.

11.2 DDR Layout Guidelines

See the *AM64x/AM243x DDR Board Design and Layout Guidelines*. The goal of the guide is to simplify the DDR4 or LPDDR4 implementation. Requirements are captured as a set of layout (placement and routing) guidelines that allow board designers to successfully implement a robust design for the topologies supported by the processor. Any needed follow-up design support is provided only for board designs using DDR4 or LPDDR4 memories that follow the *AM64x/AM243x DDR Board Design and Layout Guidelines*.

See the *AM64x/AM243x DDR Board Design and Layout Guidelines* for the recommended impedance for the DDR4 or LPDDR4 signals.

For the propagation delay, the delay to be considered for DDR4 or LPDDR4 is the delay related to the traces on the board. If package level propagation delay is required, contact the local TI sales representative.

It is recommended to perform Signal Integrity (SI) simulations during board schematic design and layout stage.

Note

Additionally, refer to the AM625 / AM623 DDR design guide that is currently being updated for the DDR interface configuration and simulation guidelines.

Note

DDR2 and DDR3 interfaces are not supported.

11.3 High-Speed Differential Signals Routing Guidance

The *High-Speed Interface Layout Guidelines* application note provides guidelines for successful routing of the high-speed differential signals. Guidelines include PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. Any follow-up design support needed is only provided for board designs that follow *High-Speed Interface Layout Guidelines*.

Note

Consider using the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)* and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* layouts for reference, as needed.

11.4 Board Layer Count and Stack-up

An important constraint in determining layer count is the number of layers required to implement the high-speed DDR4 or LPDDR4 memory interface. Memory layout meeting the recommended guidelines typically requires the number of layers used in the EVM or SK (TI recommended). Optimization of layer count can be possible based on the custom board design and functionalities. See also the *AM64x and AM243x BGA Escape Routing* user's guide.

See the *AM64x / AM243x DDR Board Design and Layout Guidelines* available on TI.com for further guidance and recommendations for implementing the DDR4 or LPDDR4 memory interface.

11.4.1 Simulation Recommendations

Simulation is recommended for any layout changes or optimizations done with respect to the EVM or SK layout.

11.5 Reference for Steps to be Followed for Running Memory Simulation

To get an overview of the basic system-level board extraction, simulation, and analysis methodologies for high-speed LPDDR4 memory interface, see also the *LPDDR4 Board Design Simulations* chapter of the *AM62Ax/AM62Px LPDDR4 Board Design and Layout Guidelines* application note.

An AM625 or AM623 DDR design guide (similar to the AM64x DDRSS) is being authored and can be referenced for 16-bit DDRSS memory interface.

12 Custom Board Assembly and Testing

The next phase of custom board design is board assembly, board bring-up, and functional and performance testing.

Before powering the custom board, make sure no components marked as DNP or DNI in the design are mounted.

No external input must be applied before the processor IO supply ramps.

Make sure none of the processor IO pullups have the supply rail referenced to the power source that is available before the processor IO supplies ramp.

12.1 Guidelines and Board Bring-up Tips

See the following FAQs during board bring-up:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Circuit Optimization of Custom board hardware design

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62Ax, AM62Px)

[FAQ] AM64x Common design Errors / Recommendations for Custom board hardware design – EVM / SK Schematics Design Update Note

13 Device Handling and Assembly

Moisture Sensitivity Level (MSL) rating and Peak reflow rating depends on the package dimensions (thickness and volume).

Recommended reviewing the device thickness information, ball pitch, Lead finish and Ball material, and the recommended MSL rating and Peak reflow to be followed.

For more information, use the following links:

- AM6442 Ordering and quality
- AM6441 Ordering and quality
- AM6422 Ordering and quality
- AM6421 Ordering and quality
- AM6412 Ordering and quality
- AM6411 Ordering and quality
- AM2434 Ordering and quality
- AM2432 Ordering and quality
- AM2431 Ordering and quality

13.1 Soldering Recommendations

Note the MSL rating and Peak reflow recommendation on TI.com for the selected processor.

13.1.1 Additional References

For more information on Moisture sensitivity level, see also the following links:

- Texas Instruments, *MSL Ratings and Reflow Profiles Application Note*
- Texas Instruments, *Moisture sensitivity level search*

14 References

14.1 AM64x

- Texas Instruments: *AM64x Sitara™ Processors Data Sheet*
- Texas Instruments: *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*
- Texas Instruments: *TMDS64EVM (AM64x evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64DC01EVM (AM64x IO-link and high-speed breakout card)*
- Texas Instruments: *Powering the AM64x with the TPS65220 or TPS65219 PMIC*
- Texas Instruments: *TMDS64EVM Design Package Folder and Files List*
- Texas Instruments: *SK-AM64B Design Package Folder and Files List*

14.2 AM243x

- Texas Instruments: *AM243x Sitara™ Microcontrollers Data Sheet*
- Texas Instruments: *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)*
- Texas Instruments: *LP-AM243 (AM243x general purpose LaunchPad™ development kit for Arm®-based MCU)*
- Texas Instruments: *TMDS243DC01EVM (AM243x and AM64x evaluation module breakout board for high-speed expansion)*
- Texas Instruments: *Powering the AM243x With the TPS65219 PMIC*
- Texas Instruments: *AM243x OSPI, QSPI Flash Selection Guide*

14.3 Common

- Texas Instruments, *AM64x / AM243x Sitara Processors Technical Reference Manual*
- Texas Instruments, *AM64x / AM243x Processor Silicon Errata*
- Texas Instruments, *AM64x / AM243x Power Estimation Tool*
- Texas Instruments, *AM64x / AM243x Schematic Design and Review Checklist*
- Texas Instruments, *AM64x and AM243x BGA Escape Routing*
- Texas Instruments, *AM64x / AM243x DDR Board Design and Layout Guidelines*
- Texas Instruments, *AM62A3 / AM62A7 DDR Board Design and Layout Guidelines*
- Texas Instruments, *Thermal Design Guide for DSP and Arm Application Processors Application Report*
- Texas Instruments, *PRU-ICSS Feature Comparison*
- Texas Instruments, *Industrial Communication Protocols Supported on Sitara™ Processors and MCUs*
- Texas Instruments, *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments, *High-Speed Interface Layout Guidelines*
- Texas Instruments, *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines*
- Texas Instruments, *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments, *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments, *XDS Target Connection Guide*
- Texas Instruments, *MSL Ratings and Reflow Profiles*
- Texas Instruments, *Moisture sensitivity level search*
- Texas Instruments, *Jacinto™ 7 DDRSS Register Configuration Tool*
- Texas Instruments, *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments, *Clocking Design Guide for KeyStone Devices*
- Texas Instruments, *Using IBIS Models for Timing Analysis*
- Texas Instruments, *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs*
- Texas Instruments, *Sitara MCU Thermal Design*
- Texas Instruments, *Functional Safety Support for Arm®-based Microcontrollers and Processors*
- Texas Instruments, *AM64x/AM243x Extended Power-On Hours*
- Texas Instruments, *AM64x, AM243x IEC61508 TUV SUD Functional Safety Certificate*

15 Terminology

ADC	Analog-to-Digital Converter
BSDL	Boundary-Scan Description Language
CAN-FD	Controller Area Network Flexible Data-Rate
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
DRD	Dual-Role Device
E2E	Engineer to Engineer
ECAP	enhanced Capture
ECC	Error-Correcting Code
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EPWM	enhanced Pulse-Width Modulator
EQEP	enhanced Quadrature Encoder Pulse
FAQ	Frequently Asked Question
FSI_RX	Fast Serial Interface Receiver
FSI_TX	Fast Serial Interface Transmitter
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High-Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IEP	Industrial Ethernet Peripheral
JTAG	Joint Test Action Group
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MAC	Media Access Controller
MCAN	Modular Controller Area Network
MCASP	Multichannel Audio Serial Ports
MCU	Micro Controller Unit
MDIO	Management Data Input/Output
MII	Media Independent Interface
MMC	Multi-Media Card
MSL	Moisture Sensitivity Level
OPP	Operating Performance Point
OSPI	Octal Serial Peripheral Interface
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
PRU_ICSSG	Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit

PWM	Pulse-Width Modulator
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TCM	Tightly Coupled Memory
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select Input
TRM	Technical Reference Manual
TRSTn	Test Reset
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCA	Via Channel Array
VTM	Voltage Thermal Management Module
XDS	eXtended Development System

16 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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