

PRU-ICSS / PRU_ICSSG Migration Guide

ABSTRACT

This migration guide details the PRU-ICSS (Programmable Real-time Unit and Industrial Communication Subsystem) and PRU_ICSSG (Programmable Real-time Unit and Industrial Communication Subsystem - Gigabit) hardware differences, and outlines software modifications required for porting custom PRU firmware and Arm® code from one Sitara device to another.

Contents

1	Introduction	2
2	PRU-ICSS / PRU_ICSSG Hardware Differences	2
3	Porting PRU Software Between Devices	9
4	Appendix– Device Hardware Comparison	11

List of Tables

1	PRU-ICSS / PRU_ICSSG Base Address Comparison for Global Memory Map	2
2	PRU-ICSS / PRU_ICSSG Local Memory Map Comparison	3
3	GPI/GPO Mode Comparison	5
4	IEP Feature Comparison	7
5	MII_RT Feature Comparison	7
6	PRU_ICSSG MII and RGMII Feature Comparison.....	8
7	PRU Firmware Checklist.....	9
8	ARM Code Checklist	9
9	Comparison of Constant Table MMR Address Mapping	11
10	Comparison of Constant Table Peripheral Mapping	12
11	Comparison of System Events [159-64].....	13
12	Comparison of System Events [63-32]	16
13	Comparison of System Events [31-0].....	18
14	Host Interrupt Comparison	19

Trademarks

Arm is a registered trademark of Arm Limited.
 All other trademarks are the property of their respective owners.

1 Introduction

This document serves as a software migration guide to assist in porting custom software developed for the PRU-ICSS (Programmable Real-time Unit and Industrial Communication Subsystem) and PRU_ICSSG (Programmable Real-time Unit and Industrial Communication Subsystem - Gigabit) from one Sitara device to another. The specific PRU-ICSS / PRU_ICSSG devices covered by this guide include:

- PRU-ICSS: AM335x, AM437x, AM574x, AM572x, AM571x, AM570x, and K2G
- PRU_ICSSG: AM65x

For more details about the PRU-ICSS / PRU_ICSSG on each device, see the PRU-ICSS / PRU_ICSSG chapter in the device-specific Technical Reference Manual (TRM).

NOTE: The focus of this document is the PRU subsystem and broad market, non-industrial applications. Some ICSS or industrial-specific features may be omitted.

NOTE: No migration changes are required for software available through the processor SDK.

2 PRU-ICSS / PRU_ICSSG Hardware Differences

This section provides a detailed overview of the PRU-ICSS / PRU_ICSSG hardware differences between different Sitara devices.

2.1 Feature Comparison

For a high-level feature comparison, refer to the [PRU-ICSS / PRU_ICSSG Feature Comparison](#) application note. The rest of this guide describes the features outlined in the application note, and provides more details regarding specific differences.

2.2 PRU Core and Clock Comparison

The PRU_ICSSG has two auxiliary PRU cores, called RTU_PRUs. Unless explicitly stated in this guide, the RTU_PRUs function the same as the PRU cores.

The default PRU frequency is 200 MHz. However, the maximum frequency varies for each device, as summarized in [PRU-ICSS / PRU_ICSSG Feature Comparison](#) application note. The PRU_ICSSG devices add a new Core/VBUS sync mode that lets the PRU cores operate in lock-step with the PRU_ICSSG interconnect, enabling the lowest latency and highest speed.

2.3 PRU-ICSS / PRU_ICSSG Memory Map Comparison

2.3.1 PRU-ICSS / PRU_ICSSG Base Address for Global Memory Map

The PRU-ICSS / PRU_ICSSG base address within the SoC memory map differs between devices. [Table 1](#) compares these base addresses, which function as the starting address for the PRU-ICSS / PRU_ICSSG global memory map.

Table 1. PRU-ICSS / PRU_ICSSG Base Address Comparison for Global Memory Map

	AM335x	AM437x ⁽¹⁾	AM57x	K2G	AM65x
PRU-ICSS0 / PRU_ICSSG0				0x00_20A8_0000	0x00_0B00_0000
PRU-ICSS1 / PRU_ICSSG1	0x4A30_0000	0x5440_0000	0x4B20_0000	0x00_20AC_0000	0x00_0B10_0000
PRU-ICSS2 / PRU_ICSSG2			0x4B28_0000		0x00_0B20_0000

⁽¹⁾ On the AM437x, the base address listed above corresponds to PRU-ICSS1. The PRU-ICSS0 memory map is accessed through the PRU-ICSS1 expansion port (address 0x5444_0000).

2.3.2 PRU-ICSS / PRU_ICSSG Local Memory Map

[Table 2](#) shows the differences between the PRU-ICSS / PRU_ICSSG local memory map on Sitara devices. To summarize, the memory map is mostly the same across devices, with the exception of new features being added into the memory map.

Table 2. PRU-ICSS / PRU_ICSSG Local Memory Map Comparison

Start Address	AM335x	AM437x	AM570x	AM571x	AM572x SR2.0	AM572x SR1.1	AM574x	K2G	AM65x
0x0000_0000	Data RAM 0/1								
0x0000_2000	Data RAM 1/0								
0x0000_4000	Reserved								
0x0000_8000	Reserved								RAT_SLICE0
0x0000_9000	Reserved								RAT_SLICE1
0x0001_0000	Shared Data RAM 2								
0x0002_0000	INTC								
0x0002_2000	PRU0 Control								
0x0002_3000	Reserved								RTU_PRU0 Control
0x0002_3800	Reserved								RTU_PRU1 Control
0x0002_4000	PRU1 Control								
0x0002_4400	Reserved								
0x0002_4C00	Reserved								PROTECT
0x0002_6000	CFG								
0x0002_7000	Reserved							ECC_CFG	PA_STATS_QRAM
0x0002_8000	UART 0								
0x0002_A000	Reserved								TM_CFG_PRU0
0x0002_A100	Reserved								TM_CFG_RTU0
0x0002_A200	Reserved								TM_CFG_PRU1
0x0002_A300	Reserved								TM_CFG_RTU1
0x0002_C000	Reserved								PA_STATS_CRAM
0x0002_E000	IEP								IEP0
0x0002_F000	Reserved								IEP1
0x0003_0000	eCAP 0								
0x0003_2000	MII_RT_CFG								
0x0003_2200	Reserved								SGMII0_CFG ⁽¹⁾
0x0003_2400	Reserved								SGMII1_CFG ⁽¹⁾
0x0003_2400	MII_MDIO								
0x0003_3000	Reserved								ICSS_G_CFG

⁽¹⁾ On the AM65x, SGMII is only supported on PRU_ICSSG2.

Table 2. PRU-ICSS / PRU_ICSSG Local Memory Map Comparison (continued)

Start Address	AM335x	AM437x	AM570x	AM571x	AM572x SR2.0	AM572x SR1.1	AM574x	K2G	AM65x
0x0003_4000	Reserved								
0x0004_0000	Reserved	External port to other PRU-ICSS							Reserved

2.3.3 PRU-ICSS Submodules Register Content and Offsets

The register content and offsets of the following PRU-ICSS / PRU_ICSSG submodules are identical on all devices covered by this guide:

- PRU-ICSS UART
- PRU-ICSS eCAP

The register content and offsets of the following PRU-ICSS / PRU_ICSSG submodules differ between devices:

- PRU-ICSS IEP
- PRU-ICSS CFG
- PRU-ICSS MII_RT

The register content and offsets of the following MMRs are the same between PRU-ICSS devices, but differ between PRU-ICSS and PRU_ICSSG devices:

- PRU-ICSS PRU<n> Control
- PRU-ICSS PRU<n> Debug
- PRU-ICSS RTU PRU<n> Control
- PRU-ICSS RTU PRU<n> Debug
- PRU-ICSS INTC
- PRU-ICSS MDIO

2.4 Constant Table Differences

The PRU-ICSS / PRU_ICSSG constant table on all devices have 24 entries with fixed addresses and 8 entries with partially programmable entries. However, the addresses and associated peripheral or memory may differ between devices. Refer to [Section 4.1](#) for the full comparison.

2.5 PRU Module Interface to PRU I/O Differences

The basic functionality and basic structure of R30 and R31 are preserved on all devices. R30 serves as an interface to the GPO pins, and R31 serves as an interface to the GPI pins and INTC status. However, the supported GPI/GPO modes differs between devices.

Table 3. GPI/GPO Mode Comparison

	AM335x	AM437x	AM570x	AM571x	AM572x SR2.0	AM572x SR1.1	AM574x	K2G	AM65x
Direct Input	√	√	√	√	√	√	√	√	√
Parallel Capture	√	√	√	√	√	√	√	√	√
Shift In	√	√	√	√	√	√	√	√	√
Direct Output	√	√	√	√	√	√	√	√	√
Shift Out	√	√	√	√	√	√	√	√	√
EnDat		√	√	√			√	√	√
Sigma Delta		√	√	√			√	√	√

The following GPIO modes in PRU_ICSSG devices are upgraded versions of the other PRU-ICSS devices:

- Direct Output – Adds optional bidirectional support, enabled through CTRLMMRs. Backwards compatible with PRU-ICSS devices.
- Shift In – Adds configuration options. Backwards compatible with PRU-ICSS devices.
- Shift Out – Adds configuration options. Backwards compatible with PRU-ICSS devices.
- EnDat – Adds option to configure RX Start Bit polarity (previously fixed to "1"). Backwards compatible with PRU-ICSS devices.
- Sigma Delta – Increased counter size and adds Fast Detect logic. Not backwards compatible with PRU-ICSS devices.

NOTE: The PRU_ICSSG's RTU_PRU cores do not have any I/Os.

2.6 Interrupt Controller Differences

The basic structure of the interrupt controller is the same on all devices. The INTC mapping framework of mapping system events to channels to hosts is also the same.

All PRU-ICSS devices support the same number of total system events (64, made up of 32 external events and 32 internal events), channels (16), and hosts (10). [Section 4.2](#) shows a detailed comparison of the PRU-ICSS devices; below is an executive summary.

- The INTC system events from modules inside the PRU-ICSS (System Event 0-31) are similar, but not identical, between devices. See [Section 4.2](#) for the specific differences.
- The INTC system events from external sources (System Event 32-63) differ between devices. See [Section 4.2](#) for the specific differences.
- The INTC host assignment the same for most devices, but differs for AM437x, K2G, and AM65x. See [Section 4.2](#) for the specific differences.
- The ARM interrupt numbers mapped to the PRU-ICSS source interrupts are different between devices.

All PRU_ICSSG devices support 160 system events (96 external events and 64 internal events), 20 channels, and 20 hosts. The INTC registers on these devices have been updated to support the increased number of system events.

2.7 Peripheral Differences

2.7.1 PRU-ICSS / PRU_ICSSG UART

The PRU-ICSS UART is identical on all PRU-ICSS and PRU_ICSSG devices.

2.7.2 PRU-ICSS / PRU_ICSSG eCAP

The PRU-ICSS eCAP is identical on all PRU-ICSS and PRU_ICSSG devices.

2.7.3 PRU_ICSSG PWM

PRU_ICSSG devices add a new PWM peripheral. This peripheral is not available on any PRU-ICSS device.

2.7.4 PRU-ICSS / PRU_ICSSG Industrial Ethernet Peripheral (IEP)

The PRU-ICSS / PRU_ICSSG IEP features differ between devices. These feature differences also include updates to the PRU-ICSS / PRU_ICSSG IEP registers. [Table 4](#) summarizes the IEP features that do not appear on every device.

Table 4. IEP Feature Comparison

	AM335x	AM437x	AM570x	AM571x	AM572x SR1.1	AM572 SR2.0	AM574x	K2G	AM65x
IEP timer bit width	32-bit	32-bit	64-bit	64-bit	32-bit	64-bit	64-bit	64-bit	64-bit
Slow compensation mode			√	√		√	√	√	√
Number of compare registers	8	16	16	16	8	16	16	16	16
Programmable reset value		√	√	√	√	√	√	√	√
32-bit shadow mode									√
IEP1 slave mode									√
Selectable capture event source (external or internal)									√

2.7.5 PRU-ICSS / PRU_ICSSG MDIO

The PRU-ICSS MDIO is identical on all PRU-ICSS devices. However, the peripheral has been updated PRU_ICSSG.

2.7.6 PRU-ICSS MII_RT

The PRU-ICSS MII_RT features differ between devices. These feature differences also include updates to the PRU-ICSS MII_RT registers. [Table 5](#) summarizes the features that are only present on select devices.

Table 5. MII_RT Feature Comparison

	AM335x	AM437x	AM570x	AM571x	AM572x SR1.1	AM572 SR2.0	AM574x	K2G	AM65x
TX/RX FIFO levels (RXFLV0/1, TXFLV0/1)		64-bytes	96-bytes	96-bytes	96-bytes		96-bytes	96-bytes	96-bytes
Back to back 32 and 16 TX push			√	√		√	√	√	√
RX_L2 with hardware filter									√
TX_L2 pre-emption FIFO									√
RX classifier with ingress filter									√
RGMII mode									√
SGMII mode									√

The PRU_ICSSG devices add RGMII support. [Table 6](#) summarizes the differences between the MII and RGMII modes in PRU_ICSSG devices.

Table 6. PRU_ICSSG MII and RGMII Feature Comparison

	MI	RGMII
RXIPG0/1	√	
Odd nibble detection and insertion	√	

2.8 Broadside Accelerator Differences

The PRU-ICSS and PRU_ICSSG devices support the following broadside accelerators:

- Scratch Pad:
 - The PRU-ICSS Scratch Pad is identical on all PRU-ICSS devices and backwards compatible on PRU_ICSSG devices. The PRU_ICSSG devices add a new XCHG instruction, which can be used to combine reads and writes to the Scratch Pad into a single instruction.
- Multiplier with optional Accumulation (MPY/MAC):
 - The PRU-ICSS MPY/MAC is identical on AM335x, AM437x, and AM57x. On K2G and AM65x, the carry flag performance was updated.
- CRC module:
 - The PRU-ICSS CRC module is identical on all applicable PRU-ICSS devices. See the [PRU-ICSS / PRU_ICSSG Feature Comparison](#) for which devices include the CRC modules.
 - The PRU_ICSSG CRC module on AM65x adds the CRC16-CCITT polynomial and FIFO to allow 32-byte pushes.

The PRU_ICSSG devices also include additional broadside accelerators and data movement accelerators. See the [PRU-ICSS / PRU_ICSSG Feature Comparison](#) for the full list of accelerators supported on the PRU_ICSSG devices. For PRU_ICSSG devices, TI recommends using the XFR2VBUS and XFR2PSI accelerators for external MMR accesses, instead of LBxO/SBxO, as this minimizes PRU stall cycles.

2.9 Instruction Set and Format Compatibility

The instruction set and format is identical on all devices, with the following exceptions:

- New XCHG instruction on PRU_ICSSG devices
- New Task Swap enable/disable instructions on PRU_ICSSG devices

3 Porting PRU Software Between Devices

The software changes required to port PRU code from one Sitara device to another are based on the hardware differences between the two devices. This section details the key differences in software, and describes how code can be modified from one device to another. Additional modifications may be required relating to other SoC differences that are external to the PRU-ICSS / PRU_ICSSG. Some of these modifications are discussed in the modifying software for SoC-related differences section.

A checklist of typical changes required for both PRU firmware and ARM code is provided in [Table 7](#) and [Table 8](#).

Table 7. PRU Firmware Checklist

1	PRU addresses within global memory map
2	PRU INTC system event numbers
3	PRU peripheral registers
4	PRU accelerator
5	PRU constant table values
6	SoC related changes (peripheral addressing or registers, and so forth)

Table 8. ARM Code Checklist

1	PRU addresses within global memory map
2	PRU INTC system event numbers
3	SoC related changes (peripheral addressing or registers, pinmux configuration, ARM Interrupt Controller, and so forth)

3.1 Updating Global Memory Map References

When porting software, the PRU-ICSS / PRU_ICSSG base address must be updated in both the PRU firmware and ARM code. Most PRU firmware code should use the local memory map to reduce latencies and does not require any modification. Only firmware that accesses the global memory map requires updates. No change is required for any offsets within the PRU-ICSS global memory map.

3.2 Configuring PRU INTC System Events

The PRU INTC on each device has some system event differences. If the existing application uses a system event that has changed, the system events must be updated both in the PRU firmware code and in the interrupt controller mapping in the ARM code.

If an interrupt used is no longer supported on the device being ported to, one option is to poll or periodically read the peripheral's status register, if it exists. For peripheral details, see the device-specific TRM. There are additional latencies when accessing memories outside the PRU-ICSS / PRU_ICSSG.

For AM437x and K2G, the functionality of Host interrupt 7 has changed. Any system events mapped to Host 7 when porting to or from the AM437x should be remapped to Host2-6 or Host8-9. This impacts ARM code and could also impact the PRU firmware (such as if the PRU configures the INTC).

The ARM interrupt controller has also changed with respect to the interrupt numbers mapped to the PRU-ICSS / PRU_ICSSG host interrupts. In the ARM code, the user must confirm that IRQs are updated for the new PRU-ICSS / PRU_ICSSG event numbers.

3.3 Updating PRU Peripheral Registers

Some PRU-ICSS / PRU_ICSSG peripheral MMRs have changed between devices. If using one of these peripherals, then the register references must be updated.

3.4 Updating PRU Constant Table References

Differences in the PRU constant table require changes to the PRU firmware code. The PRU constant table entries are partially backwards compatible, as some peripherals and features maintain the same entry numbers. However, other peripherals and features have been removed, added, or remapped to different entry numbers in the table of the device being ported to. For a comparison between the constant tables on each device, see [Section 4.1](#).

3.5 Modifying Software for SoC-Related Differences

Each device has additional differences at the SoC level that also require changes in both PRU firmware and ARM code. Below is a list of some key differences that require code updates. This is not an exhaustive list.

Common differences between devices requiring PRU legacy code updates include:

- Global device memory map:
 - Start addresses of peripherals and features
 - Base addresses of modules
 - Register addresses and offsets
- Peripherals:
 - Supported peripherals and number of instances
 - Peripherals may have new memory or register maps. The functionality of registers may also change.
- Pinmuxing

4 Appendix– Device Hardware Comparison

4.1 Constant Table Differences

Table 9 shows a comparison of the physical MMR address associated with each Constant Table entry, and Table 10 compares the Peripheral and Memory Regions associated with each Constant Table entry.

Table 9. Comparison of Constant Table MMR Address Mapping

Entry No.	Value [31:0]		
	AM335x / AM437x / AM57x	K2G	AM65x
0	0x0002_0000	0x0002_0000	0x0002_0000
1	0x4804_0000	0x0221_0000	0x0002_F000
2	0x4802_A000	0x0253_0000	0x0002_F100
3	0x0003_0000	0x0003_0000	0x0003_0000
4	0x0002_6000	0x0002_6000	0x0002_6000
5	0x4806_0000	0x2300_0000	0x0002_6100
6	0x4803_0000	0x2180_5400	0x0002_0200
7	0x0002_8000	0x0002_8000	0x0002_8000
8	0x4600_0000	0x2180_4000	0x0002_E100
9	0x4A10_0000	0x0400_0000	0x0003_3000
10	0x4831_8000	0x0250_0000	0x0002_A000 (PRU0) 0x0002_A100 (RTU0) 0x0002_A200 (PRU1) 0x0002_A300 (RTU1)
11	0x4802_2000	0x0253_1000	0x0002_2000 (PRU0) 0x0002_4000 (RTU0) 0x0002_3000 (PRU1) 0x0002_3800 (RTU1)
12	0x4802_4000	0x0253_1400	0x0002_7000
13	0x4831_0000	0x0260_0000	0x0002_C000
14	0x481C_C000	0x0260_B200	0x0002_4800
15	0x481D_0000	0x0260_B400	0x6000_0000
16	0x481A_0000	0x2180_5800	0x7000_0000
17	0x4819_C000	0x0253_0400	0x8000_0000
18	0x4830_0000	0x021D_0000	0x9000_0000
19	0x4830_2000	0x021D_1800	0xA000_0000
20	0x4830_4000	0x000A_E000	0xB000_0000
21	0x0003_2400	0x0003_2400	0x0003_2400
22	0x480C_8000	0x0264_0000	0x0000_8000 (PRU0/RTU0) 0x0000_9000 (PRU1/RTU1)
23	0x480C_A000	0x02A5_0000	0xC000_0000
24	0x0000_0n00, n = c24_blk_index[3:0]	0x0000_0n00, n = c24_blk_index[3:0]	0x0000_0n00, n = c24_blk_index[3:0]
25	0x0000_2n00, n = c25_blk_index[3:0]	0x0000_2n00, n = c25_blk_index[3:0]	0x0000_2n00, n = c25_blk_index[3:0]
26	0x0000_En00, n = c26_blk_index[3:0]	0x0000_En00, n = c26_blk_index[3:0]	0x0000_En00, n = c26_blk_index[3:0]
27	0x0003_2n00, n = c27_blk_index[3:0]	0x0003_2n00, n = c27_blk_index[3:0]	0x0003_2n00, n = c27_blk_index[3:0]
28	0x00nn_nn00, nnnn = c28_pointer[15:0]	0x00nn_nn00, nnnn = c28_pointer[15:0]	0x00nn_nn00, nnnn = c28_pointer[15:0]
29	0x49nn_nn00, nnnn = c29_pointer[15:0]	0x49nn_nn00, nnnn = c29_pointer[15:0]	0x0Dnn_nn00, nnnn = c29_pointer[15:0]
30	0x40nn_nn00, nnnn = c30_pointer[15:0]	0x40nn_nn00, nnnn = c30_pointer[15:0]	0x0Enn_nn00, nnnn = c30_pointer[15:0]

Table 9. Comparison of Constant Table MMR Address Mapping (continued)

Entry No.	Value [31:0]		
	AM335x / AM437x / AM57x	K2G	AM65x
31	0x80nn_nn00, nnnn = c31_pointer[15:0]	0x80nn_nn00, nnnn = c31_pointer[15:0]	0x0Fnn_nn00, nnnn = c31_pointer[15:0]

Table 10. Comparison of Constant Table Peripheral Mapping

Entry No.	Region Pointed To			
	AM335x / AM437x	AM57x	K2G	AM65x
0	PRU-ICSS INTC (local)	PRU-ICSS INTC (local)	PRU-ICSS INTC (local)	PRU_ICSSG INTC (local)
1	DMTIMER2	Reserved	TIMER1	PRU_ICSSG IEP1 (local)
2	I2C1	Reserved	I2C0	PRU_ICSSG IEP1_0x100 (local)
3	PRU-ICSS eCAP (local)	PRU-ICSS eCAP (local)	PRU-ICSS eCAP (local)	PRU_ICSSG ECAP0 (local)
4	PRU-ICSS CFG (local)	PRU-ICSS CFG (local)	PRU-ICSS CFG (local)	PRU_ICSSG CFG (local)
5	MMC0	I2C3	MMC0	PRU_ICSSG CFG_0x100 (local)
6	MCSPi0	Reserved	SPI0	PRU_ICSSG INTC_0x200 (local)
7	PRU-ICSS UART0 (local)	PRU-ICSS UART0 (local)	PRU-ICSS UART0 (local)	PRU_ICSSG UART0 (local)
8	McASP0 DMA	MCASP3_DAT	McASP0 DMA	PRU_ICSSG IEP0_0x100 (local)
9	Ethernet	Reserved	NSSUL	PRU_ICSSG0 CFG (local)
10	Reserved	Reserved	SEC_MGR	TM_CFG (local task manager)
11	UART1	Reserved	UART1	PRU_ICSSG PRU/RTU Control (local)
12	UART2	Reserved	UART2	PRU_ICSSG PA_STATS_QRAM (local)
13	Reserved	Reserved	CIC	PRU_ICSSG PA_STATS_CRAM (local)
14	DCAN0	Reserved	DCAN0 CFG	PRU_ICSSG PROTECT (local)
15	DCAN1	Reserved	DCAN1 CFG	Reserved ⁽¹⁾
16	MCSPi 1	Reserved	SPI1	Reserved ⁽¹⁾
17	I2C2	Reserved	I2C1	Reserved ⁽¹⁾
18	eHRPWM1/eCAP1/ eQEP1	Reserved	EPWM0	Reserved ⁽¹⁾
19	eHRPWM2/eCAP2/ePWM2	Reserved	ECAP0	Reserved ⁽¹⁾
20	eHRPWM3/eCAP3/ePWM3	Reserved	PRU-ICSS0, PRU-ICSS1 IEP (local) + 256MB	Reserved ⁽¹⁾
21	PRU-ICSS MDIO (local)	PRU-ICSS MDIO (local)	PRU-ICSS MDIO (local)	PRU_ICSSG MDIO (local)
22	Mailbox 0	Reserved	Semaphore	RAT SLICE0/1 (local)
23	Spinlock	Reserved	Message Manager Queue Proxy Region5	Reserved ⁽¹⁾
24	PRU-ICSS PRU0/1 Data RAM (local)	PRU-ICSS PRU0/1 Data RAM (local)	PRU-ICSS PRU0/1 Data RAM (local)	PRU_ICSSG PRU0/1 Data RAM (local)
25	PRU-ICSS PRU1/0 Data RAM (local)	PRU-ICSS PRU1/0 Data RAM (local)	PRU-ICSS PRU1/0 Data RAM (local)	PRU_ICSSG PRU1/0 Data RAM (local)
26	PRU-ICSS IEP (local)	PRU-ICSS IEP (local)	PRU-ICSS IEP (local)	PRU_ICSSG IEP (local)

⁽¹⁾ In the AM65x, C15-C20, C23, and C29-C31 can be remapped to any SoC address through the RAT. This can be used to achieve backward compatibility. The AM65x only has 4 RAT regions per PRU_ICSSG slice, so not all of these constant table entries can be remapped concurrently.

Table 10. Comparison of Constant Table Peripheral Mapping (continued)

Entry No.	Region Pointed To			
	AM335x / AM437x	AM57x	K2G	AM65x
27	PRU-ICSS MII_RT (local)	PRU-ICSS MII_RT (local)	PRU-ICSS MII_RT (local)	PRU_ICSSG MII_RT/SGMII0_CFG/SGMII1_CFG (local)
28	PRU-ICSS Shared RAM (local)	PRU-ICSS Shared RAM (local)	PRU-ICSS Shared RAM (local)	PRU_ICSSG Shared RAM (local)
29	TPCC (EDMA)	OCMC_RAM2_CBUF	EDMA_0_CC_CFG	Reserved ⁽¹⁾
30	L3 OCMC0 SRAM	OCMC_RAM	MSMC SRAM	Reserved ⁽¹⁾
31	EMIF0 DDR Base	EMIF1_SDRAM_CS0	DDR3A DATA	Reserved ⁽¹⁾

4.2 Interrupt Controller Differences

Table 11 shows a comparison of system events for event numbers 159-64. These are not applicable for the AM335x, AM437x, AM57x, or K2G.

Table 11. Comparison of System Events [159-64]

Event Number	AM65x		
	PRU_ICSSG0	PRU_ICSSG1	PRU_ICSSG2
159	GPIOMUX_INT31		
158	GPIOMUX_INT30		
157	GPIOMUX_INT29		
156	GPIOMUX_INT28		
155	GPIOMUX_INT27		
154	GPIOMUX_INT26		
153	GPIOMUX_INT25		
152	GPIOMUX_INT24		
151	RESERVED		
150	RESERVED		
149	RESERVED		
148	RESERVED		
147	RESERVED		
146	RESERVED		
145	RESERVED		
144	RESERVED		
143	RESERVED		
142	RESERVED		
141	RESERVED		
140	RESERVED		
139	MCU_MCAN_1_INT_1		
138	MCU_MCAN_1_INT_0		
137	MCU_MCAN_0_INT_1		
136	MCU_MCAN_0_INT_0		
135	USB_1_INT15		
134	USB_1_INT14		
133	USB_1_INT13		
132	USB_1_INT12		
131	USB_0_INT15		
130	USB_0_INT14		

Table 11. Comparison of System Events [159-64] (continued)

Event Number	AM65x		
	PRU_ICSSG0	PRU_ICSSG1	PRU_ICSSG2
129	USB_0_INT13		
128	USB_0_INT12		
127	GPMC_INT		
126	USART_2_INT		
125	USART_1_INT		
124	USART_0_INT		
123	McASP_2_RINT		
122	McASP_2_XINT		
121	McASP_1_RINT		
120	McASP_1_XINT		
119	McASP_0_RINT		
118	McASP_0_XINT		
117	NAVSS_ICSSG0_INT_7	NAVSS_ICSSG1_INT_7	NAVSS_ICSSG2_INT_7
116	NAVSS_ICSSG0_INT_6	NAVSS_ICSSG1_INT_6	NAVSS_ICSSG2_INT_6
115	NAVSS_ICSSG0_INT_5	NAVSS_ICSSG1_INT_5	NAVSS_ICSSG2_INT_5
114	NAVSS_ICSSG0_INT_4	NAVSS_ICSSG1_INT_4	NAVSS_ICSSG2_INT_4
113	NAVSS_ICSSG0_INT_3	NAVSS_ICSSG1_INT_3	NAVSS_ICSSG2_INT_3
112	NAVSS_ICSSG0_INT_2	NAVSS_ICSSG1_INT_2	NAVSS_ICSSG2_INT_2
111	NAVSS_ICSSG0_INT_1	NAVSS_ICSSG1_INT_1	NAVSS_ICSSG2_INT_1
110	NAVSS_ICSSG0_INT_0	NAVSS_ICSSG1_INT_0	NAVSS_ICSSG2_INT_0
109	PCIE1_INT13		
108	PCIE1_INT9		
107	PCIE1_INT8		
106	PCIE1_INT3		
105	PCIE1_INT2		
104	PCIE0_INT13		
103	PCIE0_INT9		
102	PCIE0_INT8		
101	PCIE0_INT3		
100	PCIE0_INT2		
99	SPI_3_INT		
98	SPI_2_INT		
97	SPI_1_INT		
96	SPI_0_INT		
95	I2C_3_INT		
94	I2C_2_INT		
93	I2C_1_INT		
92	I2C_0_INT		
91	ECAP_0_INT		
90	EQEP_2_INT		
89	EQEP_1_INT		
88	EQEP_0_INT		
87	EPWM_5_TZ_INT		
86	EPWM_4_TZ_INT		
85	EPWM_3_TZ_INT		
84	EPWM_2_TZ_INT		

Table 11. Comparison of System Events [159-64] (continued)

Event Number	AM65x		
	PRU_ICSSG0	PRU_ICSSG1	PRU_ICSSG2
83	EPWM_1_TZ_INT		
82	EPWM_0_TZ_INT		
81	EPWM_5_INT		
80	EPWM_4_INT		
79	EPWM_3_INT		
78	EPWM_2_INT		
77	EPWM_1_INT		
76	EPWM_0_INT		
75	PWM_SOCB		
74	PWM_SOCA		
73	ICSSG_2_HOST_INT7	ICSSG_0_HOST_INT7	ICSSG_1_HOST_INT7
72	ICSSG_2_HOST_INT6	ICSSG_0_HOST_INT6	ICSSG_1_HOST_INT6
71	ICSSG_2_HOST_INT5	ICSSG_0_HOST_INT5	ICSSG_1_HOST_INT5
70	ICSSG_1_HOST_INT7	ICSSG_2_HOST_INT7	ICSSG_0_HOST_INT7
69	ICSSG_1_HOST_INT6	ICSSG_2_HOST_INT6	ICSSG_0_HOST_INT6
68	ICSSG_1_HOST_INT5	ICSSG_2_HOST_INT5	ICSSG_0_HOST_INT5
67	MCU_ADC_1_INT		
66	MCU_ADC_0_INT		
65	IPC_INT21	IPC_INT23	IPC_INT25
64	IPC_INT20	IPC_INT22	IPC_INT24

Table 12. Comparison of System Events [63-32]

Event Number	AM335x	AM437x		AM57x	K2G		MII_RT Mode for all PRU- ICSS devices	AM65x
	PRU-ICSS	PRU-ICSS1	PRU-ICSS0	PRU-ICSS1 and PRU-ICSS2	PRU-ICSS1	PRU-ICSS0		All PRU_ICSSG instances
63	TPCC (EDMA) - tpcc_int_pend_po1			System event sources are configurable through the AM57x IRQ_CROSSBAR	EDMACC_1 Region 6	EDMACC_1 Region 7		PRU_ICSSG - Any sd_fd_zero/one_m ax/min(of 72)
62	TPCC (EDMA) - tpcc_errint_pend_po				EDMACC_0 Region 6	EDMACC_0 Region 7		PRU_ICSSG - iep1_sync0_uint_in tr_pend
61	TPTC0 (EDMA) - tptc_erint_pend_po				MSGMGR - Que 59	MSGMGR - Que 61		PRU_ICSSG - iep1_sync1_uint_in tr_pend
60	Mailbox0 - mail_u1_irq				MSGMGR - Que 58	MSGMGR - Que 60		PRU_ICSSG - iep1_latch0_uint_in tr_pend
59	Mailbox0 - mail_u2_irq				MSGMGR - Que 7	MSGMGR - Que 9		PRU_ICSSG - iep1_latch1_uint_in tr_pend
58	Debugss				MSGMGR - Que 6	MSGMGR - Que 8		PRU_ICSSG - iep1_pdi_wd_exp_ pend
57	GPIO0	eHRPWM0-2 Trip Zone	eHRPWM3-5 Trip Zone		BOOT_CFG - IPC_GR12	BOOT_CFG - IPC_GR14		PRU_ICSSG - iep1_pd_wd_exp_p end
56	eHRPWM0-2 Trip Zone	PRU-ICSS0 Host Interrupt 7	PRU-ICSS1 Host Interrupt 7		PRU-ICSS0 Host Interrupt 7	PRU-ICSS1 Host Interrupt 7		PRU_ICSSG - iep1_any_cmp_cap _pend
55	McASP0 TX				BOOT_CFG - IPC_GR11	BOOT_CFG - IPC_GR13	(*_mii1_col & *_mii1_txen) (external pin)	
54	McASP0 RX				CIC - Host Interrupt 102	PWM_SOCB	PRU1_RX_EOF	
53	ADC_TSC				CIC - Host Interrupt 101	PWM_SOCA	MDIO_MII_LINK[1]	
52	UART2				CIC - Host Interrupt 100	CIC - Host Interrupt 87	PORT1_TX_OVERFLOW	
51	UART0				CIC - Host Interrupt 99	CIC - Host Interrupt 86	PORT1_TX_UNDERFLOW	
50	CPSW (c0_rx_thresh_pen d)	CPSW (c2_rx_thresh_pen d)	CPSW (c2_rx_thresh_pen d)		CIC - Host Interrupt 98	CIC - Host Interrupt 85	PRU1_RX_OVERFLOW	

Table 12. Comparison of System Events [63-32] (continued)

Event Number	AM335x	AM437x		AM57x	K2G		MII_RT Mode for all PRU- ICSS devices	AM65x
	PRU-ICSS	PRU-ICSS1	PRU-ICSS0	PRU-ICSS1 and PRU-ICSS2	PRU-ICSS1	PRU-ICSS0		All PRU_ICSSG instances
49	CPSW (c0_rx_pend)	CPSW (c2_rx_pend)	CPSW (c0_rx_pend)	System event sources are configurable through the AM57x IRQ_CROSSBAR	CIC - Host Interrupt 97	CIC - Host Interrupt 84	PRU1_RX_NIBBLE_ODD	
48	CPSW (c0_tx_pend)	CPSW (c2_tx_pend)	CPSW (c0_tx_pend)		CIC - Host Interrupt 96	CIC - Host Interrupt 83	PRU1_RX_CRC	
47	CPSW (c0_misc_pend)	CPSW (c2_misc_pend)	CPSW (c0_misc_pend)		CIC - Host Interrupt 95	CIC - Host Interrupt 82	PRU1_RX_SOF	
46	eHRPWM1	eHRPWM1	eHRPWM4		CIC - Host Interrupt 94	CIC - Host Interrupt 81	PRU1_RX_SFD	
45	eQEP0				CIC - Host Interrupt 93	CIC - Host Interrupt 80	PRU1_RX_ERR32	
44	McSPI0				CIC - Host Interrupt 92	eQEP2	PRU1_RX_ERR	
43	eHRPWM0	eHRPWM0	eHRPWM3-5 Trip Zone		CIC - Host Interrupt 91	eQEP1	(*_mii0_col & *_mii0_txen) (external pin)	
42	eCAP0				CIC - Host Interrupt 90	eQEP0	PRU0_RX_EOF	
41	I2C0				CIC - Host Interrupt 89	EPWM3 TZ	MDIO_MII_LINK[0]	
40	DCAN0 (dcan_intr)				CIC - Host Interrupt 88	EPWM0 TZ	PORT0_TX_OVERFLOW	
39	DCAN0 (dcan_int1)				CIC - Host Interrupt 83	ePWM5	PORT0_TX_UNDERFLOW	
38	DCAN0 (dcan_uerr)				CIC - Host Interrupt 82	ePWM4	PRU0_RX_OVERFLOW	
37	eHRPWM2	eHRPWM2	eHRPWM5		CIC - Host Interrupt 81	ePWM3	PRU0_RX_NIBBLE_ODD	
36	eCAP2				CIC - Host Interrupt 80	ePWM2	PRU0_RX_CRC	
35	eCAP1				I2C0	ePWM1	PRU0_RX_SOF	
34	McASP1 RX	ADC1 (Mag Card)	ADC1 (Mag Card)		SPI1 (level 0)	ePWM0	PRU0_RX_SFD	
33	McASP1 TX	QSPI	QSPI		SPI0 (level 0)	eCAP1	PRU0_RX_ERR32	
32	UART1				QSPI	eCAP0	PRU0_RX_ERR	

Table 13. Comparison of System Events [31-0]

Event Number	AM335x, AM437x, AM57x	K2G, AM65x
31	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[15]_intr_req	
30	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[14]_intr_req	
29	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[13]_intr_req	
28	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[12]_intr_req	
27	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[11]_intr_req	
26	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[10]_intr_req	
25	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[9]_intr_req	
24	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[8]_intr_req	
23	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[7]_intr_req	
22	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[6]_intr_req	
21	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[5]_intr_req	
20	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[4]_intr_req	
19	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[3]_intr_req	
18	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[2]_intr_req	
17	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[1]_intr_req	
16	PRU-ICSS(G) PRU0 or PRU1 - pru_mst_intr[0]_intr_req	
15	PRU-ICSS(G) eCAP - ecap_intr_req	
14	PRU-ICSS(G) IEP - sync0_out_pend	
13	PRU-ICSS(G) IEP - sync1_out_pend	
12	PRU-ICSS(G) IEP - latch0_in (input to PRU-ICSS)	
11	PRU-ICSS(G) IEP - latch1_in (input to PRU-ICSS)	
10	PRU-ICSS(G) IEP - pdi_wd_exp_pend	
9	PRU-ICSS(G) IEP - pd_wd_exp_pend	
8	PRU-ICSS(G) IEP - digio_event_req	
7	PRU-ICSS(G) IEP - iep_tim_cap_cmp_pend	
6	PRU-ICSS(G) UART - uart_uint_intr_req	
5	PRU-ICSS(G) UART - uart_utxevt_intr_req	
4	PRU-ICSS(G) UART - uart_urxevt_intr_req	
3	PRU-ICSS(G) Scratch Pad - xfr_timeout	
2	PRU-ICSS(G) PRU1 Shift Capture - pru1_r31_status_cnt16	
1	PRU-ICSS(G) PRU0 Shift Capture - pru0_r31_status_cnt16	
0	PRU-ICSS Parity Logic - parity_err_intr_pend	PRU-ICSS(G) ECC Logic - ecc_err_intr

Table 14. Host Interrupt Comparison

	AM335x / AM57x	AM437x / K2G	AM65x
Host 1	PRU0/1 R31 bit 30		
Host 2	PRU0/1 R31 bit 31		
Host 3 - Host 6	Device level (i.e. ARM) interrupt controller		
Host 7	Device level (i.e. ARM) interrupt controller	Other PRU-ICSS	Device level (i.e. ARM) interrupt controller
Host 8 - Host 9	Device level (i.e. ARM) interrupt controller		
Host 10	N/A		RTU_PRU0/1 R31 bit 30
Host 11	N/A		RTU_PRU0/1 R31 bit 31
Host 12 - Host 19	N/A		Task Manager

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated