

Triggering ADC Using Internal Timer Events on Hercules MCUs

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ABSTRACT

This application report illustrates how to trigger the on-chip ADCs using various timer events. This allows the inputs to be sampled by the analog-to-digital converters (ADC) in synch with the timer events, which is a critical requirement in control applications. This application report includes an example program that illustrates a way to maximize the sampling rate for a set of three analog input channels, while triggering the ADC with an internally-generated pulse-width modulated (PWM) signal.

This document assumes some basic understanding of the ADC operation as well as some characteristics of the high-end timer (N2HET) and real-time interrupt (RTI) generation module. The code development is done using HALCoGen as the initial code-generation tool.

Source code discussed in this application report and the relevant HALCoGen and Code Composer Studio[™] setup files are available for download from http://www.ti.com/lit/zip/spna227.

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1 Introduction

Hercules[™] Microcontrollers (MCUs) from Texas Instruments (TI) feature peripherals for real-time controlbased applications, including one or two Next Generation High-End Timer (N2HET) timing coprocessors , up to seven Enhanced Pulse Width Modulator (ePWM) modules, up to six Enhanced Capture (eCAP) modules, up to two Enhanced Quadrature Encoder Pulse (eQEP) modules, and one or two 12-bit Analogto-Digital Converters (ADCs). The ADCs have to be triggered at specific and deterministic times with respect to the time base being used for any control loop. This is supported on Hercules MCUs by the provision of a variety of "trigger conditions" that control the start of sampling of an analog input by the ADC(s).

2 ADC Trigger Options

The ADC module on Hercules MCUs supports three conversion groups: event group (or group0), group1 and group2. The available analog input channels can be selected for conversion in one or more of these conversion groups. All channels selected in a particular conversion group share some basic characteristics such as sample time, data format, and the trigger condition. Group0 can only be triggered by an edge on the selected trigger signal, while group1 and group2 are software-triggered by default. Group1 and group2 can also be configured to be edge-triggered. Table 1 summarizes the options for triggering any of the three conversion groups using an edge-trigger signal. This table is applicable to the RM46x MCUs. A similar table can be found inside each device-specific data sheet. The table lists the trigger signal as well as the control registers setting that is required to select that trigger signal.

		Trigger Event Signal					
Group Source Select, G1SRC,	Event No	PINMMR30[0] = 0 and PINMMR30[1] = 1					
G2SRC or EVSRC		PINMMR30[0] = 1 (default)	Option A	Control for Option A	Option B	Control for Option B	
000	1	AD1EVT	AD1EVT	—	AD1EVT	—	
001	2	N2HET1[8]	N2HET2[5]	PINMMR30[8] = 1	ePWM_B	PINMMR30[8] = 0 PINMMR30[9] = 1	
010	3	N2HET1[10]	N2HET1[27]	—	N2HET1[27]	—	
011	4	RTI Compare 0 Interrupt	RTI Compare 0 Interrupt	PINMMR30[16] = 1	ePWM_A1	PINMMR30[16] = 0 PINMMR30[17] = 1	
100	5	N2HET1[12]	N2HET1[17]	—	N2HET1[17]	—	
101	6	N2HET1[14]	N2HET1[19]	PINMMR30[24] = 1	N2HET2[1]	PINMMR30[24] = 0 PINMMR30[25] = 1	
110	7	GIOB[0]	N2HET1[11]	PINMMR31[0] = 1	ePWM_A2	PINMMR31[0] = 0 PINMMR31[1] = 1	
111	8	GIOB[1]	N2HET2[13]	PINMMR32[16] = 1	ePWM_AB	PINMMR31[8] = 0 PINMMR31[9] = 1	

Table 1. MIBADC1 Event Trigger Hookup



2.1 Triggering ADC1 Using N2HET1[27] on RM46x MCUs

2.1.1 Selecting Trigger Condition

This section describes how to setup the ADC1 and N2HET1 modules so that a rising edge on N2HET1[27] can be used to periodically trigger ADC1 group1 conversions. The configuration is entirely done using HALCoGen, as described below.

ADC1 General Al	DC1 Group Event	ADC1 Group 1	ADC1 Group 2	ADC1 Memory	ADC1 Port
-ADC1 Group 1 Con	figuration				
FiFo	Size: 32	¥1	Channel Id in Conve		
Data Resolution	(Bit): 12_BIT		Continuous Conversi	on	
- ADC1 Group 1 Trig	The second second second second second	INCOME. IN		\sim	6
EVENT 1	Default Trigger	Rising I	Edge	Hardware	
HET1_27					🍽 Trigger
		and a second sec		- 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000 - 1000	
EVENT	Alternate Trigger	Falling	Edge SW Trigger	Software	
EVENT	Alternate Trigger	Falling	Edge SW Trigger	Software	
EVENT HET2_5 HET1_27 RTI_COMP0		10.000000	Edge SW Trigger	Software	
EVENT HET2_5 HET1_27	npling tExter	nded		Software	, PAESA
EVENT HET2 5 HET2 5 RTL_COMP0 HET1_17 HET1_19 HET1_11	nplingtExter	nded	Edge SW Trigger		, ALCAR
EVENT HET2 5 HET1 27 RTI_COMP0 RTI_COMP0 RTI_COMP0 RTI_17 HET1_17 HET1_19 HET1_11 HET2_13	npling tExter	nded harge tSample			, ALSA
EVENT HET2 5 HET1 27 RTL COMP0 HET1_17 HET1_17 HET1_19 HET1_11 HET2_13 EPWM_B EPWM_A1	npling Start: tDiscl	nded harge tSample	ItConversion	End:	PALSA
EVENT HET2 5 HET1 27 RTI_COMP0 RTI_COMP0 RTI_COMP0 RTI_17 HET1_17 HET1_19 HET1_11 HET2_13 EPWM_B EPWM_A1 HET2_1	npling Start: tDiscl	nded harge ItSample harge Discharge	ItConversion	End:	

Figure 1. ADC1 Group1 Trigger Selection

As shown in Figure 1, group1 is configured to be triggered by a falling edge on N2HET1[27]. HALCoGen generates the C source code to configure the PINMMRnn registers to achieve this. No external connection is required between the N2HET1 and the ADC1 modules, as this trigger signal connection is already made internally. You can choose the enable the output of the N2HET1[27] signal onto the 144QFP pin # 4 by configuring the "PINMUX" tab in HALCoGen. On the 337BGA package, the N2HET1[27] signal is always output on ball # A9. Enabling this output allows you to identify the timing of the ADC trigger, which is very useful during code development.

2.1.2 High-End-Timer Program to Generate Trigger Signal

Consider the following simple HET program:

L00 CNT {reg=A, max=374, data=0} L01 ECMP {next=L00,hr_lr=HIGH,en_pin_action=ON,pin=27,action=PULSELO,reg=A,data=187,hr_data=0}

The above code sets up a counter that counts from 0 to 374 repeatedly. Whenever this counter becomes 187, a low level is driven onto the N2HET1[27] signal. This signal is automatically driven high (opposite state) when the counter becomes zero.

This simple HET program is sufficient to generate the periodic falling edges required to trigger the ADC1 group1 as per the setup described in Section 2.1.1.

This HET program needs to be assembled so that a set of files is created. This includes a .c and a .h file that need to be included in the higher-level Code Composer Studio (CCS) project.



2.1.3 Host Program

HALCoGen makes it really easy to write the main driver program by creating the individual driver code for the ADC1 and N2HET1 modules. In this case, the main program is simply:

```
void main(void)
{
    adcInit();
    adcStartConversion(adcREG1, adcGROUP1);
    hetInit();
    while(1);
}
```

The adcInit() function sets up the ADC1 module's group1 to be triggered by a falling edge on N2HET1[27].

The *adcStartConversion()* function configures the channels selected for conversion in ADC1 group1. Now the ADC1 is ready for conversions as soon as the correct trigger condition occurs on the N2HET1[27] signal.

The *hetInit()* function sets up the N2HET1 module, copies the simple HET program from program flash into the N2HET1 program RAM, and starts execution of the HET program.

That is all that is required to demonstrate triggering of ADC group1 using a selected edge on N2HET1[27]. You are free to write the other parts of the code to either generate a DMA request or an interrupt request to read out the conversion results. The accompanying source code example uses a DMA request to transfer the conversion results to the CPU RAM and then interrupt the CPU so that the conversion results can be processed.

3 References

- HET Integrated Development Environment User's Guide (SPNU483)
- NHET Getting Started (SPRABA0)
- RM46L852 16- and 32-Bit RISC Flash Microcontroller Data Sheet (SPNS185)
- RM46x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (SPNU514)

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