Application Report
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Use of All 1's and All 0's Valid in Flash EEPROM Emulation

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ABSTRACT

The Texas Instruments Hercules™ ARM® Safety MCUs built using TI's F021 Flash process typically have one bank of Flash for emulating electrically erasable programmable read-only memory (EEPROM). This Flash is protected by single error correction double error detection (SECDED) error correcting code (ECC) bits. There is an additional feature to allow fully erased (all 1's) or fully programmed (all 0's) to be valid values. This additional feature may compromise the integrity of the SECDED scheme. While the risk is small, it needs to be understood by the system designer.

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1 Background

To understand the impact of the "All 1's Valid" and "All 0's Valid" features, review the nature of the SECDED codes.

TI has protected the Flash memory by adding 8 ECC bits to every eight bytes (64 bits) of data. These ECC bits are stored in a separate address range of the memory, but are erased at the same time as the data they protect. These 8 ECC bits provide a Hamming distance of 4. The Hamming distance is the number of bits that must change from one valid number to create another valid number. A simple graphical one-dimensional example is shown in Figure 1:

Figure 1. Hamming Distance Example

In this example, states B and F are valid numbers, but states A, C, D, E and G are invalid numbers. A single bit error in state B could result in moving to state C or A. A single bit error in state F could result in moving to state E or G. If in state A or C, it is assumed to be caused by a single bit error. The error is corrected taking you back to the nearest valid state, state B. A double bit error in state B might take you to state D. Similarly a double bit error in state F could take you to state D. You know that the number is incorrect, but cannot determine how to correct the error. This is the basic concept behind single bit error correction and double bit error detection.

Now what happens when there are three errors? If you start in state B, after three errors you could be at state E. State E is only a one bit distance from state F and would be erroneously corrected to state F. With a SECDED scheme, a triple bit error may be erroneously corrected. Of course the probability of getting a three bit error within a single group of 72 bits is very small. However, if detecting the very unlikely triple bit errors is more important than correcting the single bit errors, then the device can be set to error detection mode only.

A four bit error from state B can take you to state F. Since state F is also a valid state, there is no way to detect that errors occurred. The fewest number of bits that have to change from one valid state to reach another valid state defines the Hamming distance. In this simple example, just as in the TI ECC scheme, the Hamming distance is four.

2 EFFECT of Address in ECC

Using 8 ECC bits with each 64 bits of data provides the minimum 4 bit Hamming distance required for SECDED. The 8 ECC bits can actually provide SECDED for more than 64 bits. TI makes use of the extra coverage space by also including 19 address lines into the ECC calculation. This helps detect an error of the address lines inside of the Flash memory. When the ECC detects even a single bit error in the address lines, it treats the data read as an uncorrectable error; the data may be from the wrong address. The side affect is that the 8 bit ECC value of a given 64 bit data value will change based on the address.

Table 1. Example ECC Values

Address	Data	ECC
0xF0200000	0xFFFFFFFF 0xFFFFFFFF	0x45
0xF0200008	0xFFFFFFFF 0xFFFFFFFF	0xDB
0xF0200010	0xFFFFFFFF 0xFFFFFFFF	0xD4

3 Use of All 1's Valid

Flash memory is used to emulate EEPROM memory as a way to reduce system costs. The time to program (change a 1 to a 0) or erase (change a 0 to a 1) EEPROM is roughly the same. Most external EEPROMs will do both operations at a single request, thus, the speed is often limited by the time to serially scan the information to the EEPROM device. In Flash memory, you can program individual bits relatively quickly, but must erase all of the bits within a sector at one time. The time to erase is much longer than the time to program. Therefore, most routines that emulate EEPROM memory in Flash use larger amounts of Flash memory and implement a linked list to keep track of updating data values. Once a sector of Flash is filled with updated entries on the linked list, the newest entries are copied to another sector and then the first sector can be erased when there is time available.

The use of the linked list requires that after power on, or a reset, the program determine the address of the next available blank Flash location. When the Flash memory is protected by ECC, this is complicated by the fact that erased Flash will usually not have valid ECC bits as seen in Table 1. When the address is used in the ECC calculation, then reading most erased locations will create uncorrectable errors, reading some erased locations will create an incorrect single bit correction and reading a very few locations will create no error.

To avoid getting ECC errors when searching for the first truly blank location, TI has added a feature that allows the state of all 1's (64 data bits and all 8 ECC bits to be 1) to be a valid value. This feature is only available for the Flash EEPROM emulation (FEE) bank. It solves the problem of getting unwanted single and double bit errors, but it has some side effects that need to be understood.

With address in the ECC calculation, the all 1's condition occurs at different places in the Hamming distance at different addresses. At approximately 0.4% of the addresses, a data pattern of 63 ones and one zero have an ECC code of 0xFF. At these addresses, if that one zero bit fails, the failure would not be corrected if "All 1's Valid" is enabled. Likewise, about 0.4% of all addresses give an ECC value of 0xFF with a data pattern of 62 ones and two zeros. If both zeros fail at this location, the failure will not be detected when "All 1's Valid" is enabled.

So what are the probabilities of masking a single or double bit failure with "All 1's Valid"?

P_{MSBF} = Probability of masking a single bit failure
P_{OBF} = Probability of any one bit failing
P_{ASBF} = Probability that any address has 0xFF for ECC value of 63 ones and one zero
P_{ASBF} = 0.004
P_{SBZ} = Probability that the data matches the pattern of one zero and 63 ones that gives an ECC value of 0xFF
$P_{SBZ} = 1/2^{64} = 5.4 \times 10^{-20}$
N = Number of data bits in the EEPROM emulation memory space

$$P_{MSBF} = P_{OBF} \times N \times P_{ASBF} \times P_{SBZ}$$
$$P_{MSBF} = P_{OBF} \times N \times 0.004 \times 5.4 \times 10^{-20}$$
$$P_{MSBF} = P_{OBF} \times N \times 2.16 \times 10^{-22}$$

To give a feel for the actual probability, start with an assumed single bit failure probability (P_{OBF}) of 1 in 25,000,000,000,000. This would give a DPPM level of 1 defective part per million for a 3MB Flash device. This failure rate is being used only for illustrative purposes and is not representative of any particular part or technology. Also assume an EEPROM emulation bank of 64KB of data, or 524,288 bits. The probability of not correcting a single bit failure in the FEE memory (P_{MSBF}) would be equal to the probability of a single bit failure (P_{OBF}) times the number of bits in the FEE bank (N) times the percentage of addresses that have 0xFF for ECC with 63 1's (P_{ASBF}), times the probability of having that particular pattern (P_{SBZ}).

$$P_{MSBF} = \frac{1}{25 \times 10^{12}} \times 524288 \times 0.004 \times 5.4 \times 10^{-20}$$

$$P_{MSBF} = 4.5 \times 10^{-30}$$

The probability of failing to identify a double bit error due to using "All 1's Valid" is even smaller since you square the probability of the single bit error failure.

P_{MDBF} = Probability of masking a double bit failure

$$P_{MDBF} = (P_{OBF})^2 \times N \times 2.16 \times 10^{-23}$$

Using the example above, the probability of not detecting a double bit failure due to using "All 1's Valid" is shown below:

$$P_{MDBF} = \left(\frac{1}{25 \times 10^{12}}\right)^2 \times 524288 \times 2.16 \times 10^{-23}$$

$$P_{MDBF} = 1.8 \times 10^{-44}$$

While these probabilities are small, they are not zero. However, with some simple precautions you can avoid having this unlikely happenstance causing a problem in the application.

4 Recommendations

There are three situations where it is tempting to use the ‘All 1’s Valid” feature. The first is when verifying that a sector is blank, either after a reset, or after an erase. To accomplish this it is better to use one of the four Error Detection Sector Disable Registers (FEDACSDIS) to disable the ECC detection and correction for the sector you are checking for blank. This way accesses to other sectors that may contain valid FEE data are not affected. Remember to check that both the data and the ECC bits are all blank.

The second scenario for using “All 1’s Valid” is after reset when you are trying to determine which sector contains the valid data. Typically each Flash sector used for EEPROM emulation has a sector status word at the beginning of the sector. The status may be *old data waiting to be erased*, *currently in use*, *being updated with latest data* or *erased ready for new data*. None of these state variables should be all 1’s. However, it is possible that a device was reset or powered down after a sector was erased, but before the *erased ready for new data* status was written. In this case, since erase is a relatively long operation, the sector may only be partially erased. It is best to have in the data abort routine, code to identify that the error occurred while reading the FEE sector status word. The error can be ignored, but then the sector should be re-erased to assure the erase is complete.

The third scenario is trying to determine the first empty location in the sector containing the active link list. The best way to do this is to traverse the list for each data entry in the list, and keep track of the highest address used. This way you also verify that all the links are still working. After you identified the entry at the highest address, you add to that address the additional number of bytes for that entry’s data, if any. Then the next location should be blank. Enable “All 1’s Valid” before reading this location. It is possible that this location is not blank. If the power down or reset occurred after an entry was updated, but before the link to the new data was update, then this location may not be blank. In that case, check each block of 8 bytes after that location to identify the first blank location. Save that address in RAM for your FEE driver software to use as the starting point for updates to your linked list. Once you have found this starting point, turn off “All 1’s Valid”.

It is important when designing the data record header for your linked list that a value of 64 bits all 1 is not a valid record header. This can be done by designating a *record valid* bit, or if a record index is included in the header, not using the maximum (all 1’s) index number. You can further assure that a valid record header is not mistaken for a blank location when a single bit error is present by making sure a valid record header has at least two bits that are zero.

5 All 0’s Valid

An all zeros valid feature also exists for the FEE bank. It was designed to allow any location to be programmed to all zero bits (64 bits of data and 8 bits of ECC all zero) and not create an ECC error. The all zeros valid feature has the same limitations as the all ones valid feature. The all zeros valid feature is not required in implementing a linked list using TI’s Hercules MCUs.

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