

Clock jitter analyzed in the time domain, Part 3

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Introduction

Part 1 of this three-part article series focused on how to accurately estimate jitter from a clock source and combine it with the aperture jitter of an ADC.¹ In Part 2, that combined jitter was used to calculate the ADC's signal-to-noise ratio (SNR), which was then compared against actual measurements.² This article, Part 3, shows how to further increase the SNR of the ADC by improving the ADC's aperture jitter, with a focus on optimizing the slew rate of the clock signal.

As shown in Parts 1 and 2, a bandpass filter on the clock signal is a key component for achieving an ADC's data-sheet SNR values. The far-end phase noise of the clock signal adds a substantial amount to the total jitter of the clock signal, causing the SNR to degrade even faster at higher input frequencies.

Unfortunately, there are two major disadvantages associated with the bandpass filter. The first is that it not only removes the clock signal's far-end phase noise, it also eliminates the higher-order odd harmonics of the fundamental clock frequency, turning a square wave into a sine wave. These odd harmonics (third, fifth, etc.) are essential for achieving a fast slew rate to minimize the ADC's aperture jitter. The second disadvantage of the bandpass filter, depending on topology and order, is that it has some loss associated with it that can typically range anywhere from 1 to 9 dB. This

Figure 20. SNR versus clock amplitude versus input frequency (from ADS54RF63 data sheet)

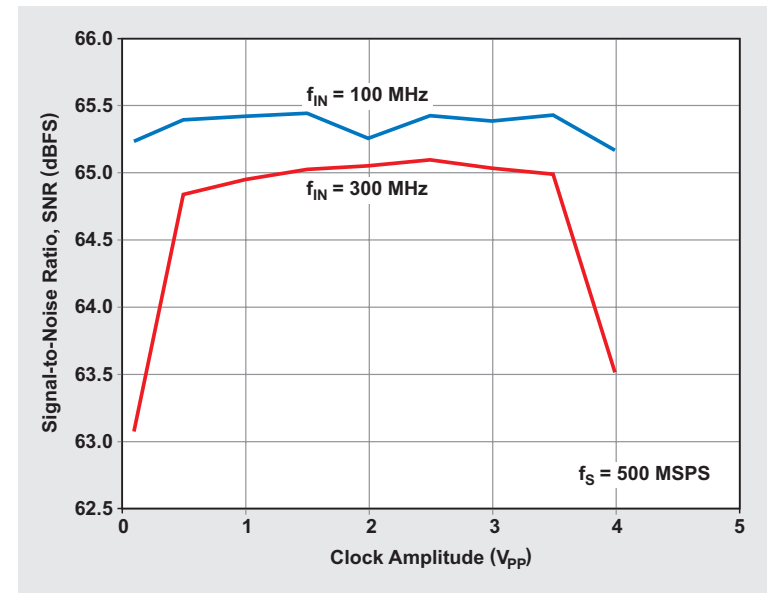
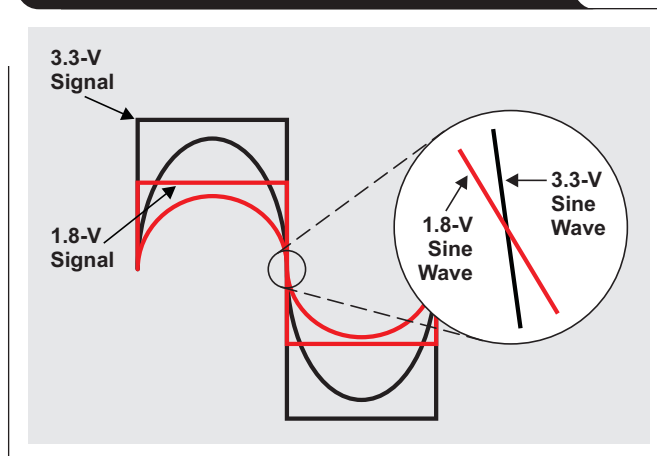


Figure 21. Bandpass-filter input and output with 1.8-V and 3.3-V logic



loss is equivalent to attenuating the clock amplitude and thus reducing the slew rate of the clock signal even further.

The slew rate's impact on an ADC's SNR performance is often shown in the ADC's data sheet as SNR plotted versus clock amplitude, as in Figure 20. This figure, taken from the Texas Instruments (TI) ADS54RF63 data sheet,³ shows that the larger the clock's amplitude is, the larger its slew rate will be. Figure 20 also demonstrates that, as expected, the SNR sensitivity to the clock's slew rate increases as the input frequency, f_{IN} , increases. However, the plot also indicates that overdriving the clock input too much may actually cause clipping or damage inside the ADC, negatively impacting the SNR.

In an effort to lower the intrinsic noise and reduce the power consumption, manufacturers produce clock-distribution ICs with smaller process nodes and consequently lower power-supply rails. For example, it is much more difficult to generate a fast-slew-rate clock signal from a 1.8-V device than from a 3.3-V device; and the loss from the bandpass filter only makes this deficiency worse (see Figure 21).

The remainder of this article focuses on two practical ways to maximize the slew rate of the filtered clock signal in real applications by trying to "restore" the removed clock harmonics. Essentially, the clock edges need to be

squared up again, and the signal swing needs to be increased as much as possible to compensate for the loss from the bandpass filter (BPF). Both tasks can be accomplished by increasing the signal gain through either an active or a passive circuit (see Figure 22). Both options have advantages and disadvantages, all of which will be discussed next along with the key considerations for making a selection.

Using a low-noise amplifier for active gain

System designers often don't want to use active gain because it adds noise to the system and consumes extra power. However, in some cases it may be the only option, as (for example) when the design uses a high clock frequency that exceeds the bandwidth of the step-up transformer.

There are several parameters the system designer needs to consider when selecting the amplifier:

Bandwidth specification—There are a lot of RF amplifiers available, but very few extend down to intermediate frequencies (<250 to 500 MHz). The noise figure of standard CMOS amplifiers isn't low enough to be considered (<2 dB), so the best practice is to choose an RF amplifier. The amplifier's usable bandwidth needs to be wide enough to include at least the third and preferably the fifth harmonic of the fundamental clock frequency. Therefore, an amplifier for a 122.88-MHz clock needs to cover at least 368.64 MHz, and for a 500-MHz clock at least 1.5 GHz.

Noise figure—To minimize the additional noise contribution of the low-noise amplifier (LNA), its noise figure

Figure 22. Addition of circuitry to boost slew rate

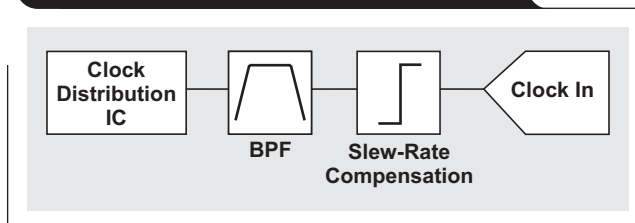
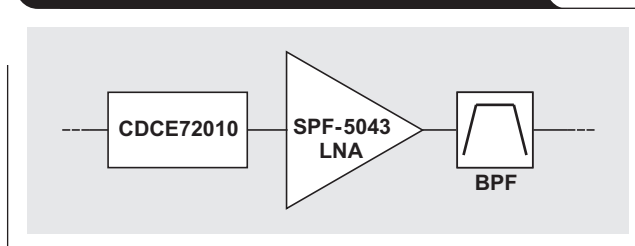
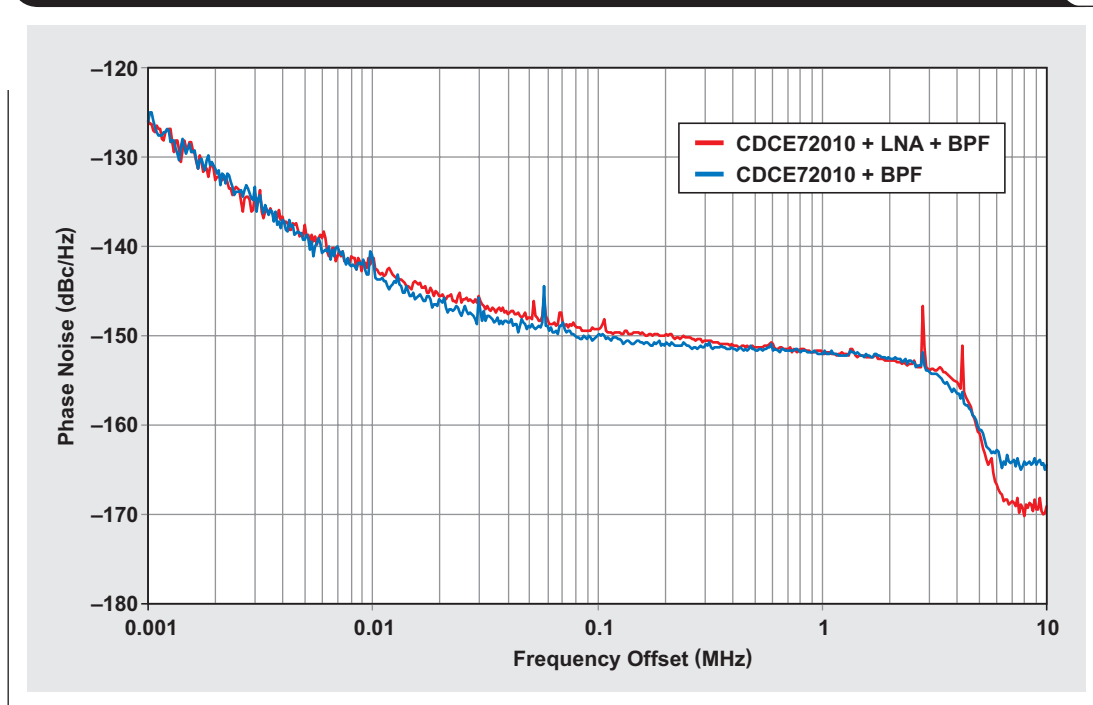


Figure 23. Low-power LNA compensates for BPF losses



should be at least 2 dB or better. Most LNAs, even with low noise figures, add broadband noise to the clock signal. Hence the LNA should be placed between the clock-distribution device and the bandpass filter (BPF) (see Figure 23) to limit the amount of extra noise (see Figure 24). (The TI CDCE72010 used for Figures 23 and 24 is the clock synchronizer used in the examples in Part 2 of this

Figure 24. LNA slightly degrades clock signal's phase noise inside BPF's pass band



article series.) Better noise figures typically require more power consumption, which may set some practical limits to the amplifier search.

P1dB compression point—The P1dB compression point essentially defines the maximum possible output swing. To achieve a clock signal of about $2 V_{PP}$, the P1dB needs to be at least 10 dBm.

Voltage rail—The voltage rail of the amplifier can be used to avoid exceeding the maximum voltage rating of the ADC's clock pins. However, for maximum performance, a new voltage rail may be necessary, adding cost and board space to the system.

Stability—A low-loss LC bandpass filter has a high reactance. RF LNAs are designed to ideally drive a resistive 50- Ω load, so driving a reactance may cause instability or distortion with additional unwanted spurs, which may require a matching network.

Gain—Even though the LNA is operated with high gain (>10 to 12 dB) similar to a comparator, the research in conjunction with this article showed that pure comparators are not suitable for this function. They add too much noise to the output signal, and most often their slew rate is not fast enough.

Part 2 described the example of the CDCE72010 clock synchronizer driving the TI ADS54RF63 and ADS5483 ADCs with a sampling frequency of 122.88 MSPS. The SPF-5043 LNA from RF Micro Devices was evaluated as a suitable amplifier for this example (see Figure 23). In an effort to keep the additional power consumption from the LNA to a minimum, the amplifier was operated from a 3.3-V supply and the quiescent current was measured at about 41 mA, or a power consumption of about 131 mW.

The SPF-5043 data sheet lists the following specifications:

- Usable bandwidth extends down to 100 MHz
- Noise figure = 0.6 dB
- P1dB = ~19 dBm
- Gain = ~22 dB

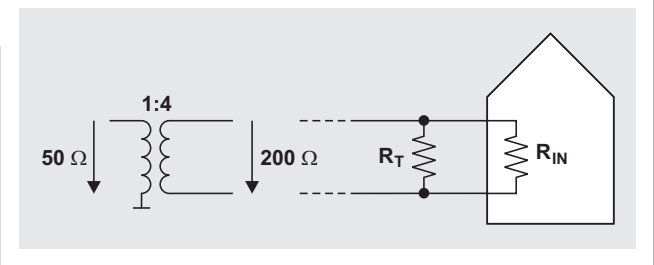
Even though the LNA's noise figure is really low, the SNR performance was better when the LNA was placed before the bandpass filter instead of following it.

The maximum output voltage of the SPF-5043 is limited by the 3.3-V voltage rail. However, when a step-up transformer is used to convert the signal from single-ended to differential, additional measures may be necessary to avoid exceeding the maximum voltage rating of the ADC's clock inputs.

Using a step-up transformer for passive gain

The easiest way to improve the slew rate of the clock signal is by means of a step-up transformer. Since it is a passive component, it doesn't add extra noise or increase power consumption. In power-sensitive or portable applications, a transformer-based solution may be the only practical

Figure 25. Step-up transformer changes input impedance



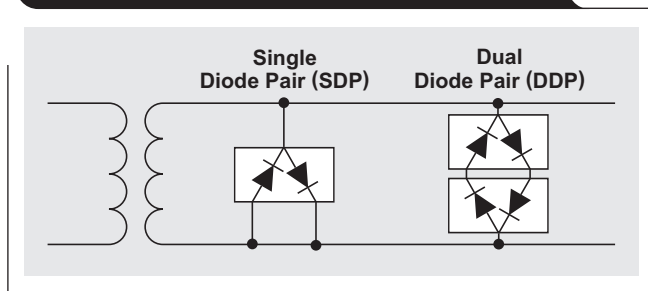
choice; and oftentimes a transformer may already be used in the clock path to convert a clock input from single-ended to differential. However, there are some applications where a step-up transformer is not practical and the following parameters need to be considered:

Bandwidth requirement—Transformers themselves have the frequency response of a bandpass filter. The magnetic coupling between input and output gets weaker as the frequency gets close to DC, and at higher frequencies the transformer parasitics such as inner-winding capacitance and leakage inductance are starting to dominate. The pass-band bandwidth of off-the-shelf transformers is typically less than that of a wideband LNA such as the SPF-5043, and the upper frequency limit decreases as the step-up ratio increases (1:8 versus 1:4).

Impedance transformation and transformer

impedance ratio—Besides increasing the output voltage, the step-up transformer also changes the input impedance. For example, a transformer with a 1:4 impedance ratio changes a 50- Ω source into a 200- Ω source impedance (see Figure 25). Therefore, the ADC clock's input impedance needs to be considered when the transformer impedance ratio is selected, because it is in parallel with the clock's input termination (R_T). For example, if the ADC clock's input impedance is only 200 to 300 Ω , then a 1:8 step-up transformer—even without any termination—would present a 25- to 40- Ω load to the clock source. This is a significant load that may keep the clock source from generating as high a swing because it can't source enough output current.

Maximum voltage swing—The step-up transformer can easily generate output voltages larger than 5 V, quickly exceeding the maximum voltage ratings of the ADC's clock input. A 5-V converter typically has a maximum input voltage of about 5.5 V, while a 3.3-V converter may tolerate a maximum of only about 3.6 V. Exceeding the maximum voltage rating of the ADC reduces its life span and may even result in catastrophic failure due to electrical overstress. Although the clock input typically is protected with ESD diodes, it is not good practice to rely solely on them. A better alternative for protecting against electrical overstress may be to employ external clipping diodes.

Figure 26. Using clipping diodes to protect ADC inputs**Using Schottky clipping diodes**

Using clipping diodes is a common way to protect the data converter's inputs from exceeding the maximum voltage rating. Because low-capacitance Schottky diodes, such as the HSMS-2812 from Avago Technologies, can maintain fast slew rates, they are well-suited for RF and high-speed applications. The HSMS-2812 has a forward voltage of 410 mV. Using a pair of anti-parallel diodes (see Figure 26) creates a differential clipping voltage of ± 410 mV (820 mV_{PP}). For ADCs that require a higher clock amplitude, two pairs of anti-parallel diodes can be placed back-to-back, doubling the clipping voltage to ± 820 mV (1.64 V_{PP}).

Figure 27 shows the filtered LVCMOS output of the CDCE72010 that results when a 1:4 transformer is used

with and without a single diode pair (SDP). Also shown is the output for when a 1:8 transformer is used with an SDP or a back-to-back dual diode pair (DDP). It can be seen that with the 1:4 transformer, the SDP reduces the sine-wave amplitude from about 1.6 to 0.9 V_{PP}. However, the clipped output waveform no longer resembles a pure sine wave but looks instead like a square wave.

It is interesting to note that when the SDP configuration is used, there doesn't seem to be an amplitude difference between using the 1:4 or the 1:8 transformer, although the waveform for the latter appears to have a slightly faster slew rate. For the DDP configuration with the 1:8 transformer, the output amplitude is about 1.6 V_{PP} with a little better slew rate around the zero crossing point.

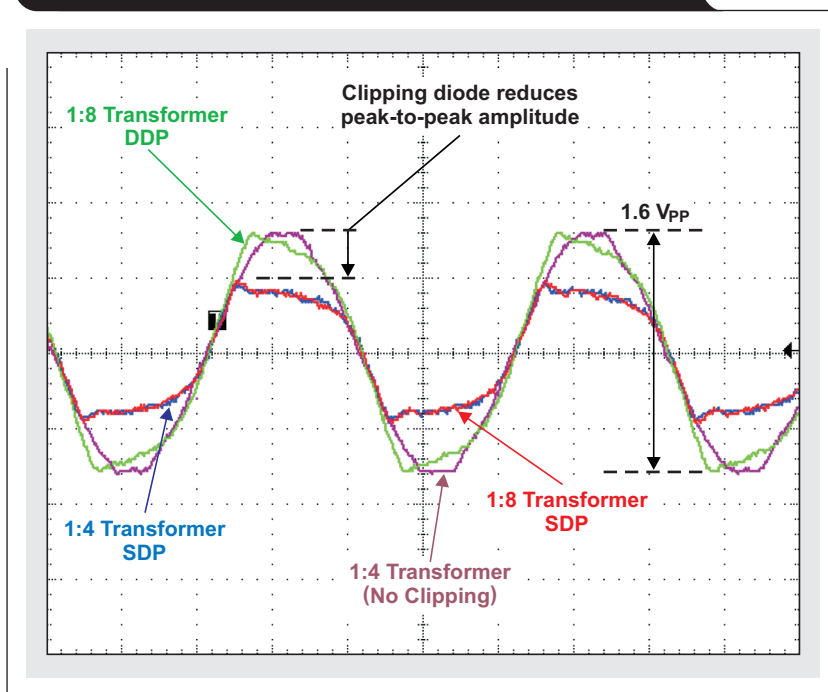
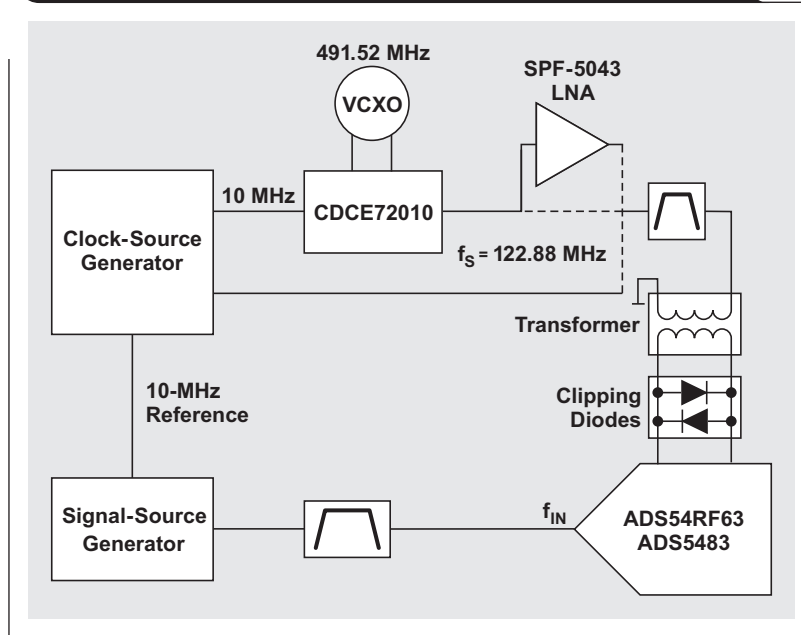
Figure 27. Clock signal with different transformer and clipping-diode configurations

Figure 28. Setup for testing different active- and passive-gain circuits

SNR measurements

An investigation was conducted to see whether the ADC's aperture degradation due to the external clock's slew-rate limitation could be improved. Different configurations using step-up transformers, an SPF-5043 LNA, and clipping diodes were tested to maximize the ADC's SNR when a realistic clocking solution such as the CDCE72010 was used (see Figure 28) rather than a low-jitter clock-source generator.

As highlighted in Part 2 of this article series, the filtered LVCMOS output of the CDCE72010 has about 90 fs of clock jitter, while the clock-source generator has only about 35 fs. Although the clock-jitter difference prevents the CDCE72010 from ever achieving the same SNR as when the clock-source generator is used, the goal was to find a configuration to reduce the resulting SNR gap as much as possible. The ADS54RF63 ADC was used with a sampling frequency (f_s) of 122.88 MSPS and an input frequency (f_{IN}) of 1.0 GHz. The ADS5483 ADC was also used,

with the same value for f_s but with an f_{IN} of 100 MHz.

The following different parameters were examined:

- Use of an LNA to boost the output voltage and slew rate of the CDCE72010
- Step-up transformers with ratios of 1:1, 4:1, 8:1, and 16:1 (Coilcraft WBC series and Mini-Circuits ADT series)
- Avago's HSMS-2812 clipping diodes—either SDPs or back-to-back DDPs in anti-parallel configuration

Measurements for ADS54RF63

The default configuration for the ADS54RF63 evaluation module (ADS54RF63EVM) used a Coilcraft WBC4-1 step-up transformer, and the baseline SNR was about 60.7 dBFS when the low-jitter clock-source generator was used. If the CDCE72010 with the LVCMOS output was used as the clock source instead, the SNR dropped to 57.8 dBFS. However, with only about 90 fs of clock jitter, an SNR better than about 60 dBFS should theoretically be attainable, so there was room for at least a 2.2-dB improvement.

Figure 29. Measured SNR of different clock-input configurations using ADS54RF63 with $f_S = 122.88$ MSPS and $f_{IN} = 1$ GHz

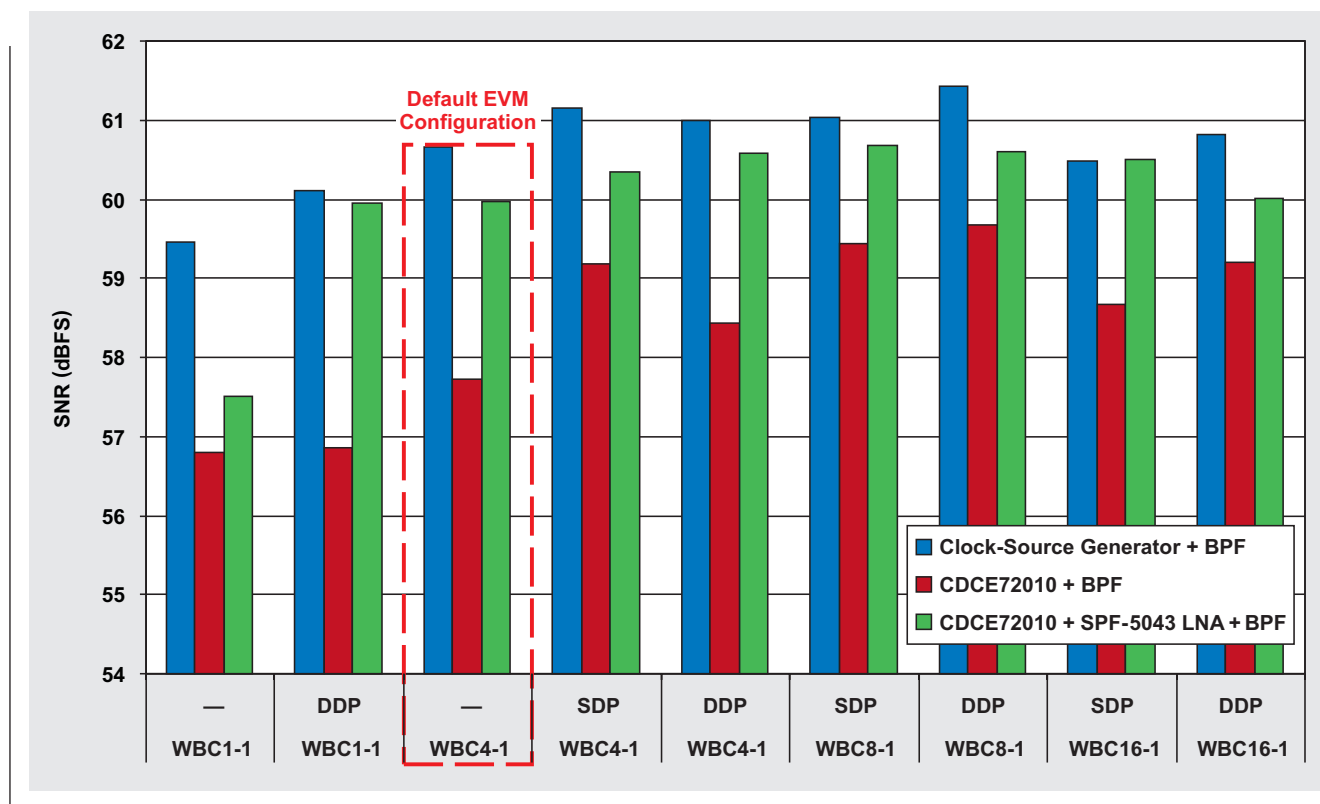
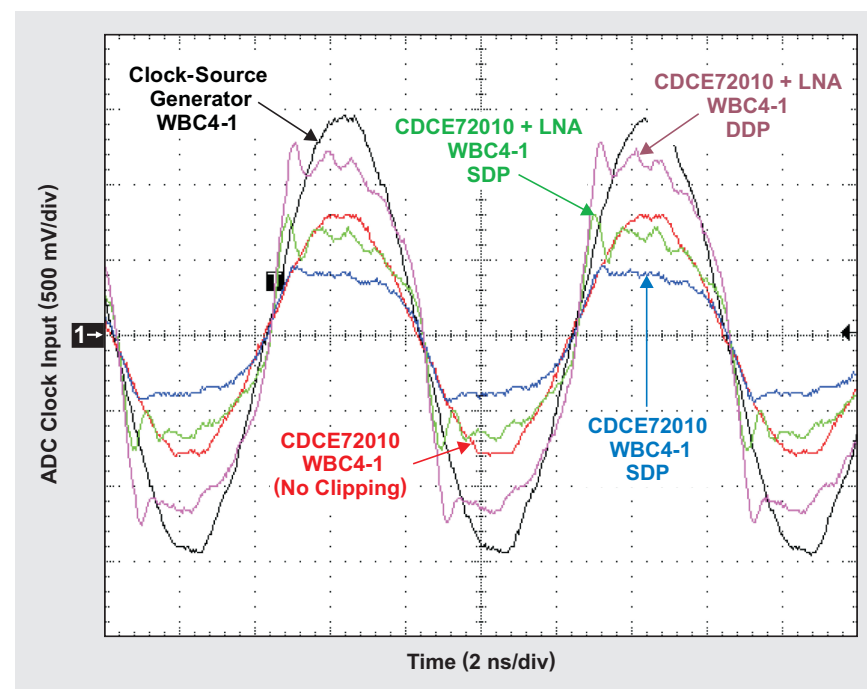


Figure 29 shows the different EVM clock-input configurations along with the measured SNR values of the ADS54RF63. It can be seen that the clipping diodes alone seemed to improve the SNR with the default WBC4-1 step-up transformer, while the addition of the SPF-5043 LNA provided a big boost in SNR. Using the single-diode-pair (SDP) configuration along with the WBC4-1 transformer and the LNA improved the SNR to about 60.4 dBFS, which was a 2.6-dB improvement! Using a purely passive solution, the WBC8-1 transformer with an SDP and no LNA, yielded an SNR of about 59.5 dBFS, very close to the 60-dBFS target.

Figure 30 shows a comparison of the clock-input waveforms that occurred with different configurations. The low-jitter clock-source generator combined with the WBC4-1 step-up transformer provided a very large slew rate. Figure 30 shows that the filtered output of the CDCE72010 had

Figure 30. Input waveforms with different clock-source and clipping-diode configurations



a smaller peak-to-peak amplitude and thus a slower slew rate, which negatively impacted the ADC's aperture jitter. Adding the SDP to that configuration seemed to slightly improve the slew rate around the zero crossing point, which also manifested itself as improved SNR performance. Adding the high-gain LNA to the CDCE72010 output sent a much larger signal with a much larger slew rate to the clipping diodes. This resulted in an even faster transition through the zero crossing point, which in turn further improved the aperture jitter of the ADC. The dual-diode-pair (DDP) configuration seemed to improve the slew rate immediately before the zero crossing point a little bit. However, Figure 30 also shows that if the CDCE72010 with the WBC4-1 transformer were used without the LNA, the output voltage might be too low to fully trigger the clipping event. The measurement results in Figure 29 show better SNR performance with the WBC8-1 step-up transformer and DDPs.

Measurements for ADS5483

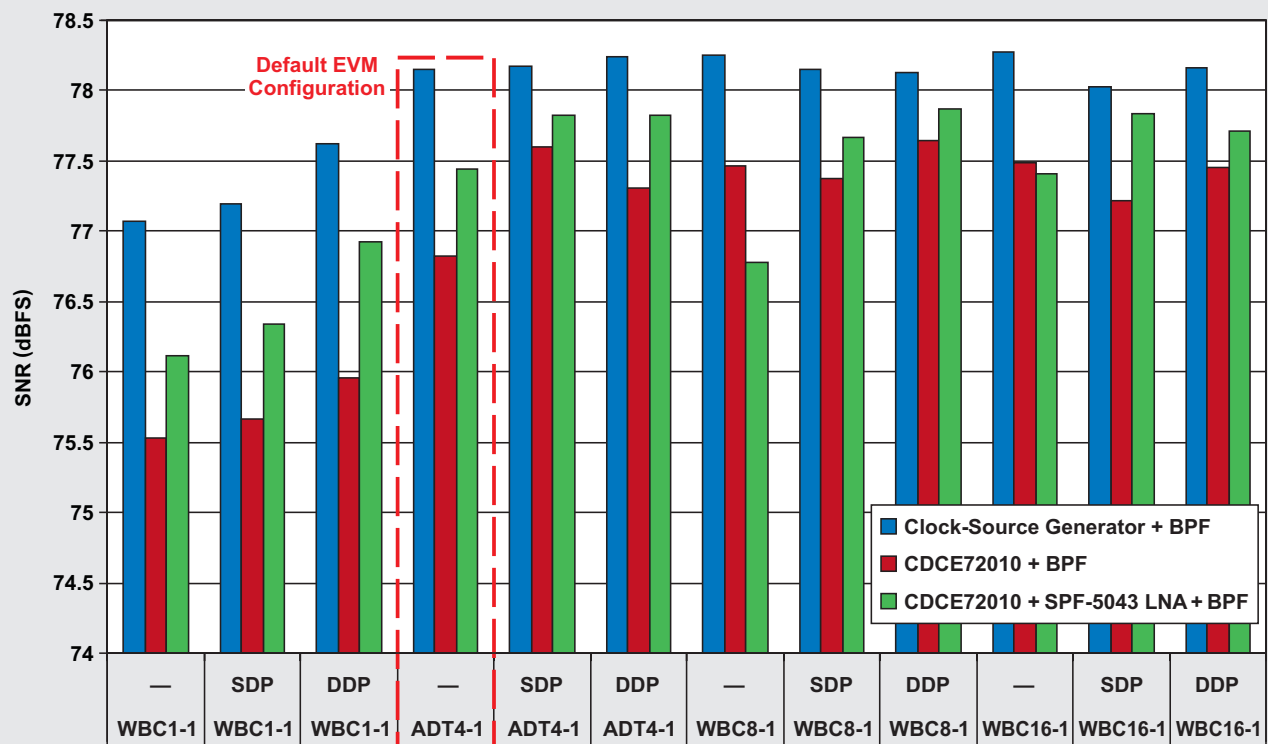
The ADS5483EVM employed a Mini-Circuits ADT4-1WT step-up transformer on the clock input. The baseline SNR with a low-jitter clock source was measured at 78.2 dBFS, while the CDCE72010 output yielded an SNR of about 76.8 dBFS. The CDCE72010 with a clock jitter of about 90 fs should provide an SNR of about 77.6 dBFS, which would be an improvement of almost 1 dB.

The measured SNR values of the ADS5483 with the various EVM clock-input configurations are illustrated in Figure 31. Adding the SDP to the ADT4-1WT transformer provided enough boost to the slew rate for the SNR with the CDCE72010 to improve by almost 1 dB to the 77.6-dBFS target. A larger step-up ratio didn't seem to add any further benefit. Adding the LNA in addition to the ADT4-1WT boosted the SNR to about 77.8 dBFS. It should be noted as well that a lower clock amplitude (WBC1-1) significantly degraded the SNR, as expected.

Conclusion

As explained in Parts 1 and 2 of this article series, the ADC's aperture jitter is not fixed but dependent on the clock-input slew rate. While the bandpass filter is necessary to minimize the clock jitter as much as possible, it also reduces the clock's slew rate by filtering out the higher-order harmonics. This article has shown practical ways (using either active or passive gain) to improve the slew rate of an existing clocking solution with a bandpass filter, thus improving the ADC's SNR by several decibels. The SNR measurements have shown that improving the slew rate of the clock signal makes the ADC's SNR match the predicted SNR for a given amount of clock jitter.

Figure 31. Measured SNR of different clock-input configurations using ADS5483 with $f_S = 122.88$ MSPS and $f_{IN} = 100$ MHz



References

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Document Title	TI Lit. #
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2. Thomas Neu, “Clock jitter analyzed in the time domain, Part 2,” <i>Analog Applications Journal</i> (4Q 2010)	slyt389
3. “12-bit, 500-/550-MSPS analog-to-digital converters,” ADS5463/54RF63 Data Sheet	slas515

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