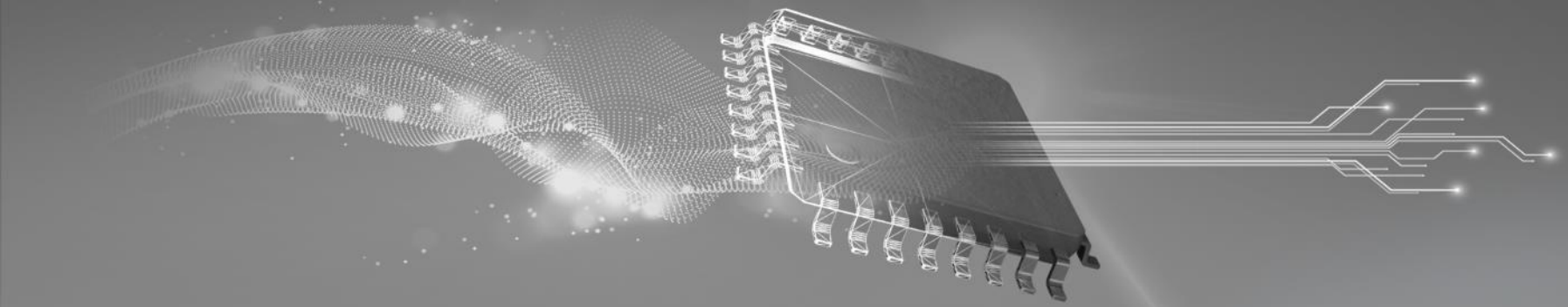
TI TECH DAYS



From start to finish: A product development roadmap for Sitara™ processors

Schuyler Patton

Sitara Processors

Texas Instruments

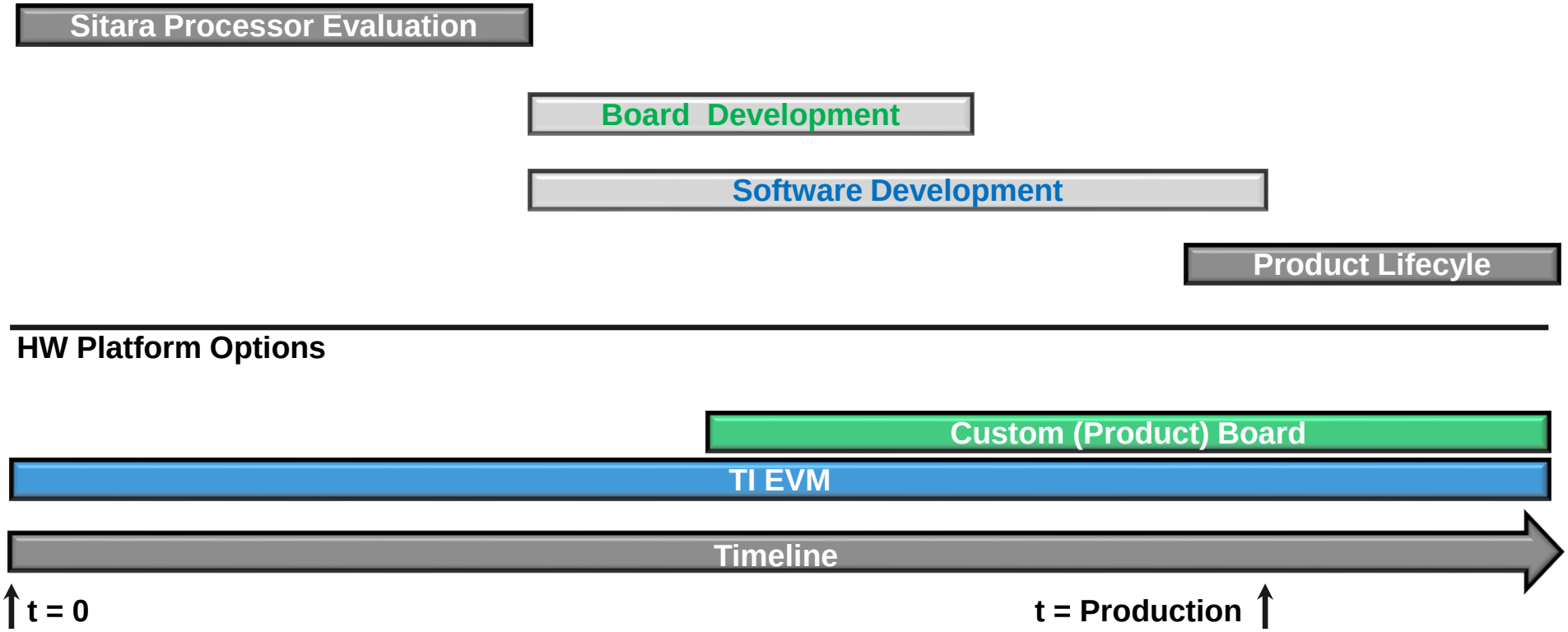
Overview

- Example Phases for a Product Development
- Evaluation Phase
- Board Development Phase
- Software Development Phase
- Production Phase / SW Lifecycle

Phases of Product Development

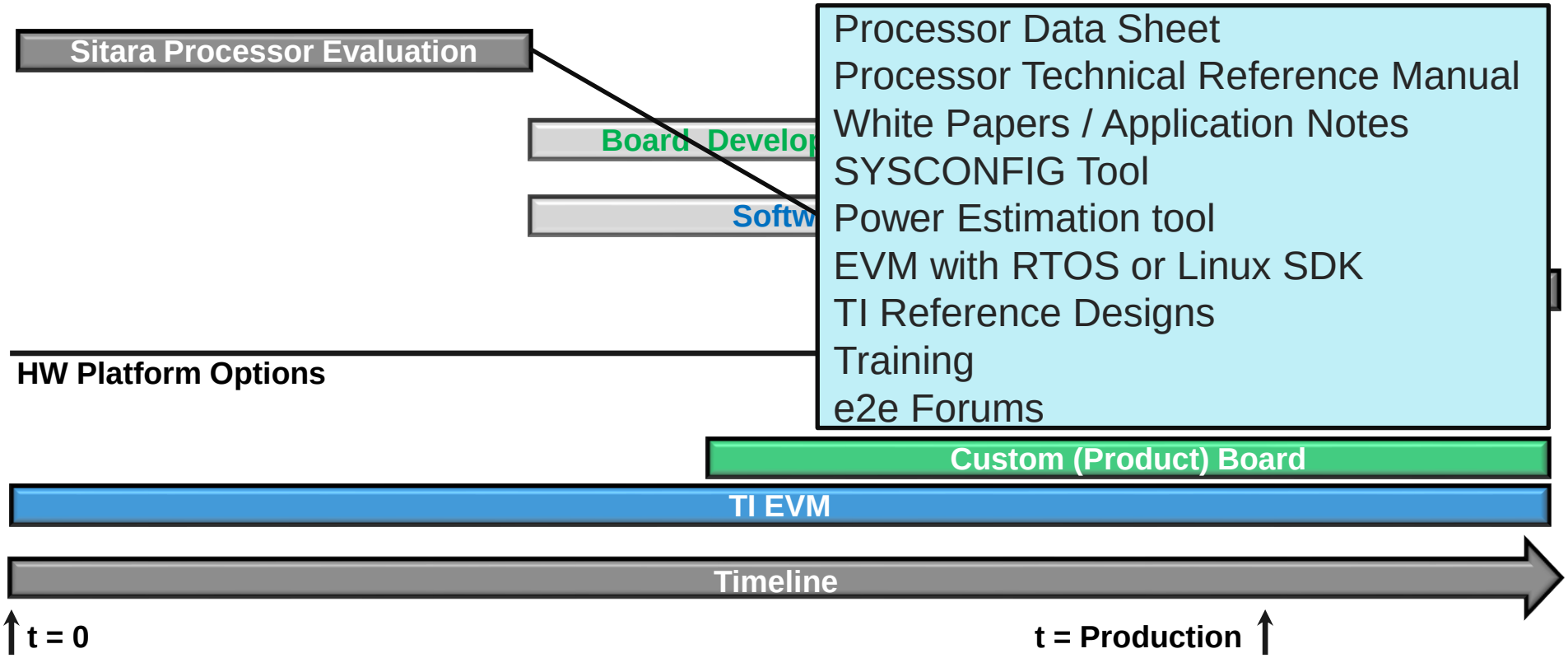
One Example of a Product Development Timeline

One Example of a Product Development Timeline

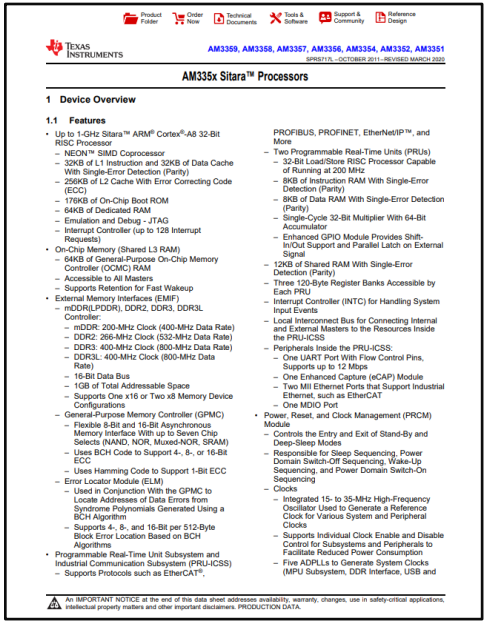


Processor Evaluation

Product Development Timeline - Evaluation



Processor Evaluation – Datasheet & TRM



Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community | Reference Design

TEXAS INSTRUMENTS

AM3359, AM3358, AM3357, AM3356, AM3354, AM3352, AM3351

SPRS717L – OCTOBER 2011 – REVISED MARCH 2020

AM335x Sitara™ Processors

1 Device Overview

1.1 Features

- Up to 1-GHz Sitara™ ARM® Cortex®-A8 32-Bit RISC Processor
  - NEON™ SIMD Coprocessor
  - 32KB of L1 Instruction and 32KB of Data Cache With Single-Error Detection (Parity)
  - 256KB of L2 Cache With Error Correcting Code (ECC)
  - 176KB of On-Chip Boot ROM
  - 64KB of Dedicated RAM
  - Emulation and Debug - JTAG
  - Interrupt Controller (up to 128 Interrupt Requests)
- On-Chip Memory (Shared L3 RAM)
  - 64KB of General-Purpose On-Chip Memory Controller (OCMC) RAM
  - Accessible to All Masters
  - Supports Retention for Fast Wakeup
- External Memory Interfaces (EMIF)
  - mDDR(LPDDR), DDR2, DDR3, DDR3L Controller:
    - mDDR: 200-MHz Clock (400-MHz Data Rate)
    - DDR2: 266-MHz Clock (532-MHz Data Rate)
    - DDR3: 400-MHz Clock (800-MHz Data Rate)
    - DDR3L: 400-MHz Clock (800-MHz Data Rate)
    - 16-Bit Data Bus
    - 1GB of Total Addressable Space
    - Supports One x16 or Two x8 Memory Device Configurations
  - General-Purpose Memory Controller (GPMC)
    - Flexible 8-Bit and 16-Bit Asynchronous Memory Interface With up to Seven Chip Selects (NAND, NOR, Muxed-NOR, SRAM)
    - Uses BCH Code to Support 4-, 8-, or 16-Bit ECC
    - Uses Hamming Code to Support 1-Bit ECC
  - Error Locator Module (ELM)
    - Used in Conjunction With the GPMC to Locate Addresses of Data Errors from Syndrome Polynomials Generated Using a BCH Algorithm
    - Supports 4-, 8-, and 16-Bit per 512-Byte Block Error Location Based on BCH Algorithms
- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
  - Supports Protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, and More
  - Two Programmable Real-Time Units (PRUs)
    - 32-Bit Load/Store RISC Processor Capable of Running at 200 MHz
    - 8KB of Instruction RAM With Single-Error Detection (Parity)
    - 8KB of Data RAM With Single-Error Detection (Parity)
    - Single-Cycle 32-Bit Multiplier With 64-Bit Accumulator
    - Enhanced GPIO Module Provides Shift-In/Out Support and Parallel Latch on External Signal
    - 12KB of Shared RAM With Single-Error Detection (Parity)
    - Three 120-Byte Register Banks Accessible by Each PRU
    - Interrupt Controller (INTC) for Handling System Input Events
    - Local Interconnect Bus for Connecting Internal and External Masters to the Resources Inside the PRU-ICSS
    - Peripherals Inside the PRU-ICSS:
      - One UART Port With Flow Control Pins, Supports up to 12 Mbps
      - One Enhanced Capture (eCAP) Module
      - Two MII Ethernet Ports that Support Industrial Ethernet, such as EtherCAT
      - One MDIO Port
- Power, Reset, and Clock Management (PRCM) Module
  - Controls the Entry and Exit of Stand-By and Deep-Sleep Modes
  - Responsible for Sleep Sequencing, Power Domain Switch-Off Sequencing, Wake-Up Sequencing, and Power Domain Switch-On Sequencing
  - Clocks
    - Integrated 15- to 35-MHz High-Frequency Oscillator Used to Generate a Reference Clock for Various System and Peripheral Clocks
    - Supports Individual Clock Enable and Disable Control for Subsystems and Peripherals to Facilitate Reduced Power Consumption
    - Five ADPLLs to Generate System Clocks (MPU Subsystem, DDR Interface, USB and

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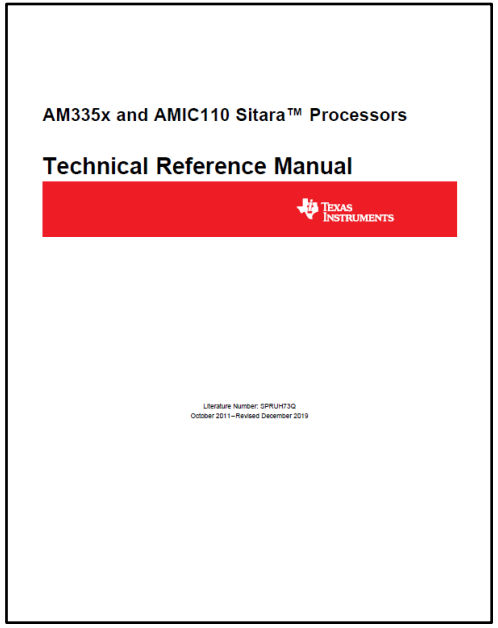


AM335x and AMIC110 Sitara™ Processors

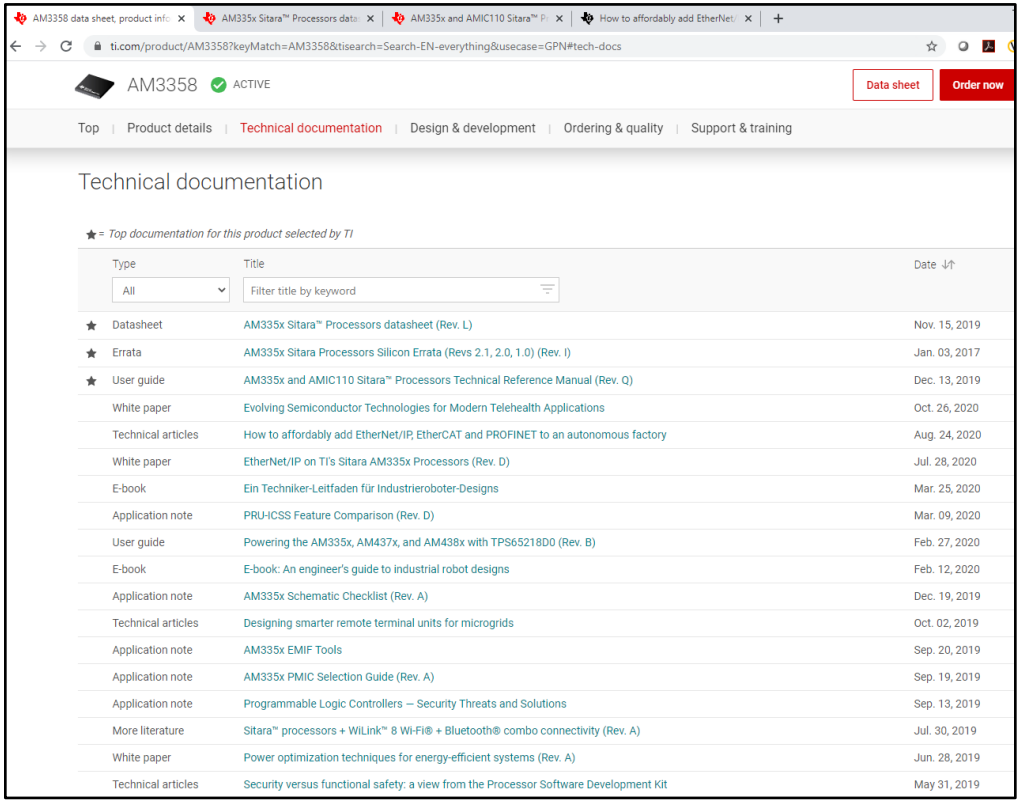
Technical Reference Manual

TEXAS INSTRUMENTS

Literature Number: SPRUH73Q
October 2011–Revised December 2019

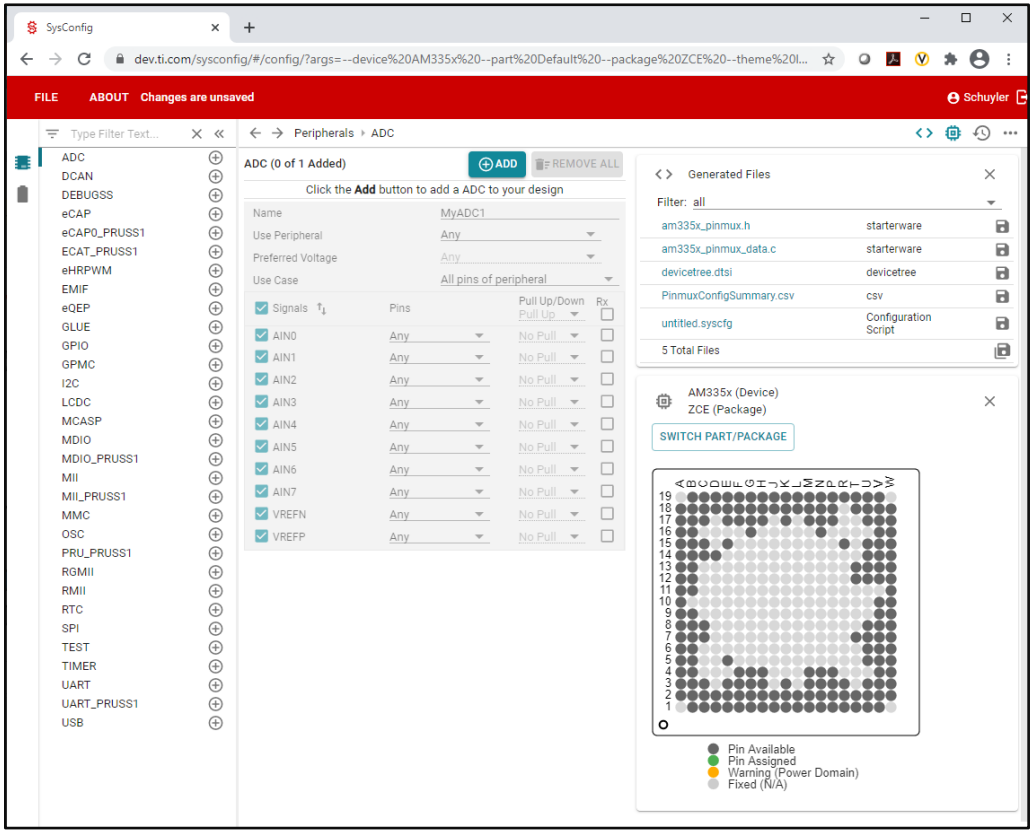
- Datasheet
  - ARM processor frequencies supported
  - Available Peripherals
  - DDR Memory types supported
  - Power, Clocking Capabilities
- Technical Reference Manual (TRM)
  - Companion guide to Datasheet
  - details the integration, environment, functional description, programming models for each peripheral and subsystem in the device

Processor Evaluation – Technical Documentation



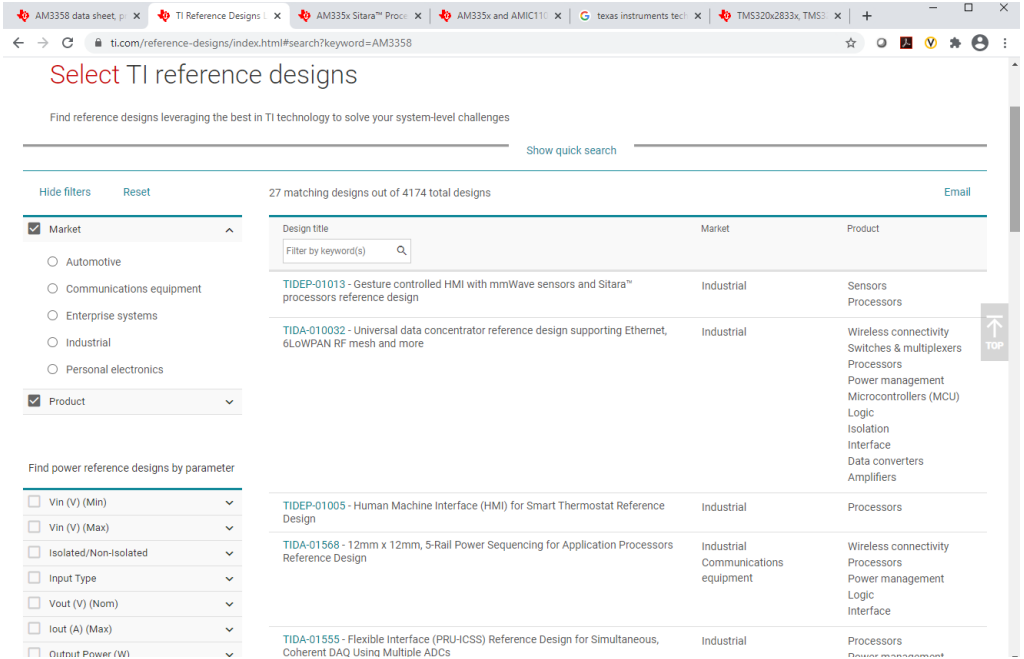
- White papers
  - Power Optimization Techniques
  - Sitara Processor Security
- Application Notes
  - Hardware Design Guide
  - Schematic Checklist
  - EMIF Tool
- E-Books
- Technical Articles

Processor Evaluation - SYSCONFIG Tool



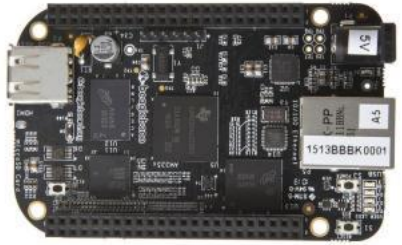
- Software tool that provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts
- Perform “what-if” on possible pin mux configurations for a particular application

Processor Evaluation - TI Reference Designs

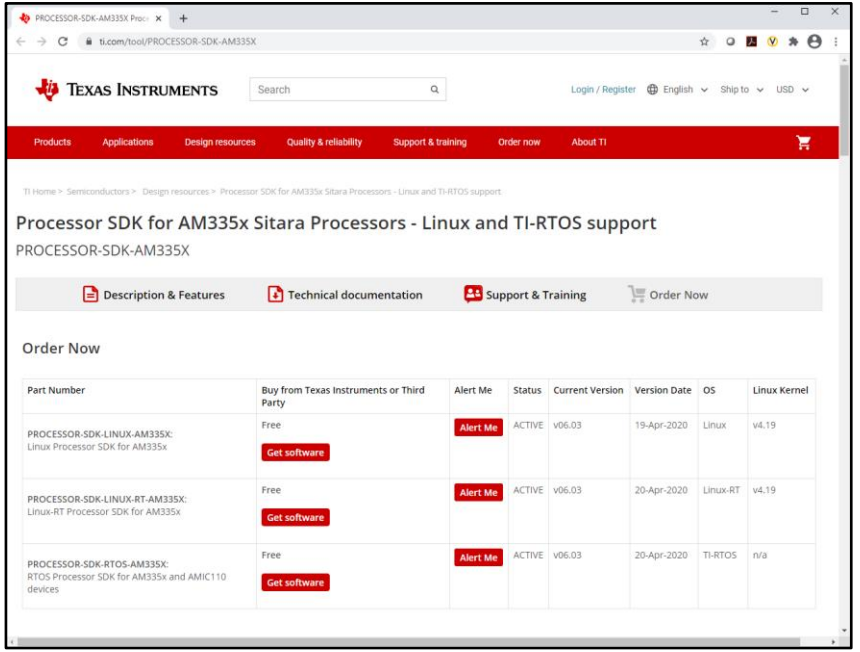


- Leverage TI technology to solve your system-level challenges
- Some designs use TI Evaluation Modules
- Schematics and other documentation provided such as PCB layouts, Bill of Materials (BOM) and User Guide

Product Timeline - Evaluation



Use TI Processor SDKs to run demos as well as build experimental applications on TI Evaluation Modules

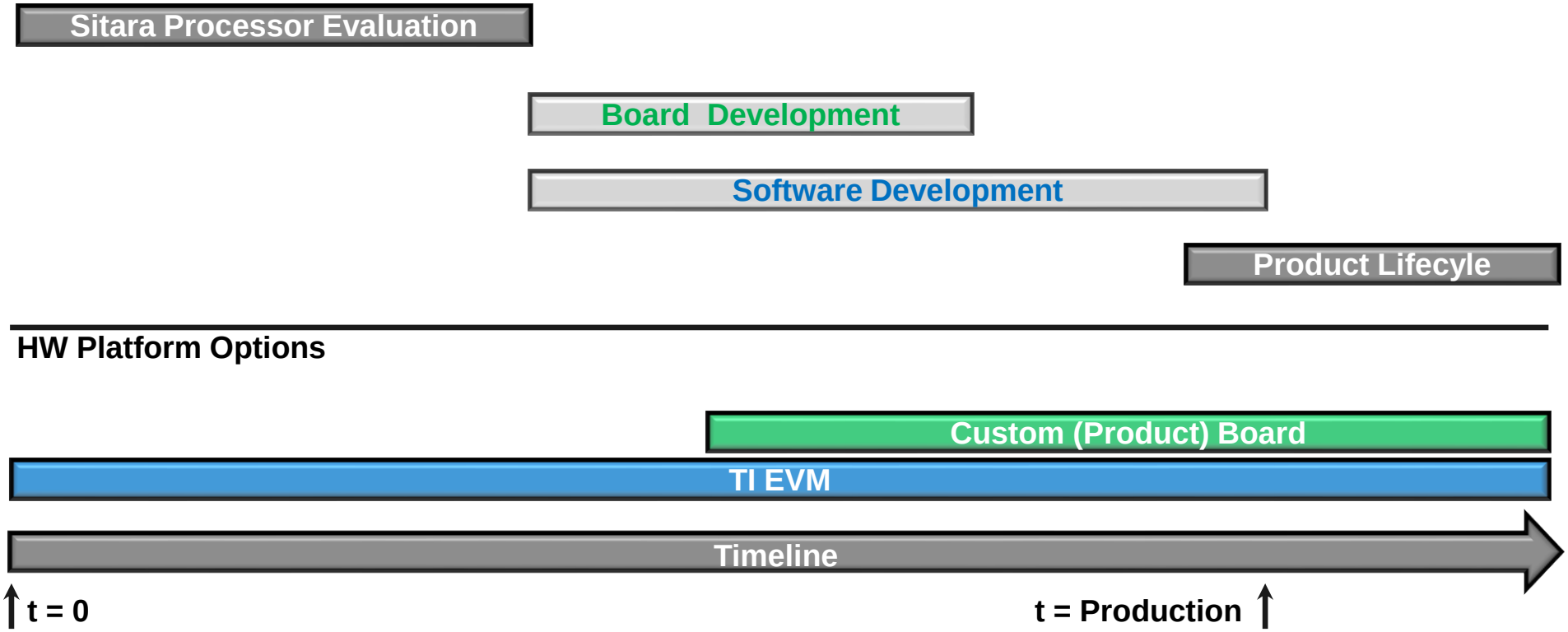


Product Evaluation Summary

- Use the Datasheet and The Technical Reference Manual to determine processor compatibility
- Review the available Application Notes, Whitepapers and other technical documentation available on ti.com
- Use the SYSCONFIG tool to evaluate possible pin mux outputs to determine “what if” processor configurations
- Review TI Reference Designs for design elements to be used in a new product
- Experiment with TI Evaluation Modules and the RTOS and Linux Software Development Kits to evaluate processor capabilities

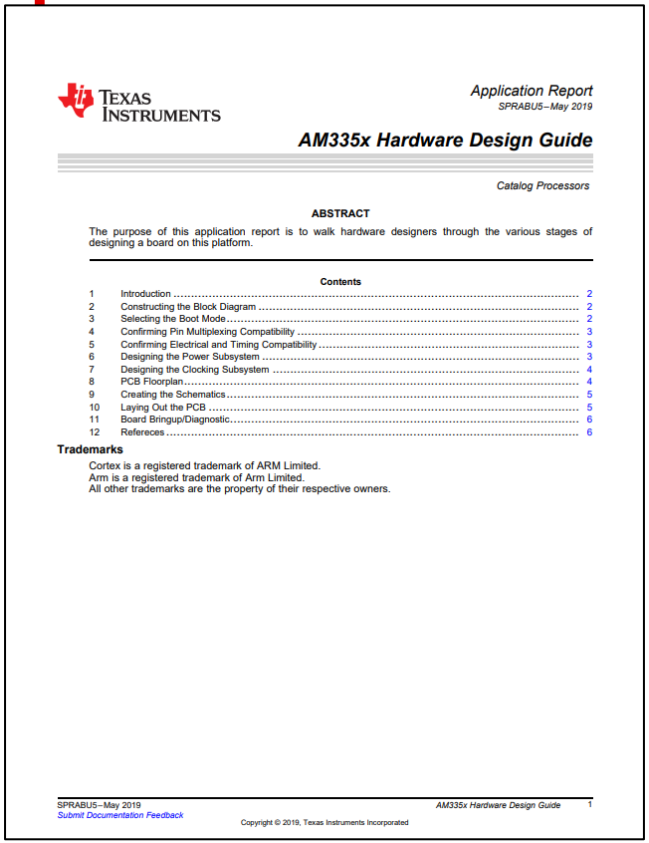
Board Development

Product Timeline – Board Development



Product Timeline – Board Development

- The purpose of this application report is to walk hardware designers through the various stages of designing a board on this platform.
- Block diagram of suggested of hardware design flow for a board design
- Use Reference material provided by TI in the Technical Documentation tab of the Processor Product folder



Texas Instruments

Application Report
SPRABU5–May 2019

AM335x Hardware Design Guide

Catalog Processors

ABSTRACT

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Contents

Trademarks

SPRABU5

Product Timeline – Board Development

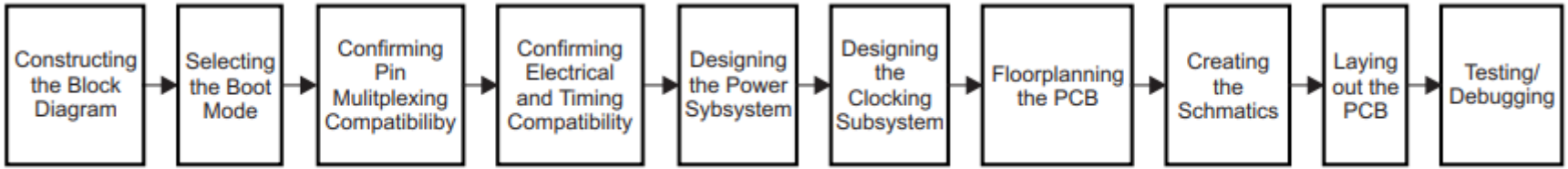
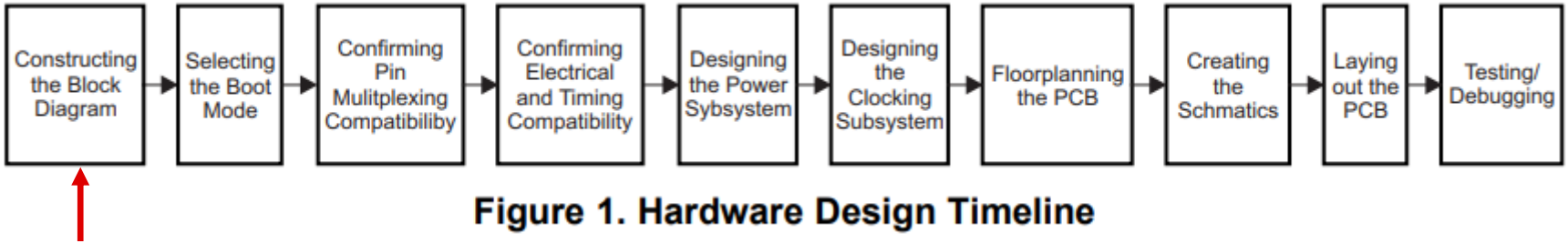


Figure 1. Hardware Design Timeline

Product Timeline – Board Development



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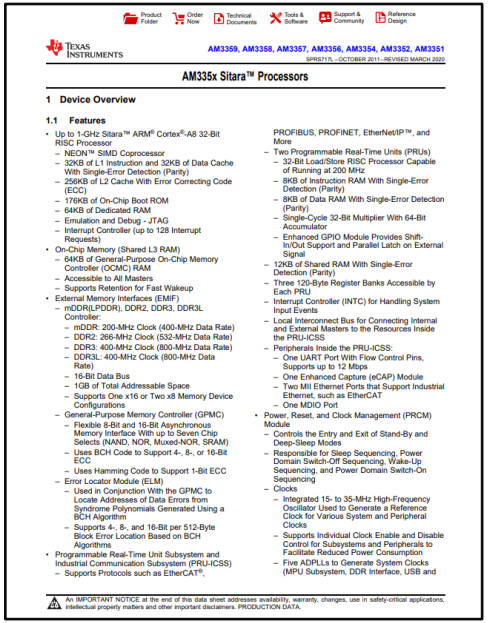
Processor Datasheet
Technical Reference manual

Board Development – Datasheet & TRM



Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community | Reference Design

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SPRS717L – OCTOBER 2011 – REVISED MARCH 2020

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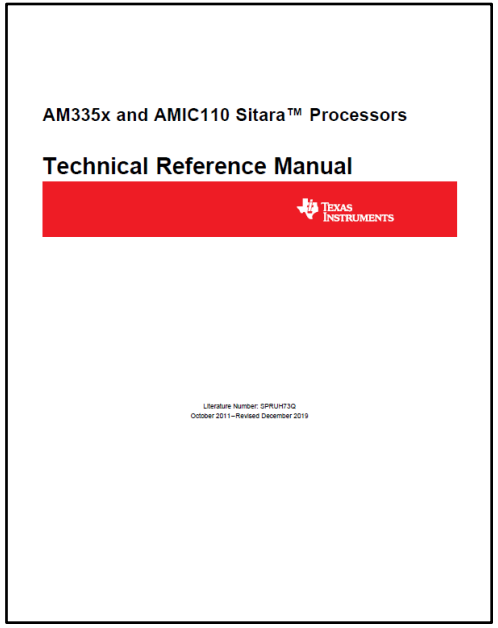


AM335x and AMIC110 Sitara™ Processors

Technical Reference Manual

TEXAS INSTRUMENTS

Literature Number: SPRUH73Q
October 2011–Revised December 2019

- Datasheet
  - Designing
    - Device interconnections
    - Electrical & Timing requirements
    - Pin Muxing
    - Power
    - DDR Memory Interfacing
- Technical Reference Manual (TRM)
  - Boot Modes
  - Peripheral Clocking and operations
  - Control Module, register descriptions

Product Timeline – Board Development

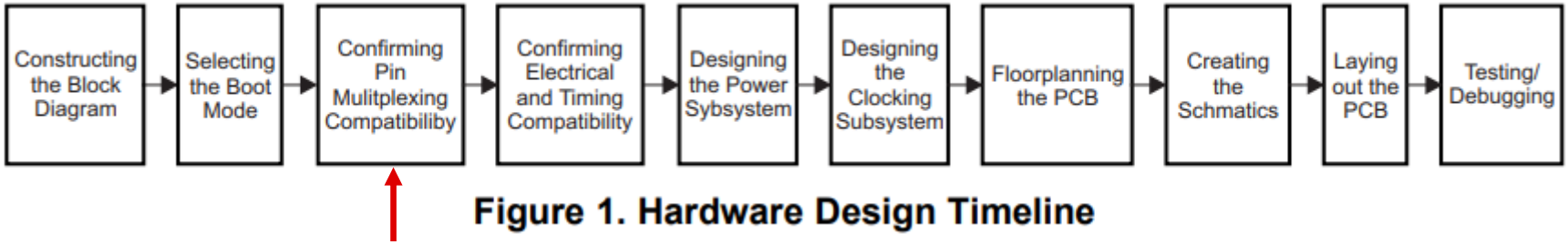
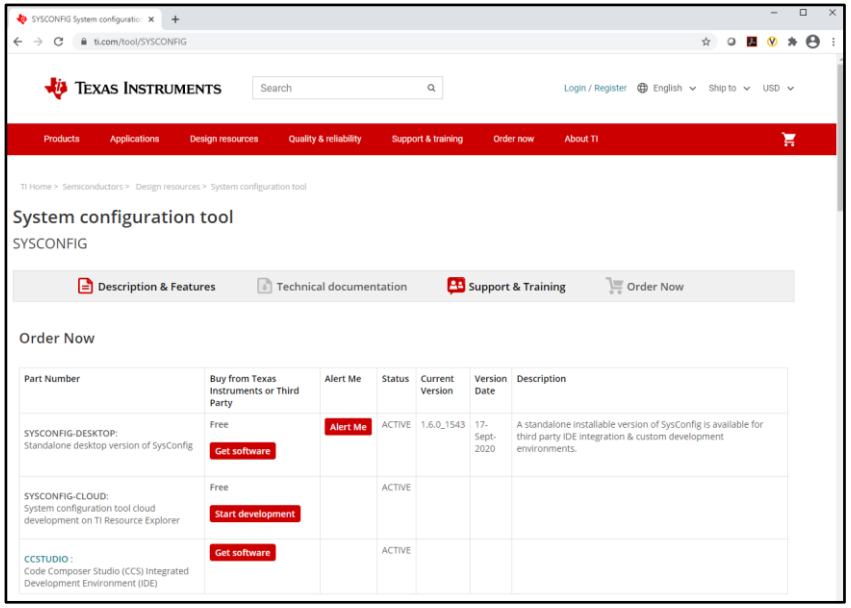
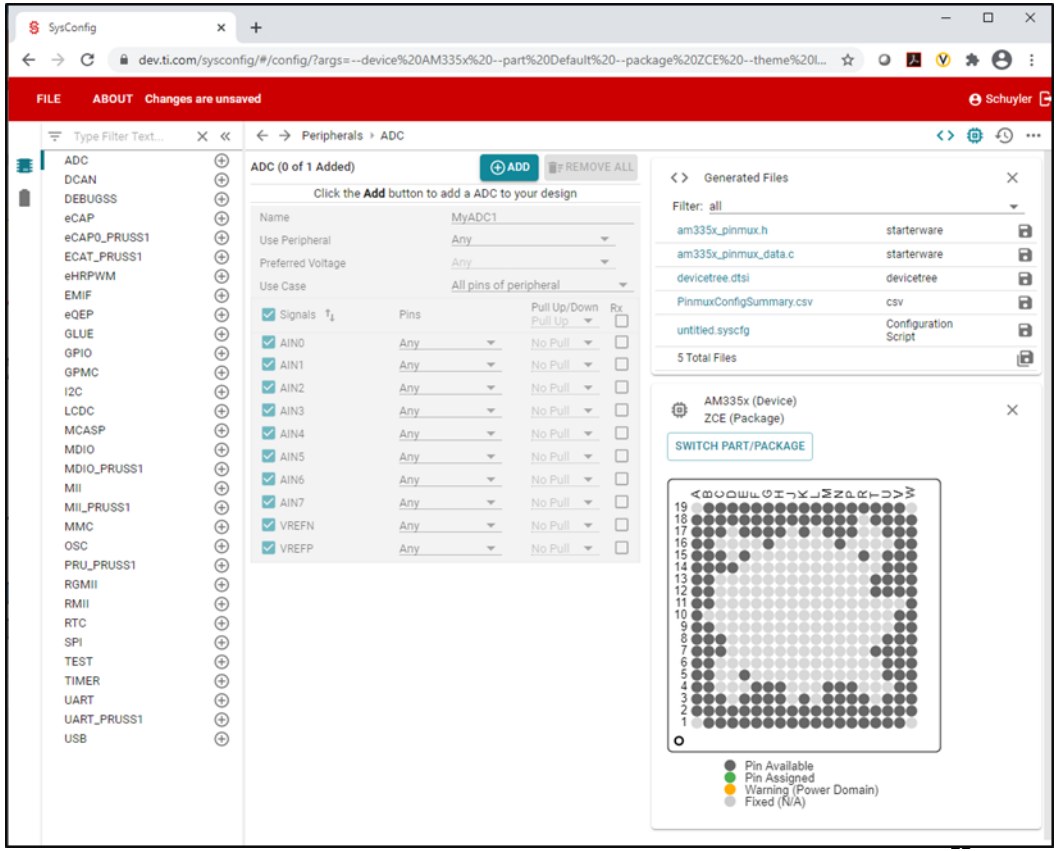


Figure 1. Hardware Design Timeline

Board Development - SYSCONFIG Tool





- SYSCONFIG tool can be downloaded or has cloud access

Product Timeline – Board Development

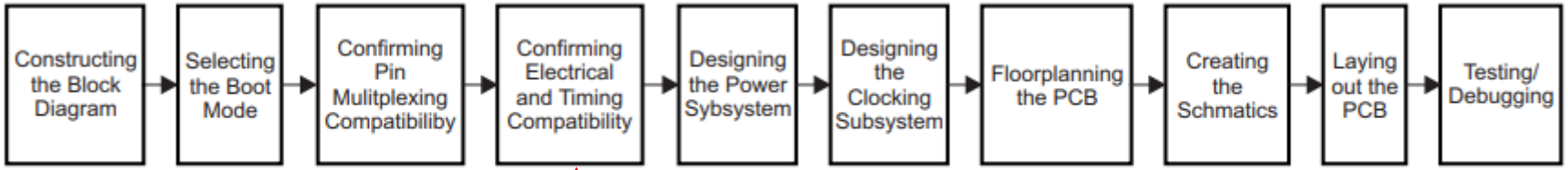
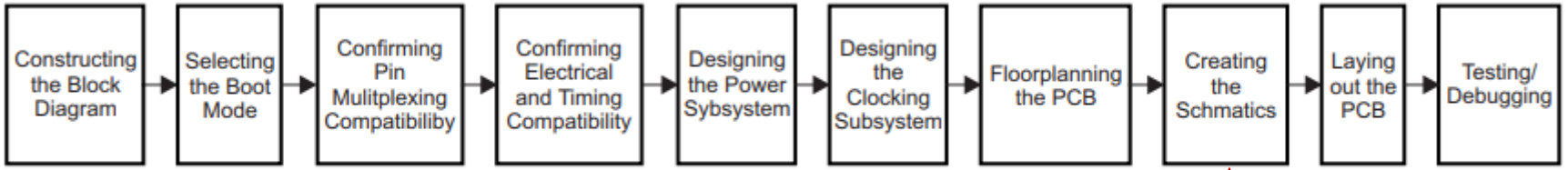


Figure 1. Hardware Design Timeline

IBIS Models for Timing Analysis

Product Timeline – Board Development



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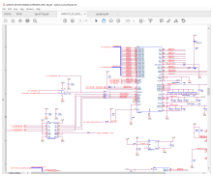
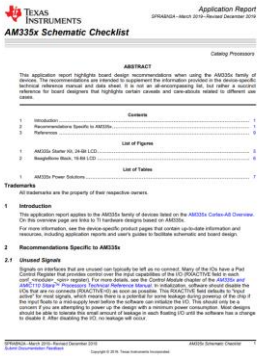
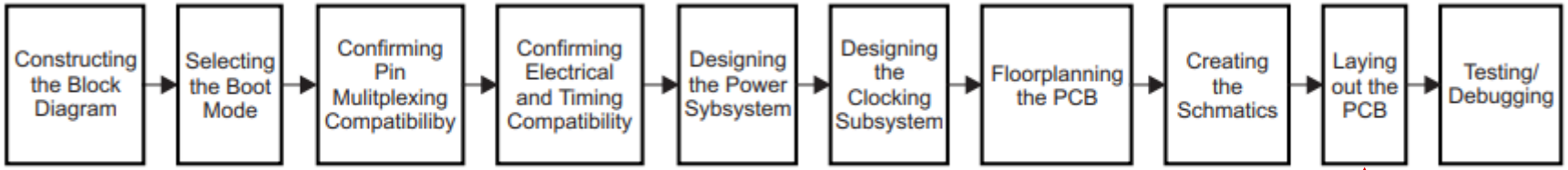


EVM Schematics



AM335x Schematic Checklist
(SPRABN2A**)**

Product Timeline – Board Development



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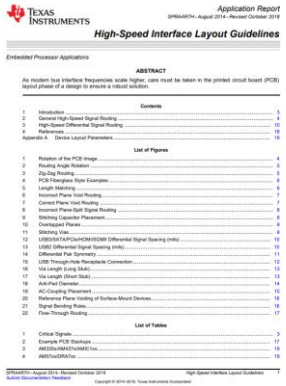


Texas Instruments

Application Report

SPRAAR7H–August 2014–Revised October 2018

High-Speed Interface Layout Guidelines

Embedded Processor Applications

ABSTRACT

As modern bus interface frequencies scale higher, care must be taken in the printed circuit board (PCB) layout phase of a design to ensure a robust solution.

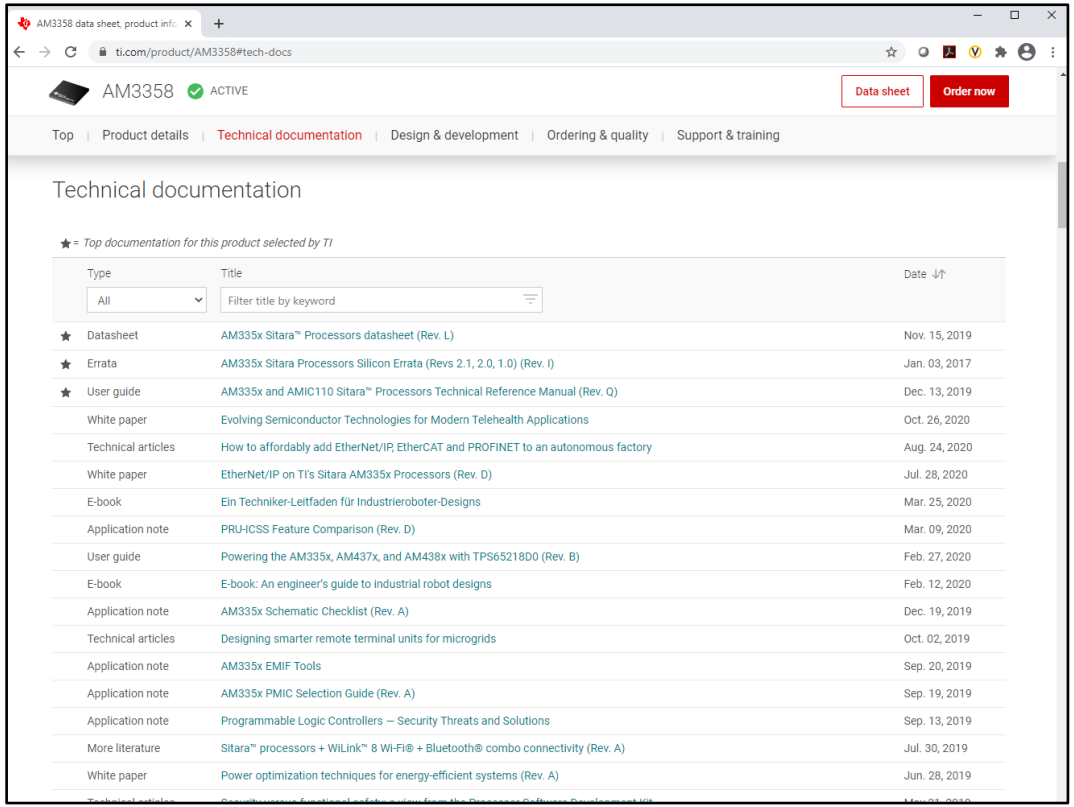
Contents

List of Figures

List of Tables

High Speed Interface Layout Guidelines (SPRAAR7H)

Product Timeline – Board Development



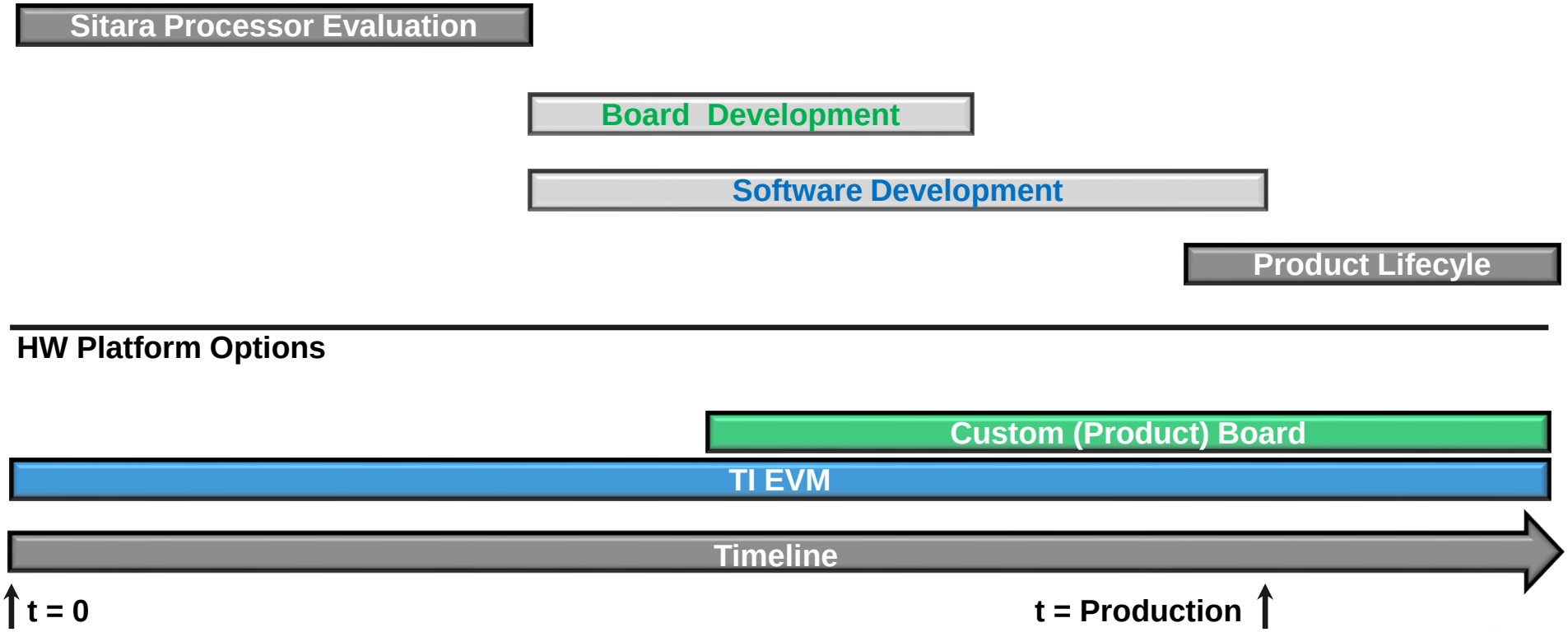
- The Technical documentation Tab of the product folder contains the list of available documentation for a Processor.

Board Development Summary

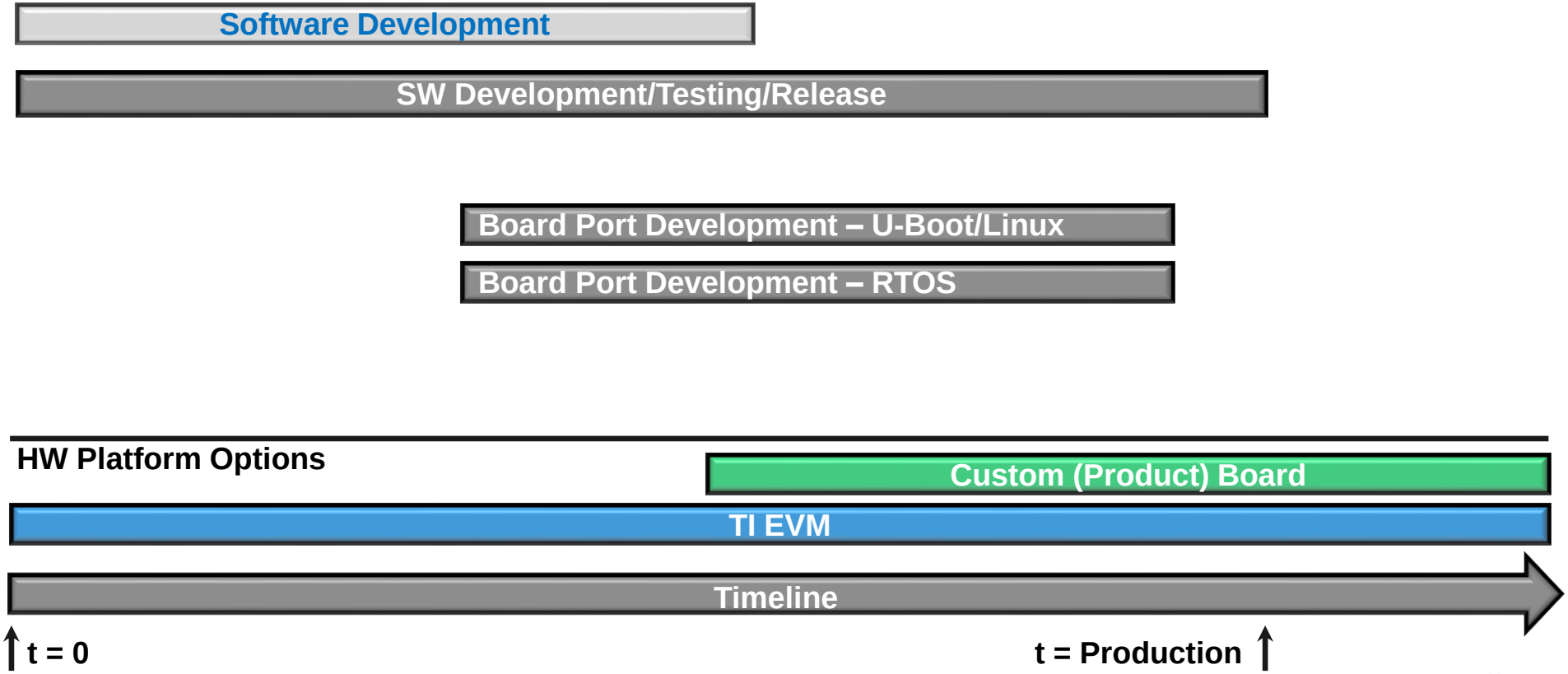
- Follow the steps shown in the Hardware Design guide
- Leverage the documentation provided in the processor product folder
- Use the Datasheet and TRM to create system block diagram
- The tools for SYSCONFIG, EMIF tool assists with determining pin mux configuration

Software Development

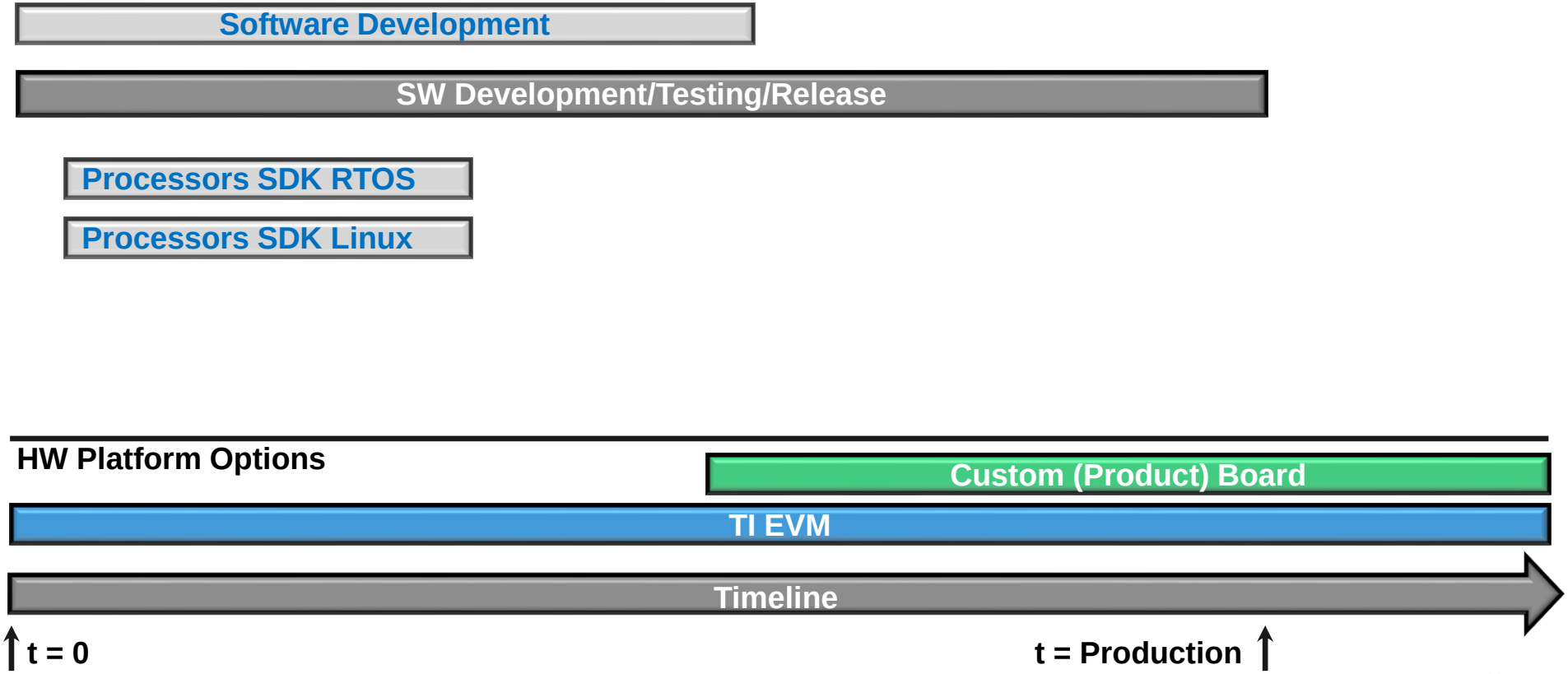
Product Timeline – Software Development



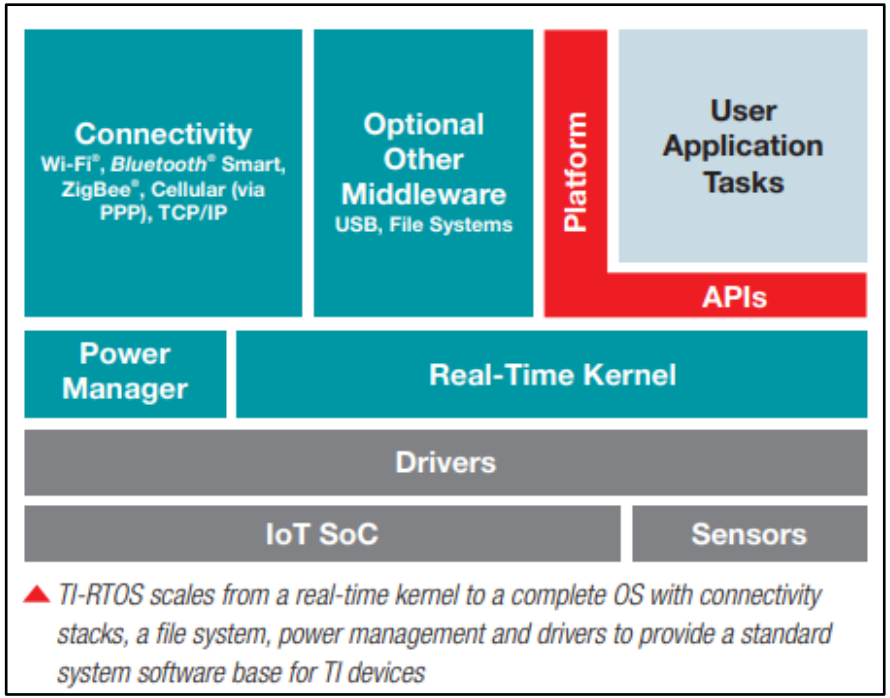
Product Timeline – Software Development



Product Timeline – Software Development



Product Timeline – Software Development RTOS



sprt646a.pdf

- Robust real-time TI-RTOS kernel including TCP/IP networking stack
- Posix thread-compatible API layer available
- Driver libraries that can be used with TI-RTOS or without a kernel
- Free and available as open source

Product Timeline – Software Development Linux

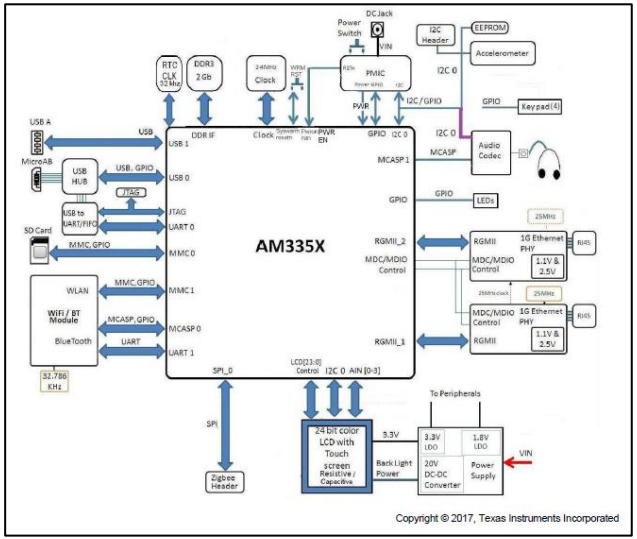
Foundational Components (more information on each piece of the distribution)			
U-Boot	Boot Monitor	Kernel	Filesystem
Tools	OpenCL	OpenCV	Graphics & Display
Multimedia	Examples, Demos	PRU-ICSS / PRU_ICSSG	Virtualization
IPC	OpenVX	CMEM	Machine Learning
ATF	OPTEE		

- **Updated to the latest Long Term support (LTS) Linux kernel, boot loader and Yocto file system on an annual basis**
- **U-Boot community boot loader**
- **Robust, commercial-grade Linaro® GNU compiler collection (GCC) toolchain**
- **Yocto Project™ OE Core compatible file systems support enables tailored Linux application support**
- **RT-Linux releases include a fully pre-emptible kernel for real-time applications**

Product Timeline – Software Development

Board Port Development – U-Boot/Linux

- Porting - Bring up U-Boot/Linux on Custom Hardware
  - Processor SDK Linux has the processor initialization, driver support for Linux and U-Boot
  - Leveraging TI EVM code makes porting strait forward
  - Use the EMIF and SYSCONFIG tools to assist with the port effort



HW Platform Options

Custom (Product) Board

TI EVM

Timeline

t = 0

t = Production

Product Timeline – Software Development

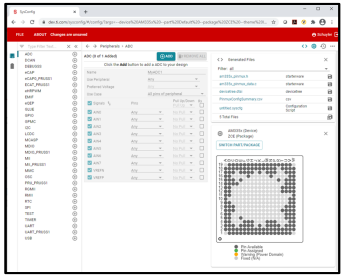
Board Port Development – U-Boot/Linux

Porting U-Boot

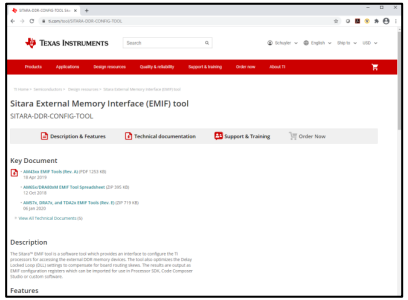
Leverage TI Code — TI U-Boot Code in SDK

DDR Settings — EMIF Tool

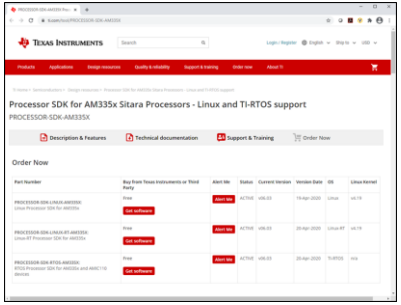
Pin Mux Configuration — SYSCONFIG



SYSCONFIG

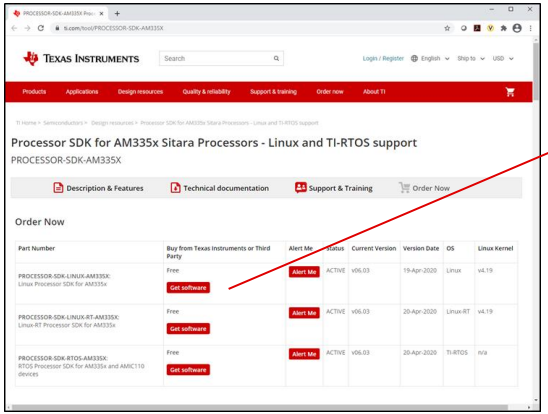


EMIF Tool



TI Processors SDK Linux

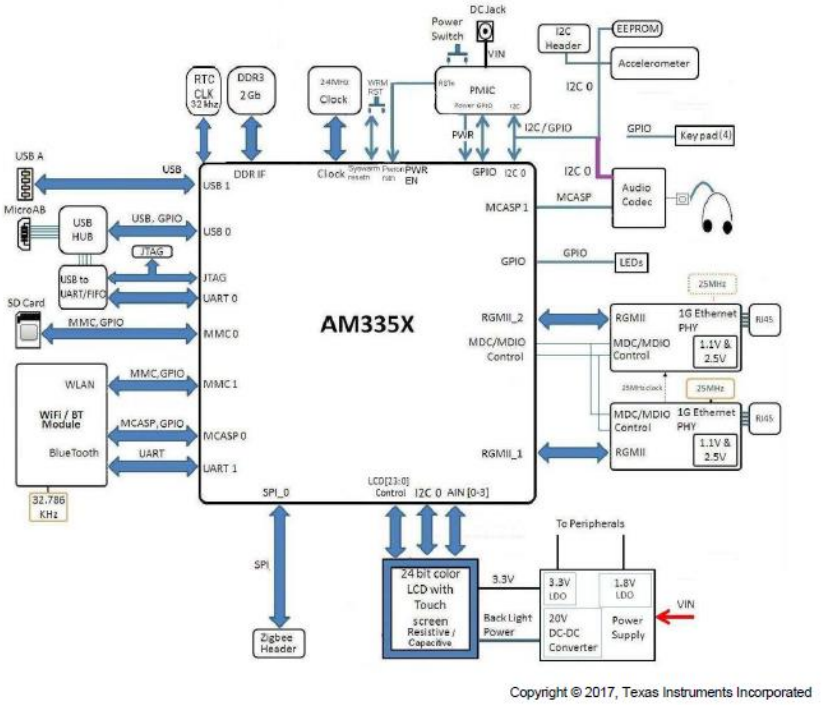
Product Timeline – U-Boot Board Port



TI Processors SDK Linux

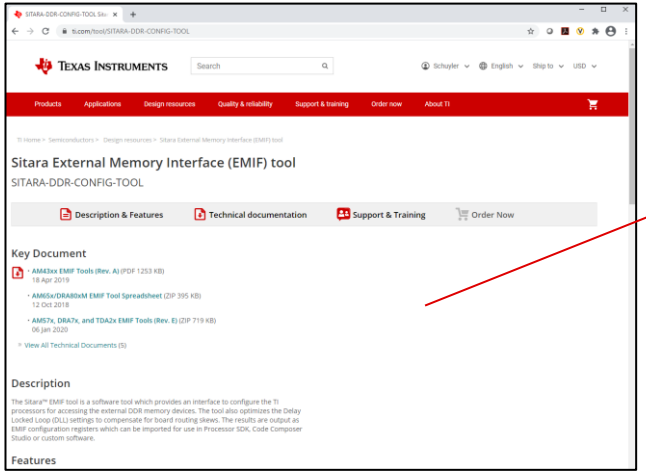
board/ti/am335x/board.c

board.c



The board.c file is a key file for porting U-Boot to a custom board

Product Timeline – U-Boot Board Port

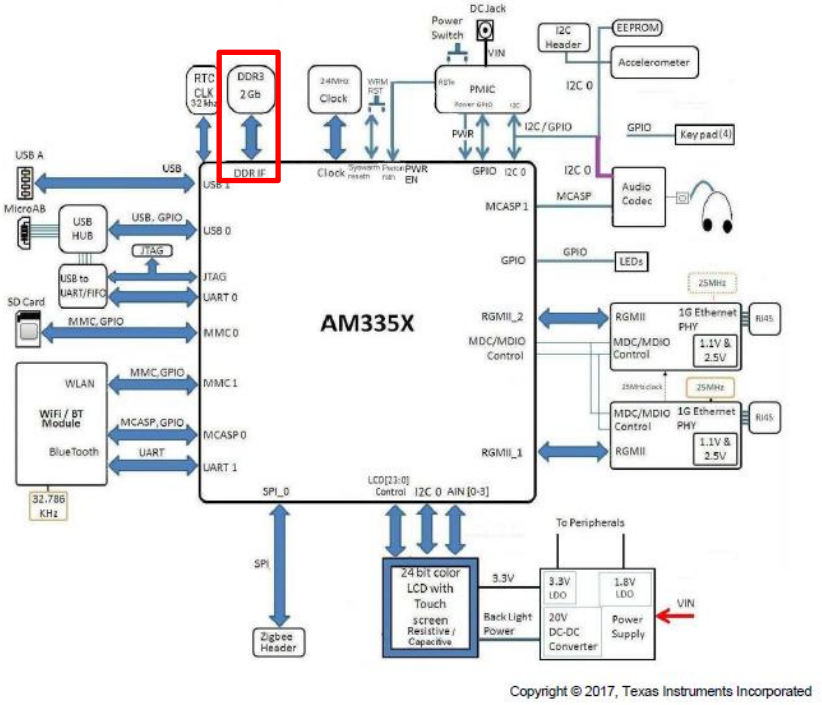


EMIF Tool

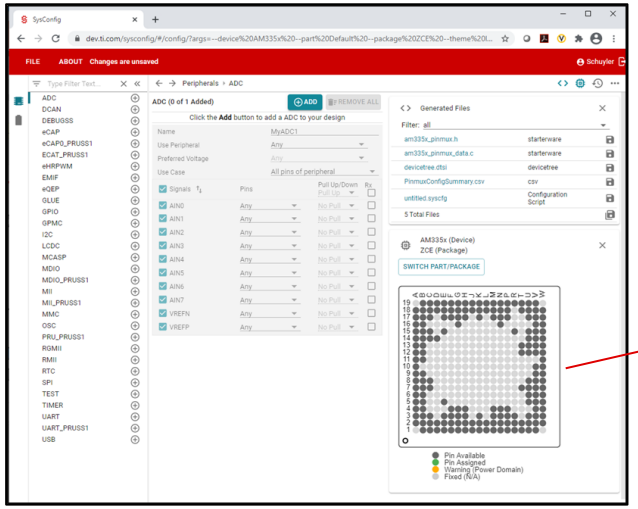
board/ti/am335x/board.c

board.c

EMIF Settings



Product Timeline – U-Boot Board Port



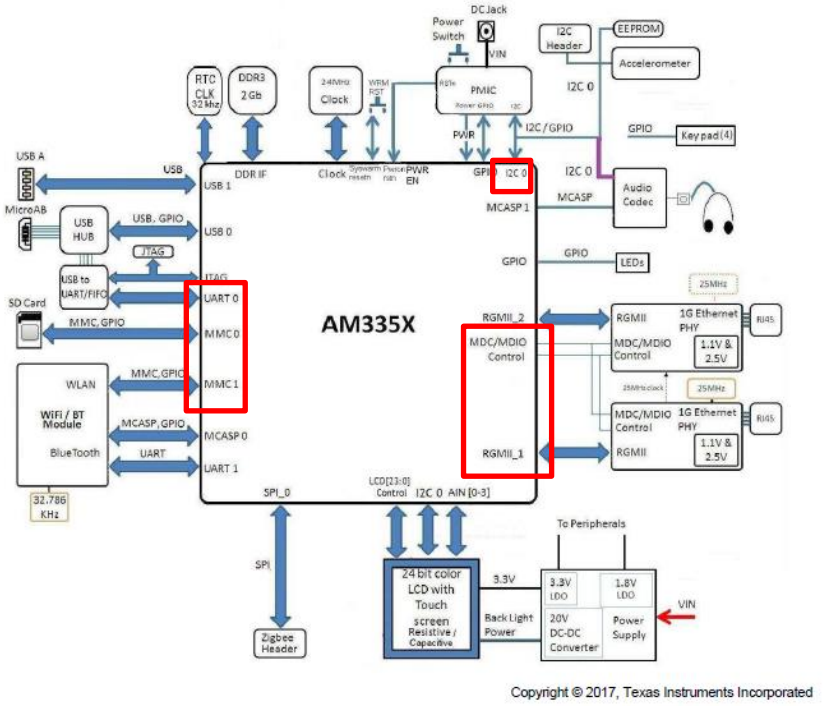
SYSCONFIG

board/ti/am335x/board.c

board.c

EMIF Settings

Pin Mux Settings

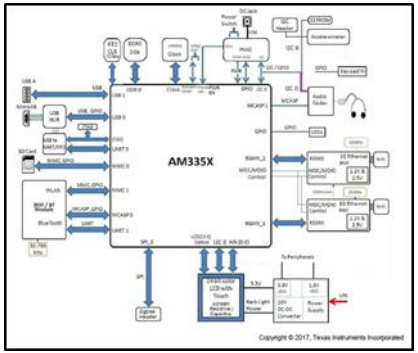


Product Timeline – Software Development

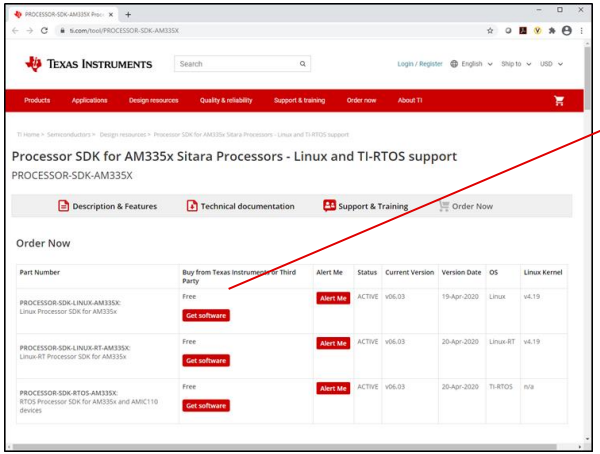
Board Port Development – U-Boot/Linux

Porting Linux

Leverage TI Code	**TI DTS Code**
Pin Mux Configuration	**SYSCONFIG**



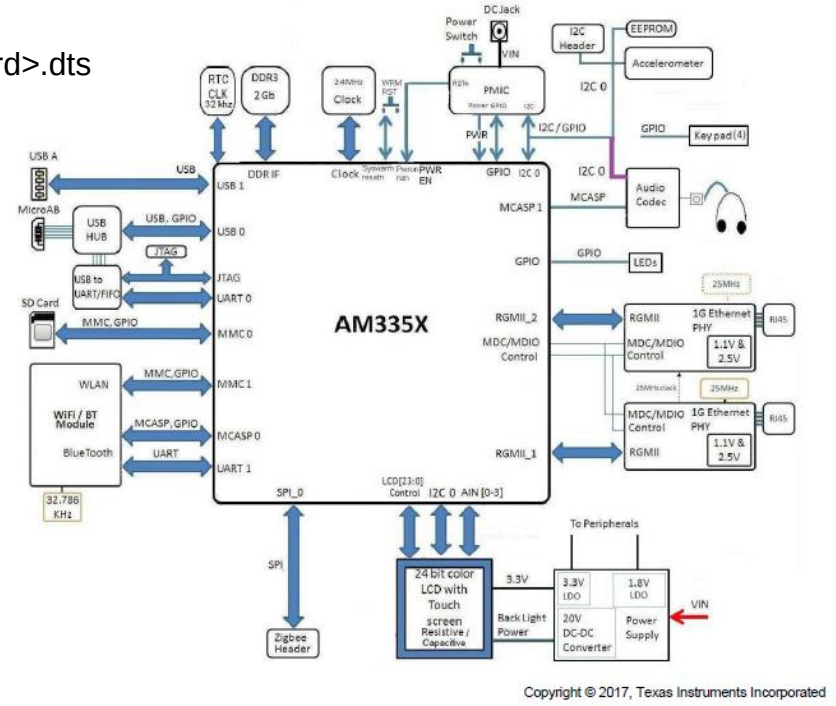
Product Timeline – Linux Board Port



TI Processors SDK Linux

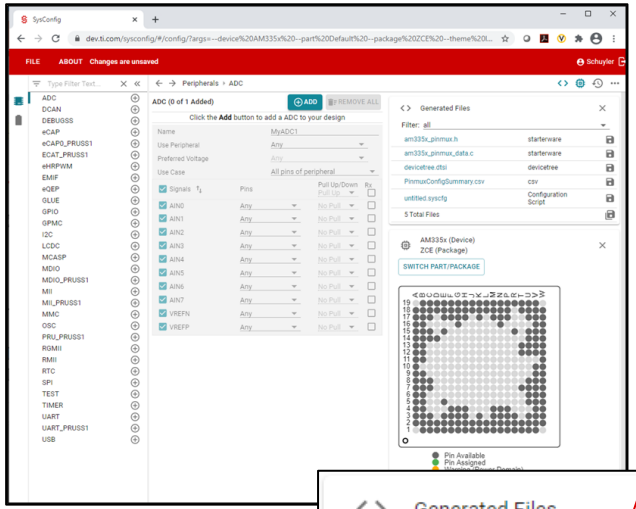
arch/arm/boot/dts/<board>.dts

<board>.dts



The <board>.dts file is the key file for porting Linux to a custom board

Product Timeline – Linux Board Port

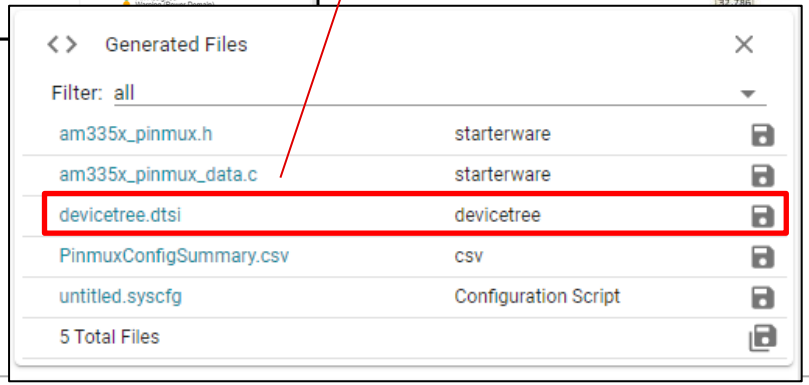


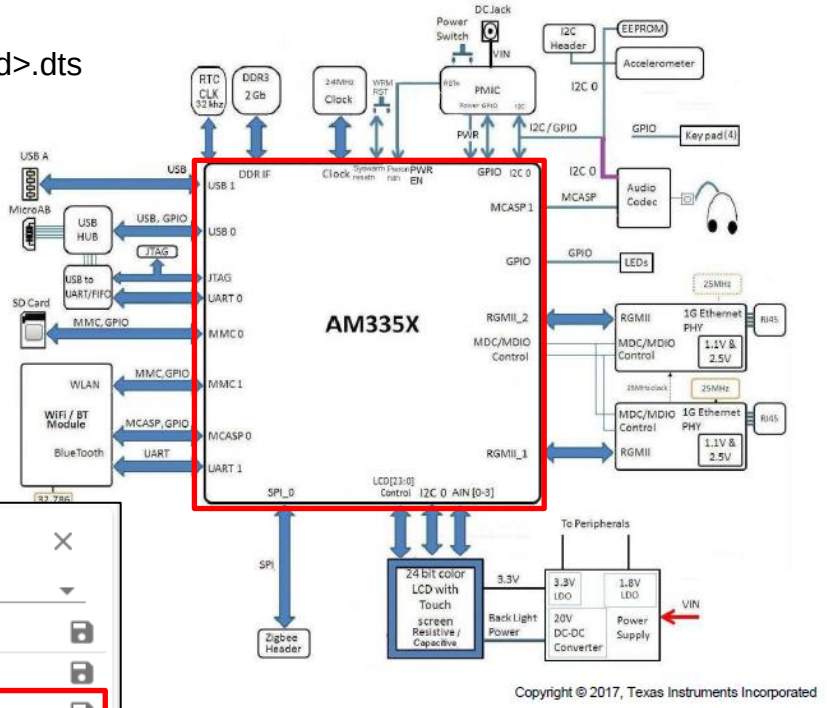
SYSCONFIG

arch/arm/boot/dts/<board>.dts

<board>.dts

devicetree.dtsi



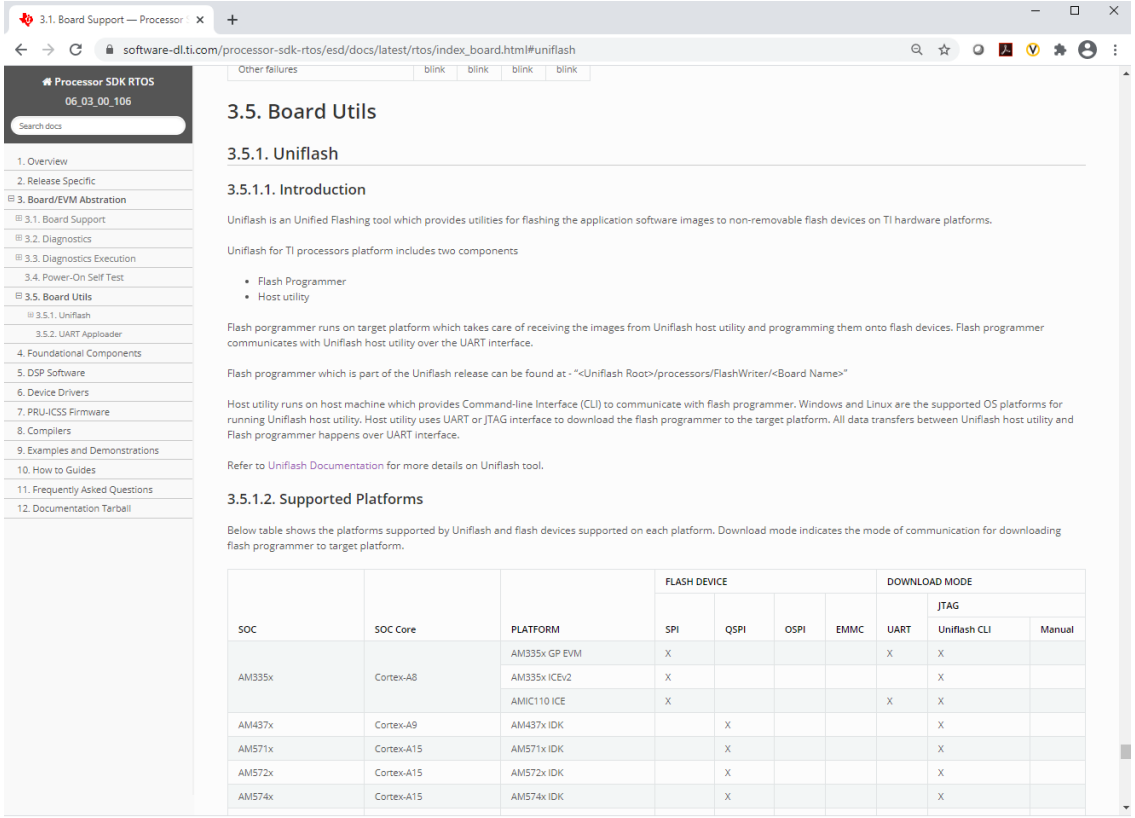


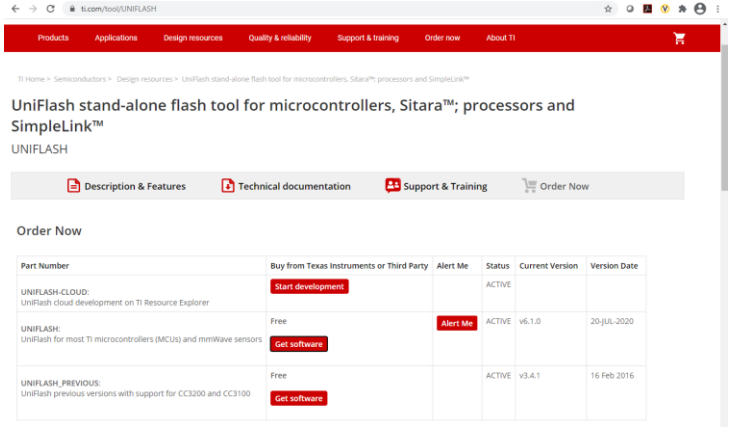
Software Development Summary

- TI Provides an RTOS and Linux SDK operating system for each processor
- The SDKs provide the starting point for application development
- The SYSCONFIG and EMIF Tools should be used to accelerate porting operating systems to a new board

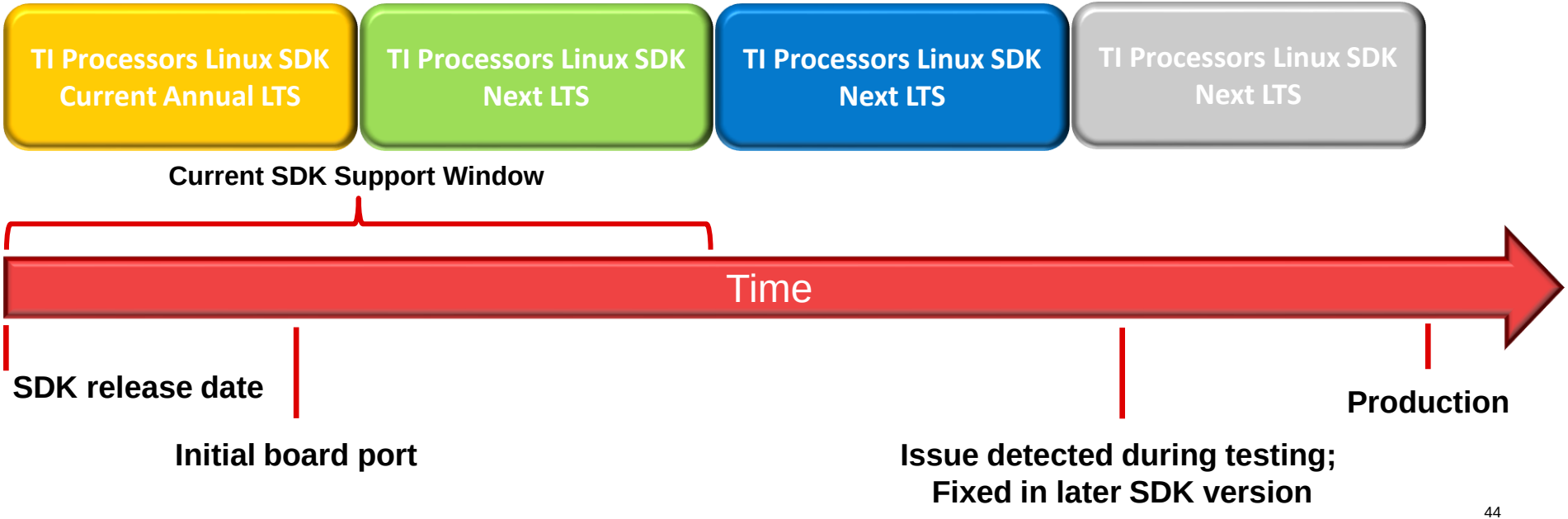
Production and Lifecycle

Product Timeline – Production UniFlash





Product Timeline – Lifecycle



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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265