Powering the AM335x With the TPS650250

This document details a power solution for the AM335x application processor with a TPS650250 power management unit (PMU) or power management IC (PMIC).

Portable application solution size demands a high level of integration and the AM335x requires at least three different voltage rails with specific power-on and power-off sequencing requirements. The TPS650250 is a highly integrated power solution that provides the 1.8-, 3.3-, and 1.1-V rail signals required by the AM335x. The TPS650250 has three step-down converters, three low-dropout (LDO) regulators, and a voltage supervisor.

This document can be used as a reference for connectivity between the TPS650250 and the AM335x.

Contents

1 Power Requirements 2
1.1 Power-On Sequence 3
1.2 Power-Off Sequence 3
2 Schematic 4
3 Waveforms 5
4 Bill of Materials 9
5 Use of a Clamping Circuit for Simultaneous Ramp Down 10
6 Using the TPS650250 to Support DDR3 or DDR3L 11
6.1 Adjusting DCDC2 Output Voltage to 1.5 V or 1.35 V 12
7 Conclusion 13
8 References 13

List of Figures

1 TPS650250 With Sequencing Circuit and AM335x Functional Block Diagram 2
2 TPS650250 Powering and Sequencing Circuit for the AM335x Powering Requirements 4
3 Power-On Sequence With PWRONRSTn 5
4 Power-On Sequence for the TPS650250 Converter Rails 6
5 Power-Off Sequence With PWRONRSTn 7
6 Power-Off Sequence for the TPS650250 Converter Rails 8
7 Clamping Circuit 10
8 TPS650250 Shutdown without Clamping Circuit 11
9 TPS650250 Shutdown with Clamping Circuit 11
10 DCDC2 Resistor Change (R14) to Achieve 1.5 V 12

List of Tables

1 AM335x Power Requirements 2
2 Bill of Materials 9
3 Clamp Circuit Testing 10
4 AM335x Power Requirements for Supporting DDR3 or DDR3L 11

Trademarks

Sitara is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

1 Power Requirements

Figure 1 shows a block diagram of the TPS650250-AM335x interface. Figure 2 shows a detailed circuit schematic of the power solution (TPS650250 and sequencing circuit).

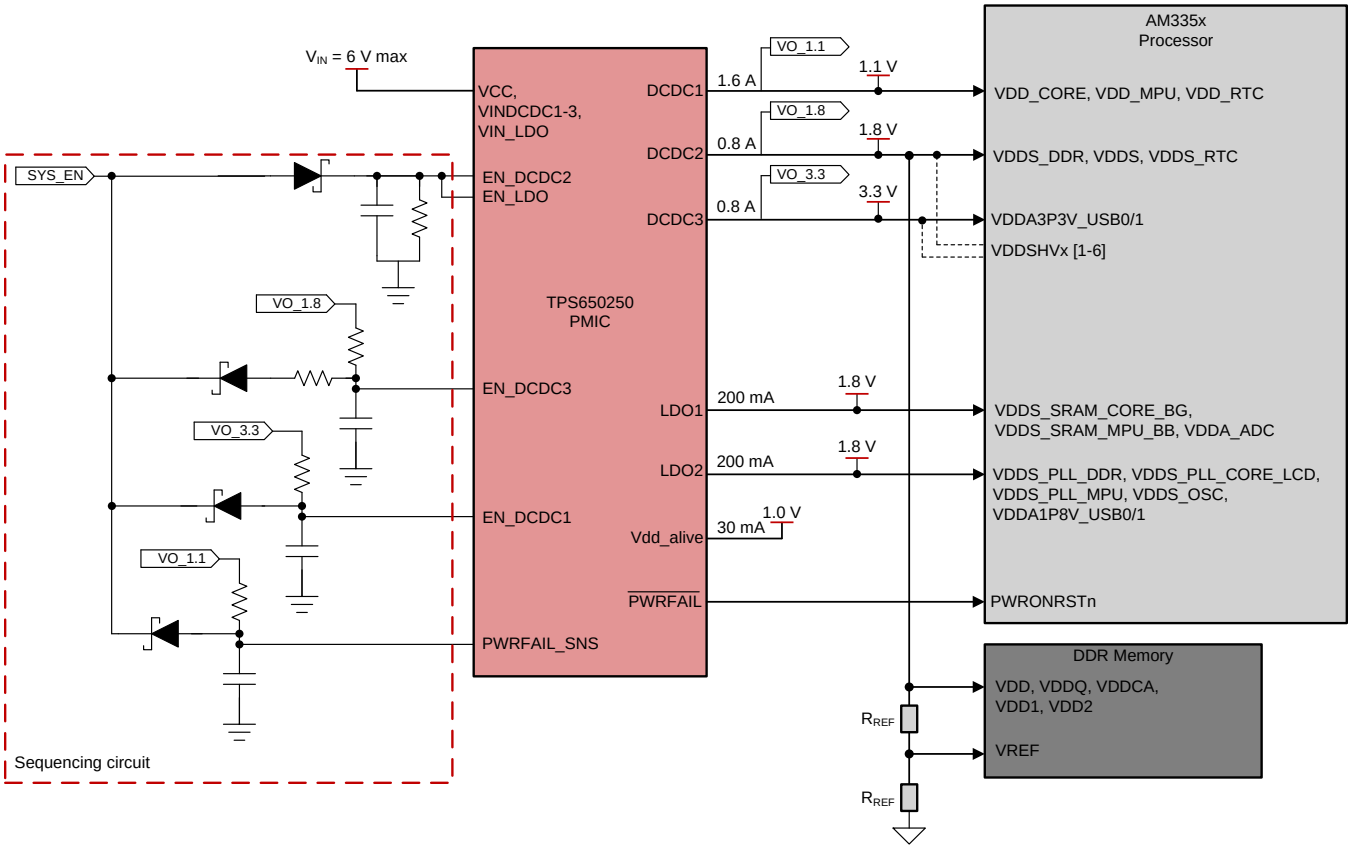


Figure 1. TPS650250 With Sequencing Circuit and AM335x Functional Block Diagram

Table 1 lists the AM335x power requirements.

Table 1. AM335x Power Requirements

TPS650250						AM335x			
Power-Up Sequence	Power-Down Sequence	Power Supply	V_{OUT} [V]	I_{OUT} [mA]	Output Voltage [V]	Power Supply	Nominal Rating	Grouping	Max Current [mA]
3	1	DCDC1	2.8, 3.3, Adjustable	1600	1.1	VDD_CORE, VDD_MPU, VDD_RTC	1.1 V ±4%	1.1-V Core	902
1	3	DCDC2	1.8, 2.5, Adjustable	800	1.8	VDDS_DDR, VDDS, VDDS_RTC, VDDSHVx	1.8 V ±5%	1.8-V IO	605
2	2	DCDC3	Adjustable	800	3.3	VDDA3P3V_USB0, VDDA3P3V_USB1, VDDSHVx	3.3 V ±5%	3.3-V Analog and IO	370
1	3	VLDO1	1-3.3	200	1.8	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC	1.8 V ±5%	1.8-V Analog	30
1	3	VLDO2	1-3.3	200	1.8	VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD, VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1	1.8 V ±5%	1.8-V Analog	125
		VLDO3	1.0	30	1.0	n/a	n/a	n/a	n/a

The TPS650250 meets these power requirements with its three step-down converters and three LDO regulators. A simple sequencing circuit is required to meet power-sequence requirements. This document details a power-sequencing solution for the RTC feature disable as described in the *AM335x Sitara™ Processors* data sheet and timing diagram, *Power Supply Sequencing with RTC Feature Disabled*.

1.1 Power-On Sequence

According to the excerpt from the AM335x datasheet, the device must be powered on in the following order:

1. 1.8-V Analog and I/O
2. 3.3-V Analog and I/O
3. 1.1-V Core

An external system enable signal, SYS_EN, is enabled HIGH for power up. Diodes D2, D3, and D4 are reversed biased. Diode D1 is forward biased and EN1.8 is HIGH. This turns ON the 1.8-V rails DCDC2, LDO1, and LDO2. The output voltage of the DCDC2 converter, VO_1.8, is filtered into the enable of the DCDC3 converter EN3.3 and creates an RC (R7 and C12) delay before turning ON the 3.3-V rail. When EN3.3 reaches the turn-on threshold of the converter, VO_3.3 ramps up to nominal voltage. The output voltage of the DCDC3 converter, VO_3.3, is filtered into the enable of the DCDC1 converter EN1.1 and creates an RC (R16 and C15) delay before turning ON the 1.1 V rail. When EN1.1 reaches the turn-on threshold of the converter, VO_1.1 ramps up to nominal voltage. Lastly, the output voltage of the DCDC1 converter VO_1.1 is filtered into the power sense fail pin of the TPS650250 PWRRAIL_SNS and creates an RC (R17 and C16) delay between the last rail turning on and the Power On Reset signal, PWRONRSTn, pulling HIGH. The PWRFAIL_SNS signal is sensed through an internal comparator in the TPS650250 and triggers the PWRONRSTn signal HIGH when PWRRAIL_SNS reaches 1 V.

Power-on sequence is complete.

Figure 2 shows the correct connections for this power-on sequencing.

1.2 Power-Off Sequence

As shown in the excerpt from the AM335x data sheet, the device must be powered off in reverse order as power-on.

1. 1.1-V Core
2. 3.3-V Analog and I/O
3. 1.8-V Analog and I/O

SYS_EN is LOW for power down. D2, D3, and D4 are forward biased. PWRFAIL_SNS becomes LOW to pull PWRONRSTn LOW. EN1.1 becomes LOW and VO_1.1 ramps down. EN3.3 signal is filtered to create an RC (R3 and C12) delay between VO_1.1 ramping down and VO_3.3 ramping down. Lastly, D1 is reversed biased and capacitor C11 discharges through resistor R2 with a delay longer than the ramping down of VO1.1 and VO3.3. After VO1.1 and VO3.3 are off, the 1.8-V rail ramps down.

Power-off sequence is complete.

Figure 2 shows the correct connections for this power-off sequencing.

2 Schematic

Figure 2 shows the circuit schematic detailing the external components required by the TPS650250 to achieve the 1.8-, 3.3-, and 1.1-V power rails required by the AM335x. In addition, Figure 2 shows the sequencing circuit that achieves the proper power-on, power-off, and PWRONRSTn sequencing required by the AM335x.

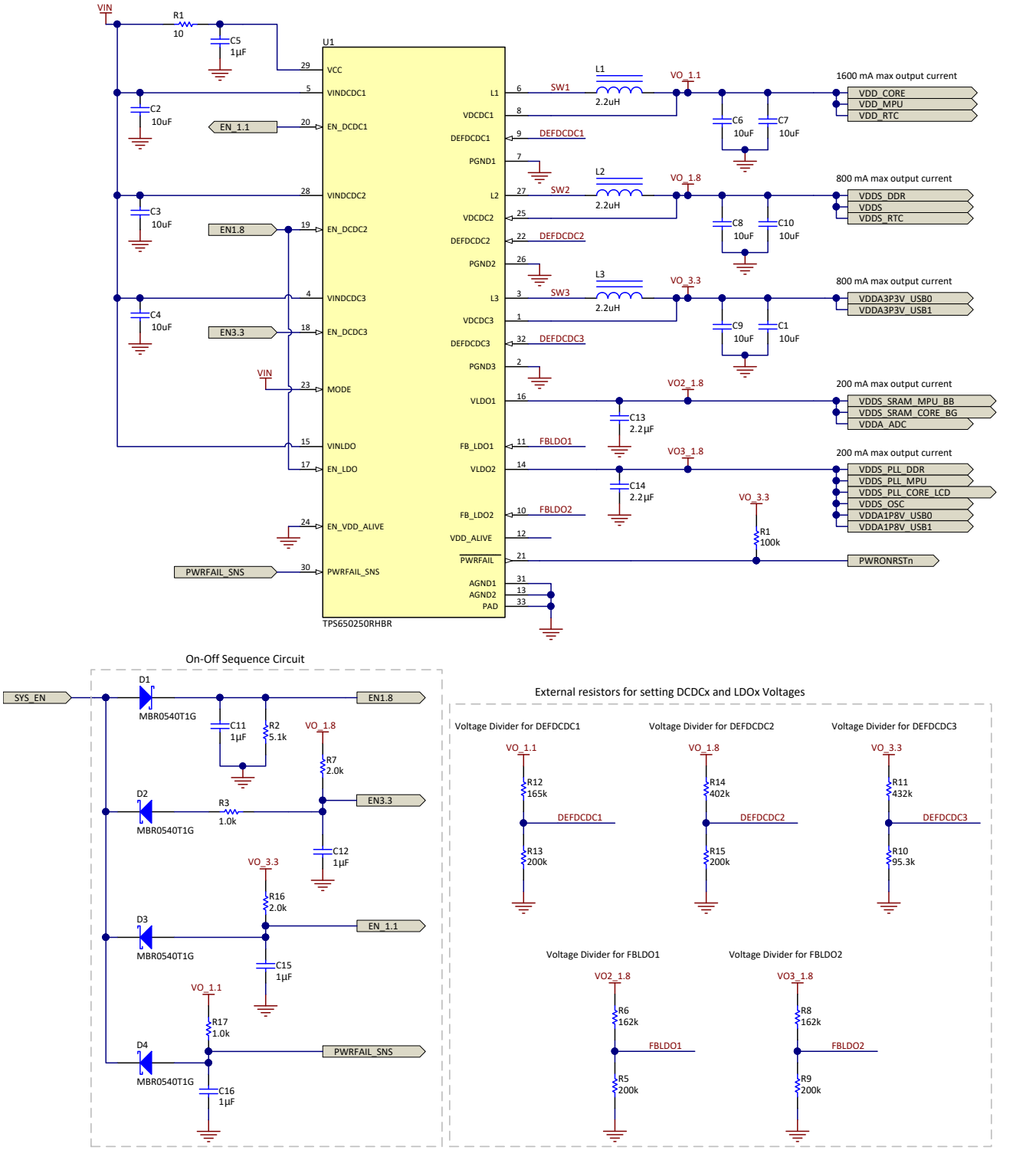
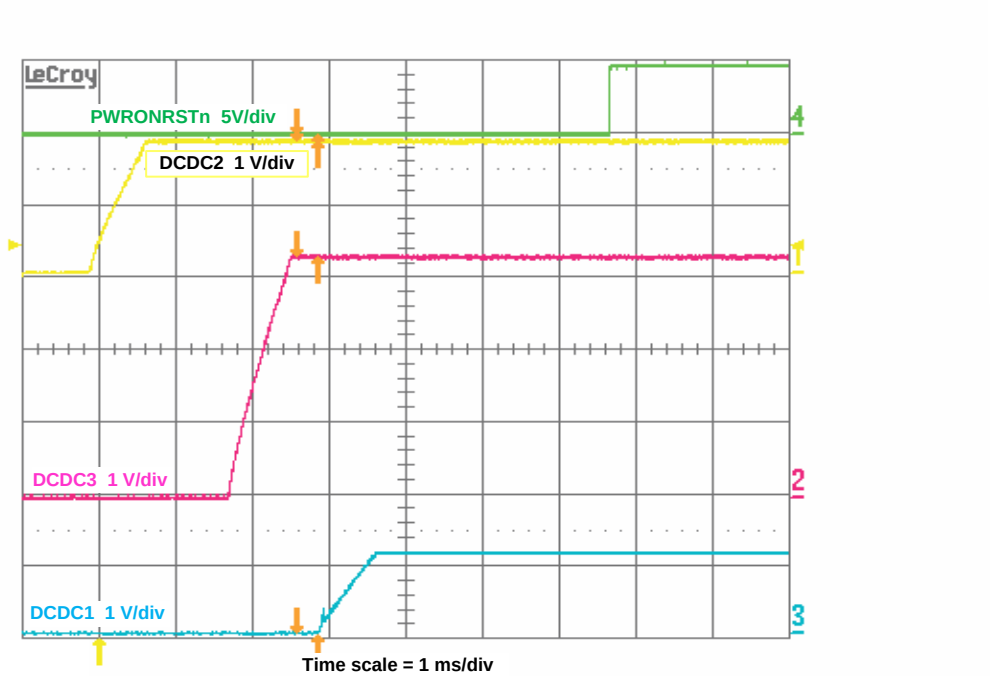


Figure 2. TPS650250 Powering and Sequencing Circuit for the AM335x Powering Requirements

3 Waveforms

The following waveforms demonstrate the power-on and power-off sequence of the TPS650250 as required by the AM335x.

Figure 3 shows the power-on sequence for each of the output voltage rails and the PWRONRSTn signal. The 1.8-, 3.3-, and 1.1-V rails turn on sequentially and the PWRONRSTn signal goes HIGH after all rails are ON.



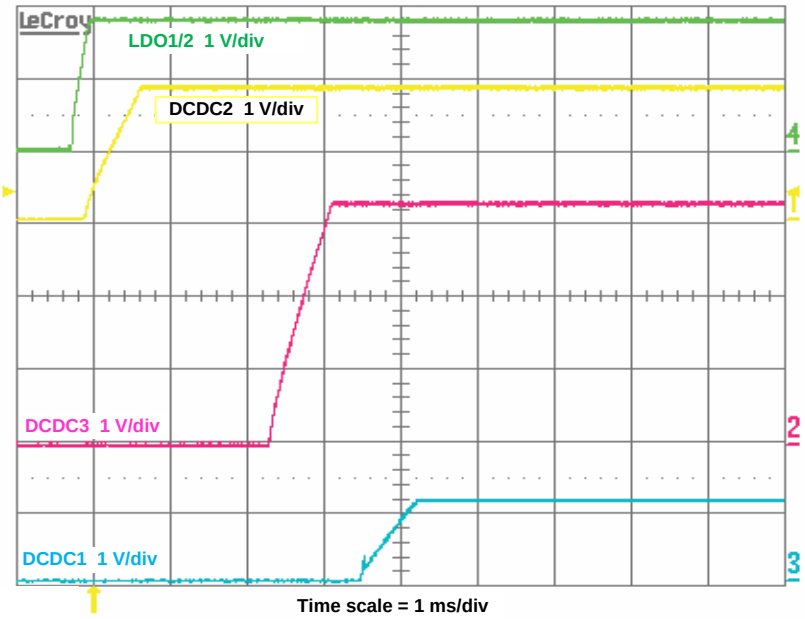
1.8-V (DCDC2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 3. Power-On Sequence With PWRONRSTn

Figure 4 shows the power-on sequence for each of the output voltages of the TPS650250. DCDC2 (1.8 V) and the LDOs (1.8 V) of the TPS650250 turn on before DCDC3 (3.3 V) and DCDC1 (1.1 V).

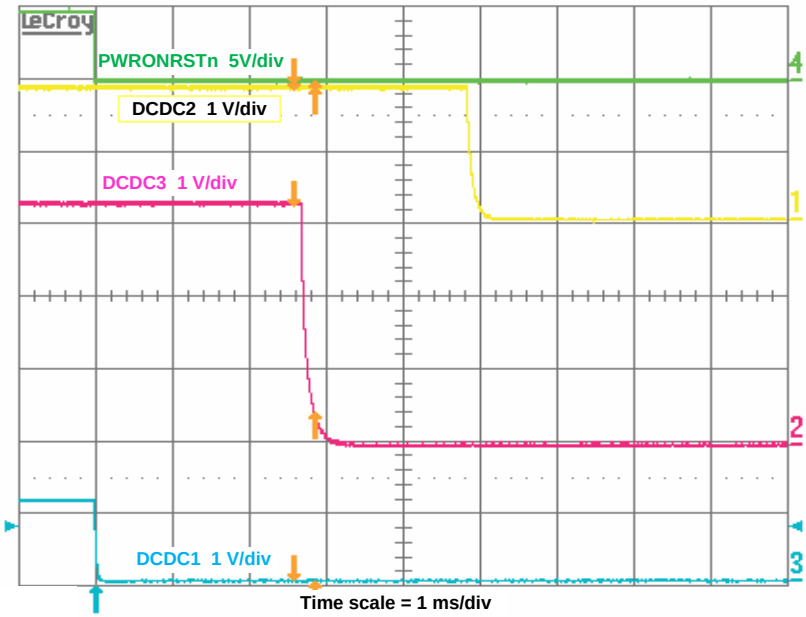
Figure 5 shows the power-off sequence for each of the output voltage rails and the PWRONRSTn signal. The 1.8-, 3.3-, and 1.1-V rails turn off sequentially and the PWRONRSTn signal goes LOW when the 1.1-V rail begins to ramp down.

Figure 6 shows the power-off sequence for each of the output voltages of the TPS650250. DCDC2 (1.8 V) and the LDOs (1.8 V) of the TPS650250 turn off after DCDC1 (1.1 V) and DCDC3 (3.3 V) have ramped down.



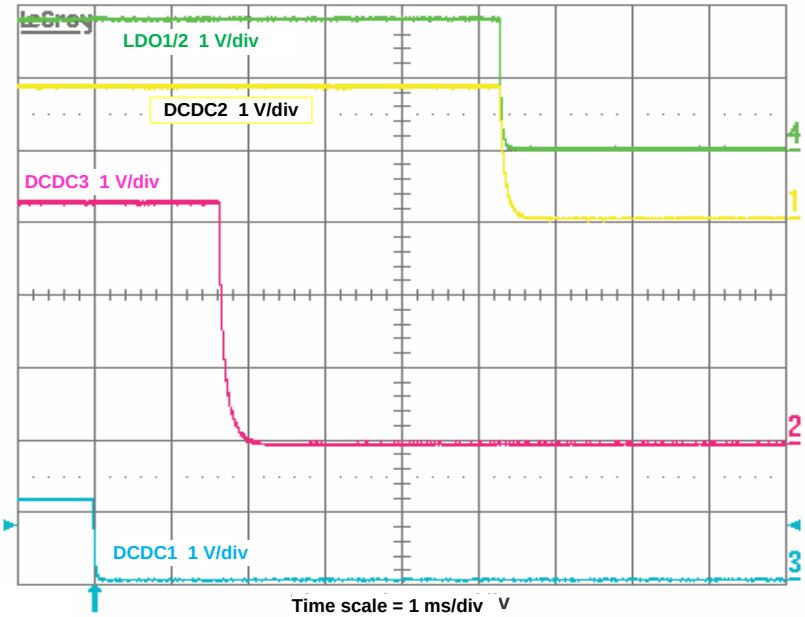
1.8-V (DCDC2,LDO1/2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 4. Power-On Sequence for the TPS650250 Converter Rails



1.8-V (DCDC2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 5. Power-Off Sequence With PWRONRSTn



1.8-V (DCDC2,LDO1/2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 6. Power-Off Sequence for the TPS650250 Converter Rails

4 Bill of Materials

Table 2 lists the bill of materials (BOM).

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C2	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C3	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C4	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C5	1.0 µF	Capacitor, ceramic, 6.3 V, X5R,10%	0603	Std	Std
1	C6	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C7	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C8	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C9	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C10	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C11	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C12	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C13	2.2 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	Std	Std
1	C14	2.2 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	Std	Std
1	C15	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C16	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	D1	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D2	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D3	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D4	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	L1	2.2 µH	Inductor, SMT, 1.72 A, 59 mΩ	0.157 × 0.157 inch	VLCF4020T-2R2N1R7	TDK
1	L2	3.3 µH	Inductor, SMT, 1.52 A, 78 mΩ	0.157 × 0.157 inch	VLCF4020T-3R3N1R5	TDK
1	L3	2.2 µH	Inductor, SMT, 1.72 A, 59 mΩ	0.157 × 0.157 inch	VLCF4020T-2R2N1R7	TDK
1	R1	100 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R2	5 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R3	1 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R4	1 Ω	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R5	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R6	162 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R7	2 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R8	162 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R9	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R10	95.3 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R11	432 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R12	165 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R13	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R14	402 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R15	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R16	2 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R17	1 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	U1	TPS650250	IC, Power Management ICs for Li-Ion Powered Systems	QFN-32	TI	

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG components.

5 Use of a Clamping Circuit for Simultaneous Ramp Down

Ramping down the VDDS and VDDSHVx [1–6] power rails for the AM335x processor at the same time presents a challenge that is made clear in the *AM335x Sitara™ Processors* data sheet. For this power design, the following statement only refers to the DCDC2 rail named VO_1.8 (1.8-V for VDDS of the processor) and the DCDC3 rail named VO_3.3 (3.3-V for VDDSHVx of the processor):

> If it is desired to ramp down VDDS and VDDSHVx [1–6] simultaneously, it should always be ensured that the difference between VDDS and VDDSHVx [1–6] during the entire power-down sequence is < 2 V. If this is violated it can result in reliability risks for the device.

The worst-case scenario of this issue is the 3.3-V rail remains high possibly because of large output capacitance or no load being present on the output while, the 1.8-V rail ramps down quickly such as if it were fully loaded.

A solution to this issue is the use of a clamping circuit between the 1.8-V VDDS and 3.3-V VDDSHVx rails, ensuring proper shutdown when V_{IN} is removed. As illustrated in Figure 7, the clamping circuit suggested is only five additional components, 3 of which are resistors. The 3.3-V VDDSHVx rail powered by DCDC3 is shown using the net name VO_3.3 as defined by the schematic in Figure 2. The 1.8-V VDDS rail powered by DCDC2 is shown using the net name VO_1.8 as defined by the schematic. The TLVH431 is regulated at 1.5 V through resistor divider R1 and R2. Before the rails ramp down, Q1 is off. When the 1.8-V rail drops, Vbase drops and Q1 turns ON. The 3.3-V rail discharges through Q1 and the 1.8-V rail. This technique ensures that the difference between the 3.3-V VDDSHVx rails and the 1.8-V VDDS rail never exceeds 2 V.

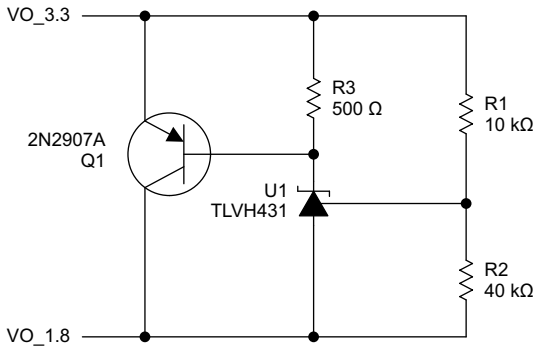


Figure 7. Clamping Circuit

Figure 8 shows the power-down sequence for the DCDCs, LDOs and PWRONRSTn outputs and signals of the TPS650250 without the clamping circuit. This is the worst-case scenario since the VDDSHVx 3.3-V rail is not loaded at all while the VDDS 1.8-V rail is fully loaded. Notice that the difference between DCDC3 and DCDC2 (VDDSHVx and VDDS) exceeds 2 V. Table 3 lists details of the testing performed to identify this violation of the AM335x data sheet.

Figure 9 shows the power-down sequence for the DCDCs, LDOs and PWRONRSTn output voltages of the TPS650250 with the clamping circuit. With the same load conditions, the clamp circuit test results show the difference between DCDC3 and DCDC2 is kept below 2 V. Notice how the 3.3-V rail tracks the 1.8-V rail. Refer to Table 3 for more testing details.

Table 3. Clamp Circuit Testing

Rail	Steady-State V_{OUT} [V]	Net Name	Load Current [mA]
DCDC2	1.8	VO_1.8	600
DCDC3	3.3	VO_3.3	0.01
DCDC3 – DCDC2	(3.3 – 1.8) = 1.5	(VO_3.3 – VO_1.8)	n/a

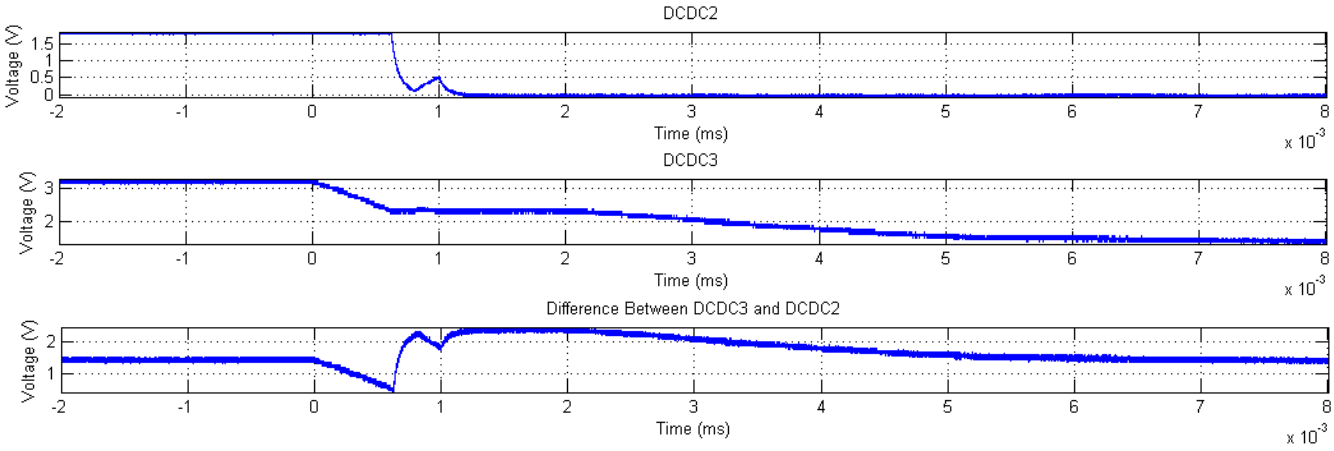


Figure 8. TPS650250 Shutdown without Clamping Circuit

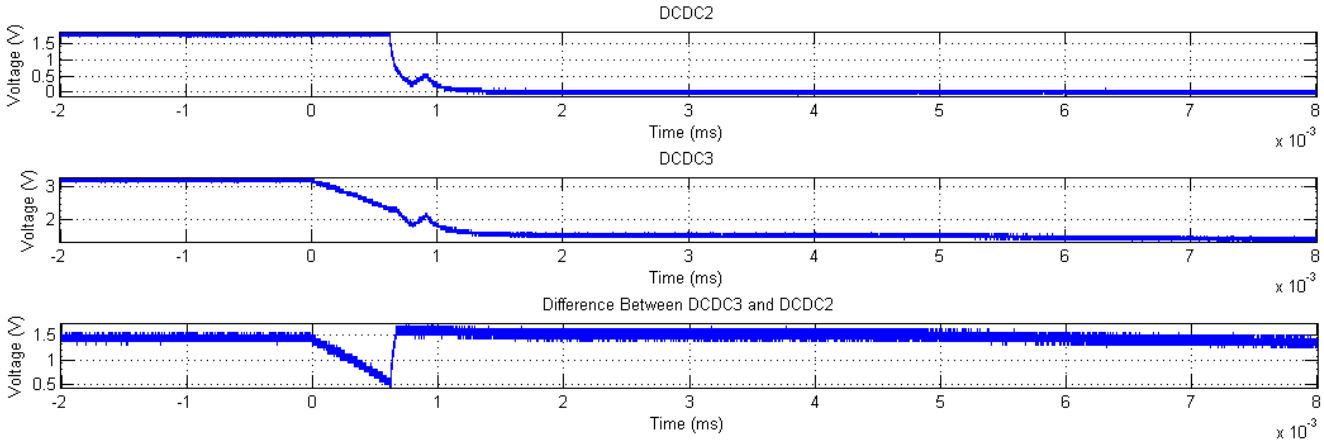


Figure 9. TPS650250 Shutdown with Clamping Circuit

6 Using the TPS650250 to Support DDR3 or DDR3L

The TPS650250 provides the power required by the AM335x and is capable of supporting external DDR3 or DDR3L memory applications. However, the 1.8-V I/O output current capabilities are reduced from what was presented in Section 1. Table 4 shows the power requirements for powering the AM335x with DDR3 or DDR3L support.

Table 4. AM335x Power Requirements for Supporting DDR3 or DDR3L

TPS650250						AM335x			
Power-Up Sequence	Power-Down Sequence	Power Supply	V_{OUT} [V]	I_{OUT} [mA]	Output Voltage [V]	Power Supply	Nominal Rating	Grouping	Max Current [mA]
4	1	DCDC1	2.8, 3.3, Adjustable	1600	1.1	VDD_CORE, VDD_MPU, VDD_RTC	1.1 V ± 4%	1.1-V Core	902
2	3	DCDC2	1.8, 2.5, Adjustable	800	1.5, 1.35	VDDS_DDR	1.5 V ± 5%, 1.35 ± 5%	1.5-V (DDR3), 1.35-V (DDR3L)	300
3	2	DCDC3	Adjustable	800	3.3	VDDA3P3V_USB0, VDDA3P3V_USB1, VDDSHVx	3.3 V ±5%	3.3-V Analog and IO	370

Table 4. AM335x Power Requirements for Supporting DDR3 or DDR3L (continued)

TPS650250						AM335x			
Power-Up Sequence	Power-Down Sequence	Power Supply	V_{OUT} [V]	I_{OUT} [mA]	Output Voltage [V]	Power Supply	Nominal Rating	Grouping	Max Current [mA]
1	4	VLDO1	1–3.3	200	1.8	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC, VDDSHVx,VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD, VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1	1.8 V ± 5%	1.8-V Analog	155
1	4	VLDO2	1–3.3	200	1.8	VDDS, VDDS_RTC, VDDSHVx	1.8 V ± 5%	1.8-V IO	55
		VLDO3	1.0	30	1.0	n/a	n/a	n/a	n/a

On the TPS650250, DCDC2 is dedicated to 1.5 V to support external DDR3 applications. The AM335x DDR3 I/O domain (VDDS_DDR) must be 1.5 V, leaving 500 mA of available current for external DDR3 memory. The output voltage of DCDC2 is set to 1.35 V to support DDR3L with lower supply voltage.

The 1.8-V I/O domains (VDDSHVx) are now powered through the 1.8-V rails, VLDO1 and VLDO2, of the TPS650250. The added loads cause current constraints on LDO1 and LDO2 so as not to go over the rated current of 200 mA. Therefore, the AM335x must be operated such that VDDSHVx does not cause each LDO current to exceed 200 mA on VLDO1 or VLDO2.

6.1 Adjusting DCDC2 Output Voltage to 1.5 V or 1.35 V

A 1.5-V rail is required to power DDR3. If R15 is 200 kΩ, change R14 to 301 kΩ to adjust the output voltage of DCDC2 to 1.5 V. Figure 10 shows this change of the resistor divider for DCDC2.

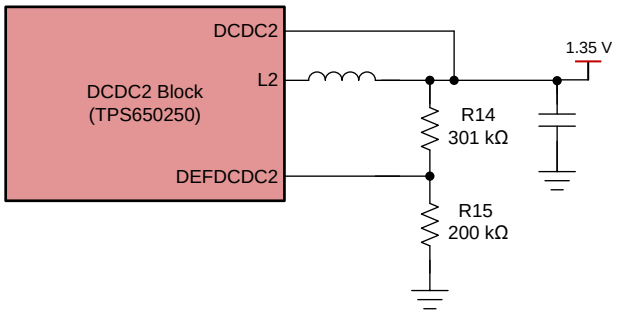


Figure 10. DCDC2 Resistor Change (R14) to Achieve 1.5 V

A 1.35-V rail is required to power DDR3L. If R15 is kept as 200 kΩ, change R14 to 255 kΩ to adjust the output voltage to 1.35 V.

7 Conclusion

The TPS650250 provides a low-cost, comprehensive power solution for the AM335x. This reference design demonstrates the external components of the TPS650250 to provide the required voltage rails and a simple sequencing circuit that meets power-on and power-off sequencing required by the AM335x. For external DDR3 applications, the output voltage of DCDC2 for the TPS650250 can be easily adjusted to accommodate a 1.5-V rail. However, this limits the output-current capabilities of the 1.8-V I/O Domains (VDDSHVx) in the AM335x. If simultaneous ramp down of the VDDSHVx and VDDS rail is desired a clamping circuit may be required.

8 References

1. Texas Instruments, *TPS650250 Power Management IC for Li-Ion Powered Systems* data sheet
2. Texas Instruments, *AM335x, AM335x ARM® Cortex™-A8 Microprocessors (MPUs)* data sheet

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (December 2012) to B Revision	Page
• Updated resolution and clarity of all figures	2
• Clarified terminology and test data in the *Use of a Clamping Circuit for Simultaneous Ramp Down* section	10
• Moved the *Use of a Clamping Circuit for Simultaneous Ramp Down* section to before the *Using the TPS650250 to Support DDR3* section	10
• Added support for DDR3L (1.35 V) in the *Using the TPS650250 to Support DDR3* section	12

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265