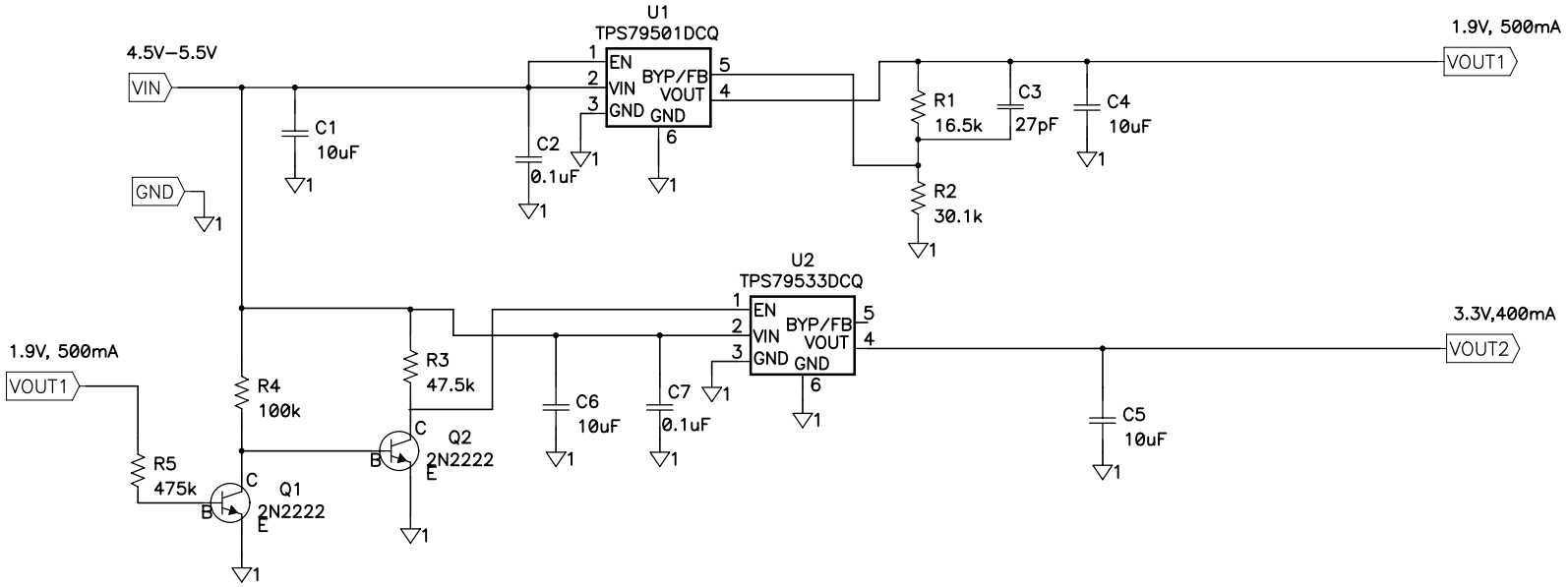

TEXAS INSTRUMENTS

Title: F2833x Power Reference Design		
Size: B	Number: PMP3782	Rev: A
Date: 03/31/08		Drawn by: K Ohn
Filename: PMP3782.sch		Sheet: of

Filename: PMP3782_bom.xls

Date: 04/16/2008

PMP3782 BOM

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C3	27pF	Capacitor, Ceramic, 50V, COG, 5%	0402	C1005C0G1H270JT	TDK
4	C1, C4, C5, C6	10uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	C2012X5R1A106K	TDK
2	C2, C7	0.1uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	GRM39X7R104K016A	Murata
2	Q1, Q2	2N2222	Transistor, NPN, 40V, 600mA, 225mW	TO-92	MMBT2222ALT1	Fairchild
1	R1	16.5k	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R2	30.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	47.5k	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R4	100k	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R5	475k	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	U1	TPS79501DCQ	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF, 500mA, xxV	SOT223-6	TPS795xxDCQ	TI
1	U2	TPS79533DCQ	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF, 500mA, xxV	SOT223-6	TPS795xxDCQ	TI

1 Power Up

The figure below shows the startup waveforms after ENABLE is applied. The outputs voltages shown are at full load. (Enable=5.00V/div, 1.9-V=1.00V/div, 3.3-V=1.00V/div, 50us/div)

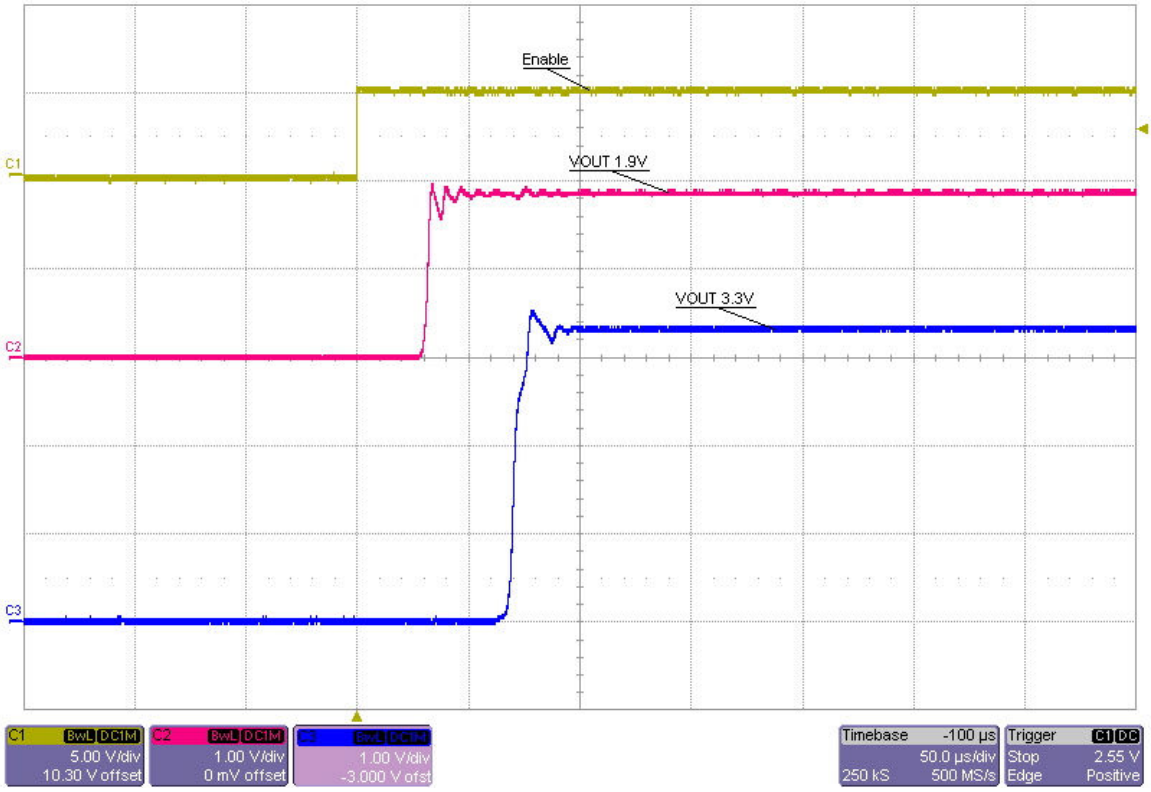

Figure 1. Power Up with 5-V Input and ENABLE Voltage

Once ENABLE is pulled high, the 1.9-V rail comes up and 3.3-V rail comes up later.

2 Power Down

The figure below shows the power down waveforms after ENABLE is pulled low. The outputs voltages shown are at full load. (Enable=5.00V/div, 1.9-V=1.00V/div, 3.3-V=1.00V/div, 200us/div)

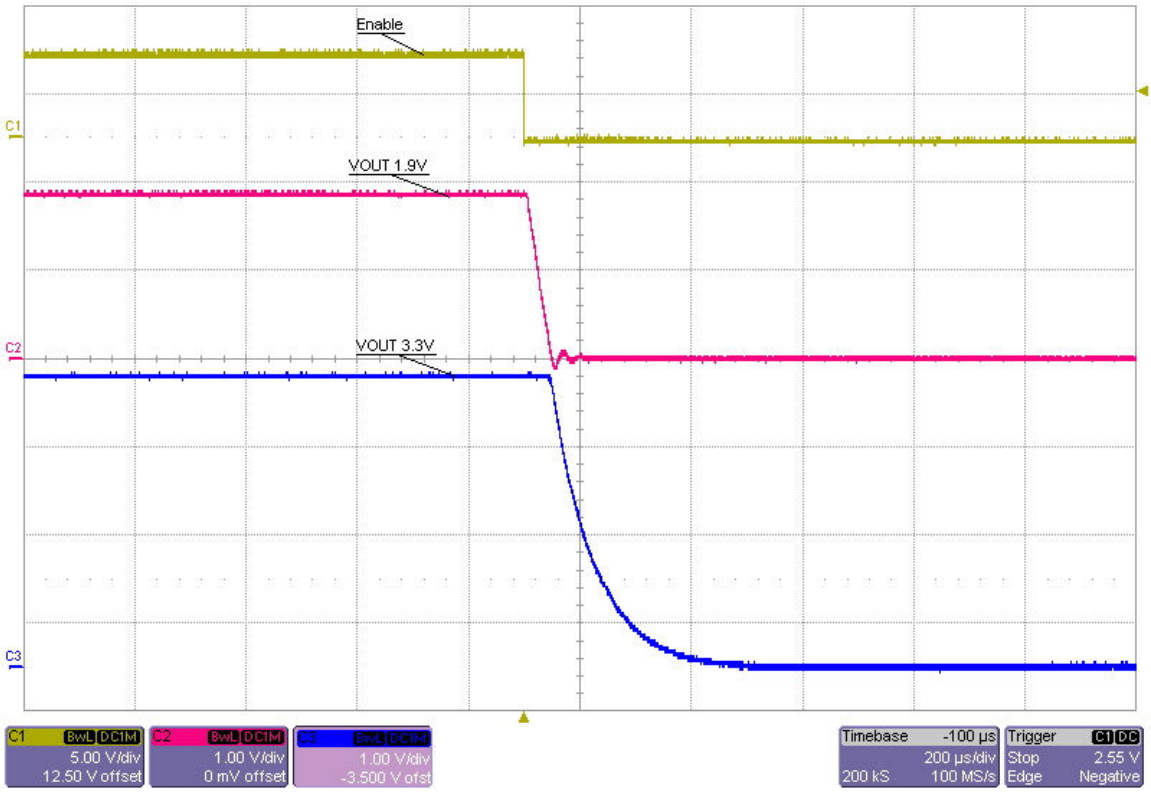

Figure 2. Power Down with 5-V Input and ENABLE Voltage

Once ENABLE is pulled low, the 1.9-V rail starts to come down first, and 3.3V comes down after 50us.

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