

Considering TI Smart DACs As an Alternative to 555 Timers



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ABSTRACT

The 555 timer is a versatile integrated circuit that has been used by system designers for decades to solve a variety of system needs. Texas Instruments family of smart digital-to-analog converters (DACs) combines multiple mixed-signal blocks in a manner that also offers versatility and can be configured to solve many of the same system needs as a 555 timer. This application note reviews popular 555 timer configurations and shows how the same function can be met using a TI smart DAC. Trade-offs between the two approaches are reviewed and conclusions are presented on which type of device fits best to each application.

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1 Introduction

For decades the 555 timer has enabled system designers to create solutions for a variety of applications, including oscillators, pulse generation, and converting analog signals to pulse width modulated (PWM) signals. Depending on the 555 timer configuration, there can be limits to how flexible the device is in meeting the system designer's need, whether it be due to the structure of the internal blocks or the tolerances of the external components used to construct the complete circuit.

Texas Instrument's new family of smart DACs are capable of voltage output configurable waveform generation and include configurable threshold blocks that can be used to exceed the functionality of 555 timer circuits in most cases. The following sections explore a handful of common 555 timer circuits and present the alternative smart DAC solution.

2 Functional Overview of 555 Timers vs. Smart DACs

A block diagram of the 555 timer is shown in [Figure 2-1](#). It consists of an internal resistor divider between the supply voltage (VDD) and ground (GND) with each resistor equaling a nominal value of 100 kΩ. The THRESH and TRIG pins are direct inputs to the two input comparators and the CONT pin gives the user a direct input to the inverting input of the high comparator. The trigger levels of these two comparators are set to $\frac{1}{3} \times VDD$ and $\frac{2}{3} \times VDD$ due to the internal resistor divider made up of three equal resistors. Applying a voltage to the CONT pin changes the trigger levels to $\frac{1}{2} \times V_{CONT}$ and V_{CONT} . The outputs of the two comparators are fed to a flip-flop and the output of the flip-flop is sent to the base of an NPN transistor (in the case of a bipolar 555 timer) or gate of an NMOS transistor (in the case of a CMOS 555 timer) which functions as the discharge path of the device and is also sent through an inverter to the OUT pin. Therefore, when OUT is high, the discharge path between the DISCH pin and GND is disabled and when OUT is low, the discharge path is enabled. Collections of various external components can be used with these blocks to create many functional circuits.

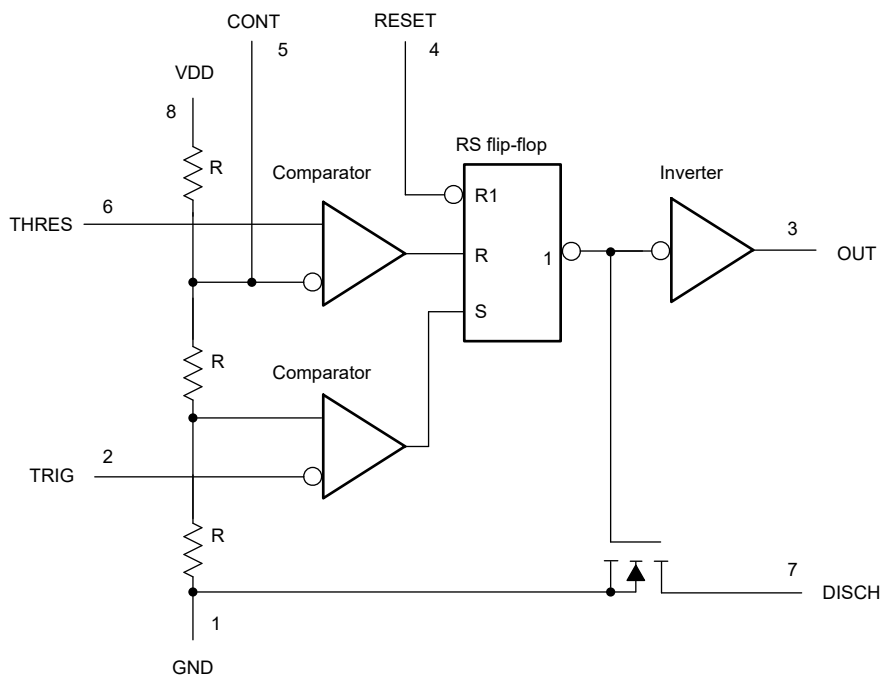


Figure 2-1. Functional Block Diagram of a 555 Timer

A block diagram of the **DAC53701** smart DAC is shown in **Figure 2-2**. A typical smart DAC consists of a I²C or SPI digital interface, a precision internal reference, and a string DAC. The internal voltage output buffer has an exposed feedback path available that can sense the output voltage. An additional feature common to smart DACs is non-volatile memory (NVM) which can store the register settings of the smart DAC for use in the field without a microcontroller. Smart DACs have general purpose input (GPI) pin handling that can be configured to control various register settings or output states. A power down logic block is included to set the output state of the smart DAC to modes such as high impedance (Hi-Z) power down, or 10-k Ω to GND power down. One final common feature of smart DACs is a continuous waveform generation (CWG) mode that can produce triangular, sawtooth, square, or sine waveforms. These features can be applied in circuits that will be discussed in the upcoming sections.

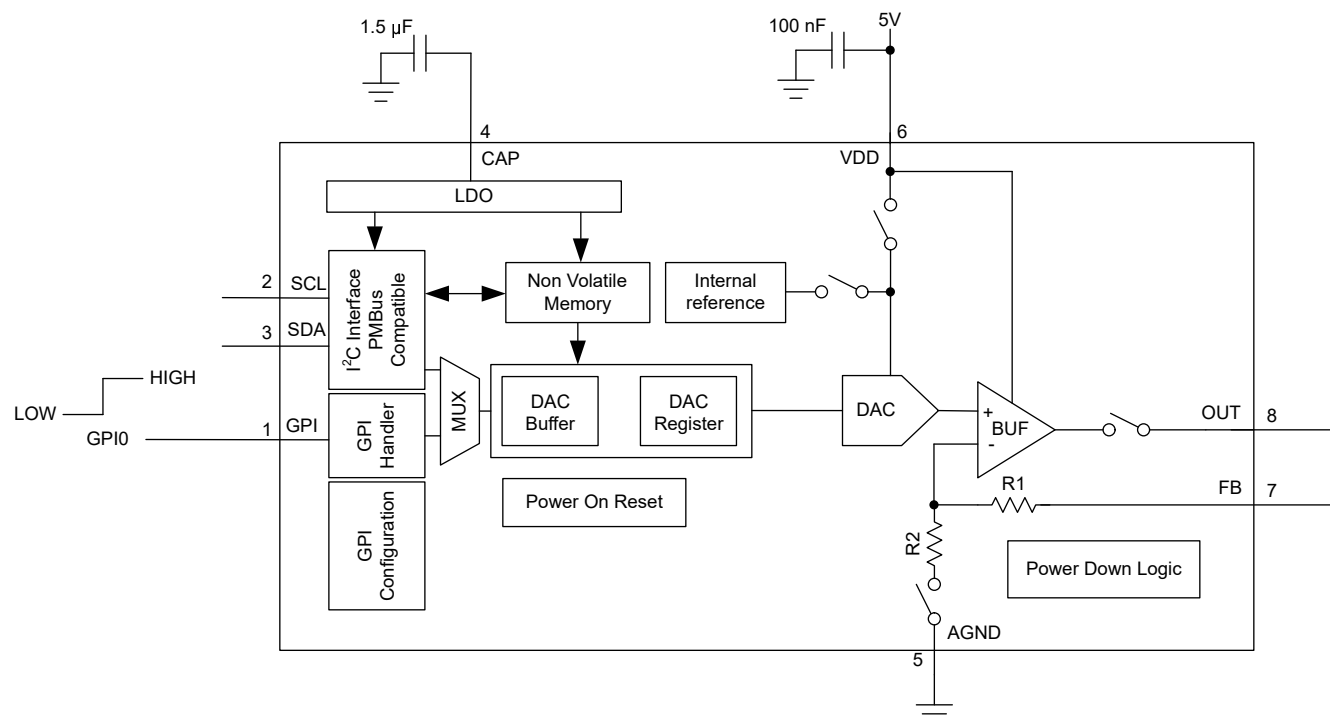


Figure 2-2. Functional Block Diagram of the DAC53701 Smart DAC

3 Pulse Generator with Variable Frequency and Variable Duty Cycle

The designer can use the 555 timer in a stable operation to create an output pulse train with variable frequency and variable duty cycle. If 50% duty cycle is required, the simpler configuration shown in [Figure 3-1](#) can be used. If a duty cycle other than 50% is required, the configuration shown in [Figure 3-3](#) can be used.

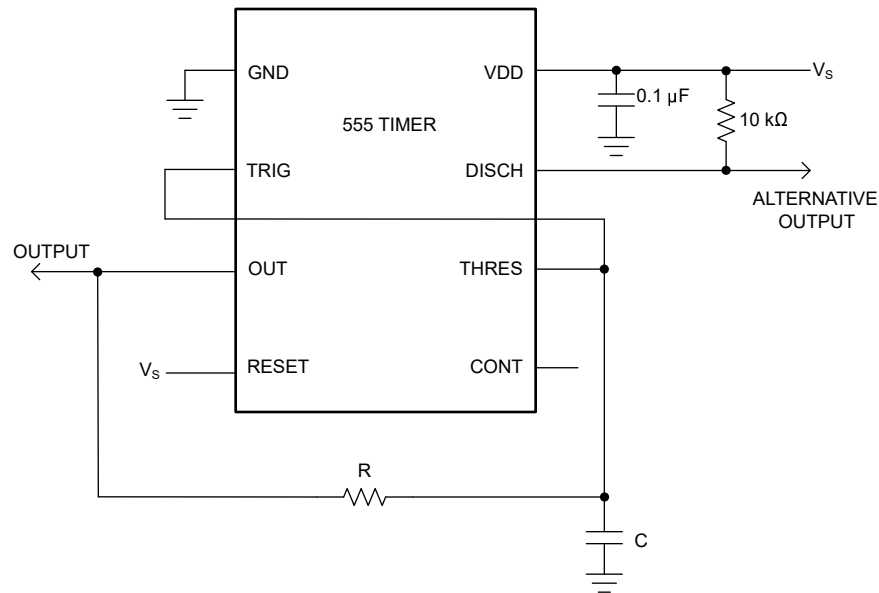


Figure 3-1. 555 Timer Configured for a 50% Duty Cycle Oscillator

In the 50% duty cycle configuration, the circuit is configured with the TRIG and THRESH pins tied together, which causes the circuit to re-trigger after every timing cycle. During each cycle, the capacitor charges up to the upper comparator limit of $\frac{2}{3} \times VDD$ through the external R and C and then discharges down to the lower comparator limit of $\frac{1}{3} \times VDD$ through the same external R and C. Using [Equation 1](#) for the capacitor voltage (V_{CAP}) in an RC circuit, it is shown that the time to charge from $\frac{1}{3} \times VDD$ to $\frac{2}{3} \times VDD$ is equal to [Equation 3](#):

$$V_{CAP}(t) = V(1 - e^{-t/RC}) \quad (1)$$

$$t = -RC \times \ln\left(1 - \frac{V_C(t)}{V}\right) \quad (2)$$

If $V = VDD$, $V_{CAP}(t_1) = \frac{1}{3} \times VDD$, and $V_{CAP}(t_2) = \frac{2}{3} \times VDD$, [Equation 2](#) can be rewritten as:

$$t_{charge} = t_2 - t_1 = -RC \times \ln\left(\frac{1}{3}\right) + RC \times \ln\left(\frac{2}{3}\right) = 0.693 \times RC \quad (3)$$

Because the discharge time from $\frac{2}{3} \times VDD$ to $\frac{1}{3} \times VDD$ uses the same external R and C, the discharge time is equal to [Equation 3](#):

$$t_{discharge} = 0.693 \times RC \quad (4)$$

The equal charge and discharge times produce a 50% duty cycle waveform with the frequency defined in [Equation 5](#):

$$f = \frac{1}{t_{charge} + t_{discharge}} = \frac{1}{1.386 \times RC} \quad (5)$$

During a charging event, the OUT pin retains a high state and during a discharge event the OUT pin holds a low state. The 50% duty cycle configuration relies on OUT having a high voltage output (VOH) and low voltage output (VOL) be driven symmetrically with respect to the supply rails for t_{charge} to equal $t_{\text{discharge}}$. This symmetry is a characteristic of CMOS 555 timers. A bipolar 555 timer does not have symmetrical VOH/VOL characteristics and would not yield a 50% duty cycle in this configuration.

Figure 3-2 shows the resulting waveforms for a 1.5-kHz waveform with 50% duty cycle. Note that the DISCH pin can be used as an alternate output with drive characteristics on the discharge path and an external pull-up resistor.

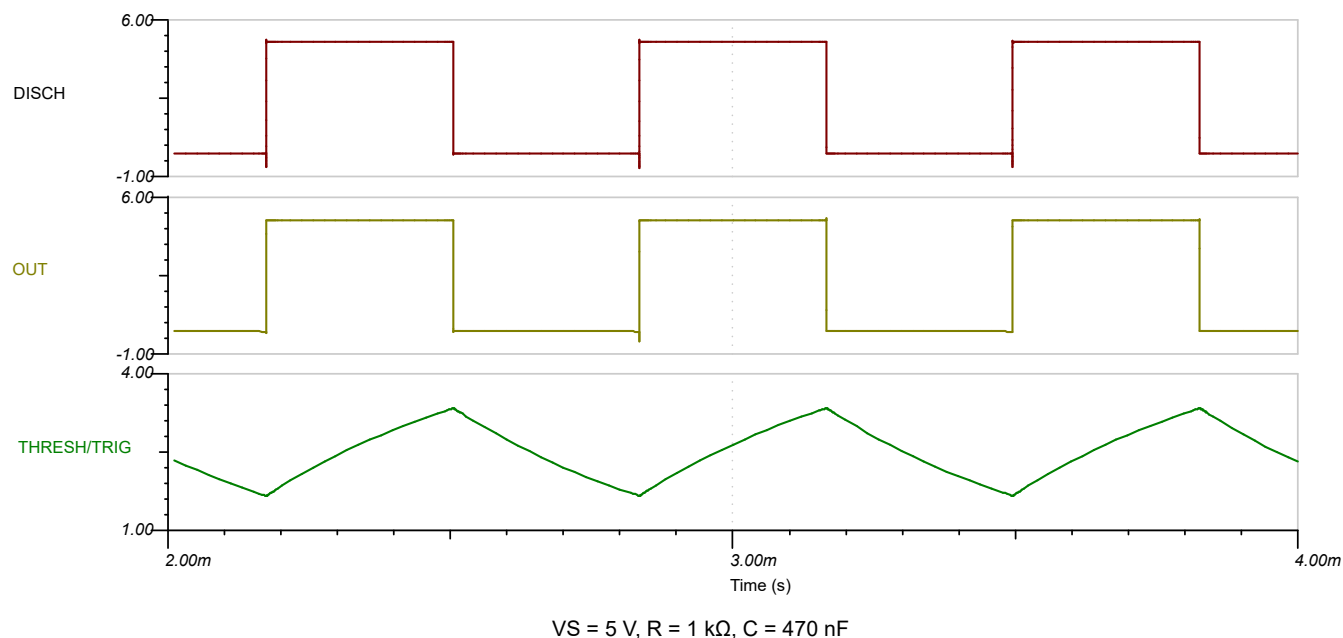


Figure 3-2. TINA-TI Simulation Results for a 50% Duty Cycle Oscillator Using a 555 Timer

In the variable duty cycle configuration shown in Figure 3-3 the circuit is also configured with the TRIG and THRESH pins tied together, but the resistor and capacitor configuration is changed such that the capacitor charges through both R_A and R_B and the capacitor discharges through only R_B .

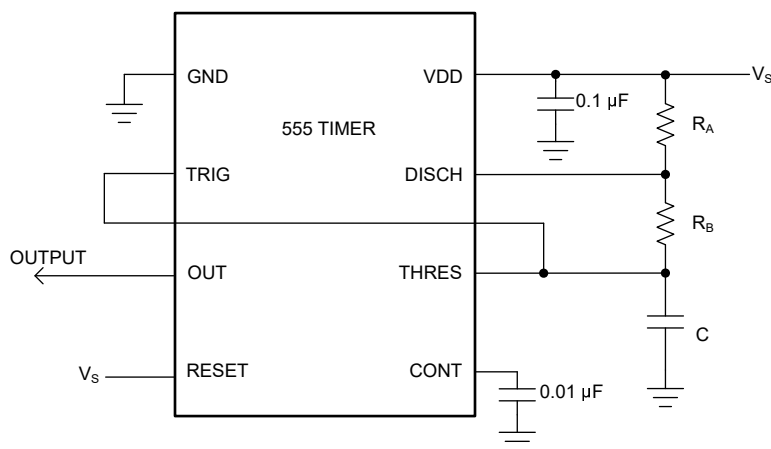


Figure 3-3. 555 Timer Configured for a Variable Duty Cycle Oscillator

This creates the asymmetric charge and discharge timings of Equation 6 and Equation 7. During a charge event, the OUT pin holds a high state and during a discharge event the OUT pin holds a low state. The configurable charge and discharge times produce a variable duty cycle waveform with the frequency defined in Equation 8 and a duty cycle defined in Equation 9.

$$t_{charge} = 0.693 \times (R_A + R_B) \times C \quad (6)$$

$$t_{discharge} = 0.693 \times R_B C \quad (7)$$

$$f = \frac{1}{t_{charge} + t_{discharge}} = \frac{1}{0.693 \times (R_A + 2R_B) \times C} \quad (8)$$

$$Duty\ Cycle = \frac{t_{charge}}{t_{charge} + t_{discharge}} = \frac{R_A + R_B}{R_A + 2R_B} \quad (9)$$

Figure 3-4 shows the resulting waveforms for a 1.5-kHz output with a 62.5% duty cycle.

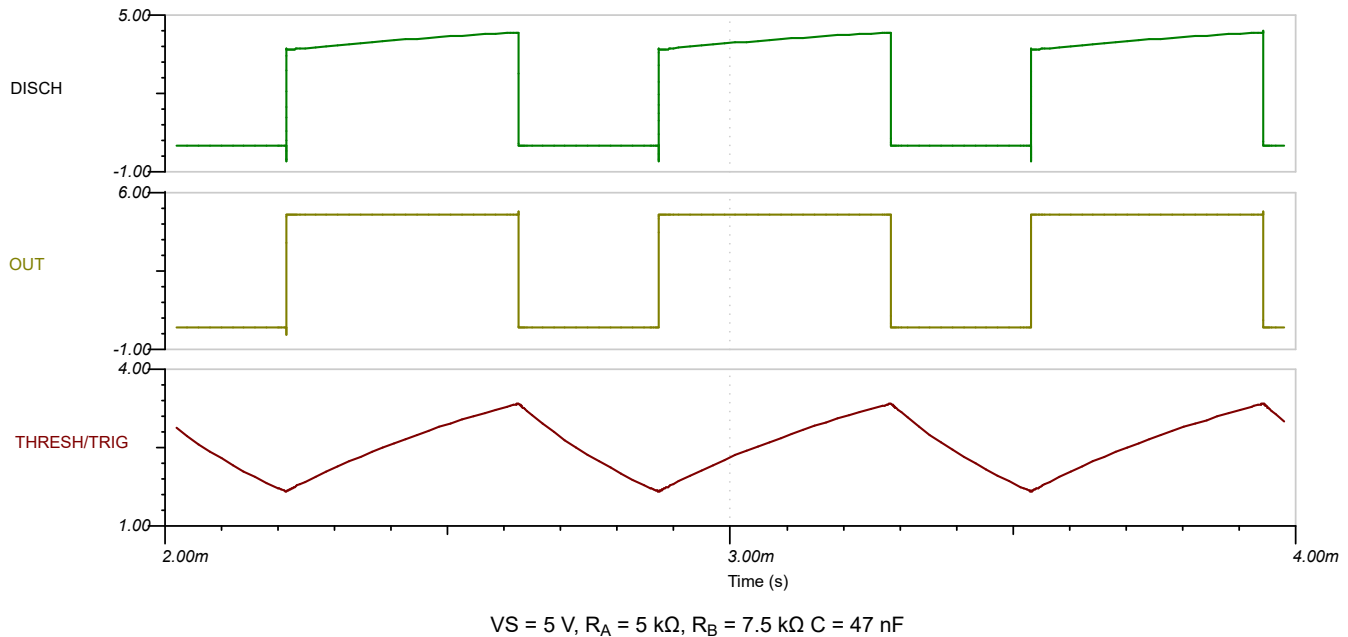


Figure 3-4. TINA-TI Simulation Results for a Variable Duty Cycle Oscillator Configuration Using a 555 Timer

Alternatively, the designer can use a smart DAC such as the DAC53701 to create an output pulse train with variable frequency and variable duty cycle. The CWG mode of the DAC53701 has the ability to output triangle waves, sawtooth waves with rising or falling slopes, and square waves. Configuration registers are available to customize the slew rate and the high and low voltage levels of the output. This circuit is shown in Figure 3-5.

The function generator can create a 50% duty-cycle square wave with a limited number of adjustable frequencies. The frequency is given in Equation 10:

$$f = \frac{1}{2 \times SLEW_RATE} \quad (10)$$

Where: SLEW_RATE is the time per high and low pulse of the square waveform.

A 50% duty cycle output pulse train with a greater number of frequencies, or a pulse train with duty cycles other than 50% can be created by using the [DAC53701](#) in CWG mode and applying a fixed input voltage on the feedback pin (VFB) of the DAC. The [DAC53701](#) can create a triangle wave with a frequency given by:

$$f = \frac{1}{2 \times \text{SLEW_RATE} \times \left(\frac{\text{MARGIN_HIGH} - \text{MARGIN_LOW} + 1}{\text{CODE_STEP}} \right)} \quad (11)$$

Where:

SLEW_RATE is given in time per step.

MARGIN_HIGH and MARGIN_LOW are the programmable DAC codes.

CODE_STEP is the programmable number of DAC codes per step.

The margin-high voltage is the high-voltage level of the waveform, and the margin-low voltage is the low-voltage level. The pulse train frequency will be equal to the frequency of the triangle wave generated by the DAC.

The duty cycle of the pulse train output correlates with the margin-high voltage, margin-low voltage and voltage applied to the feedback pin (VFB), as expressed by:

$$\text{Duty Cycle} = \frac{\text{MARGIN_HIGH_VOLTAGE} - \text{VFB}}{\text{MARGIN_HIGH_VOLTAGE} - \text{MARGIN_LOW_VOLTAGE}} \quad (12)$$

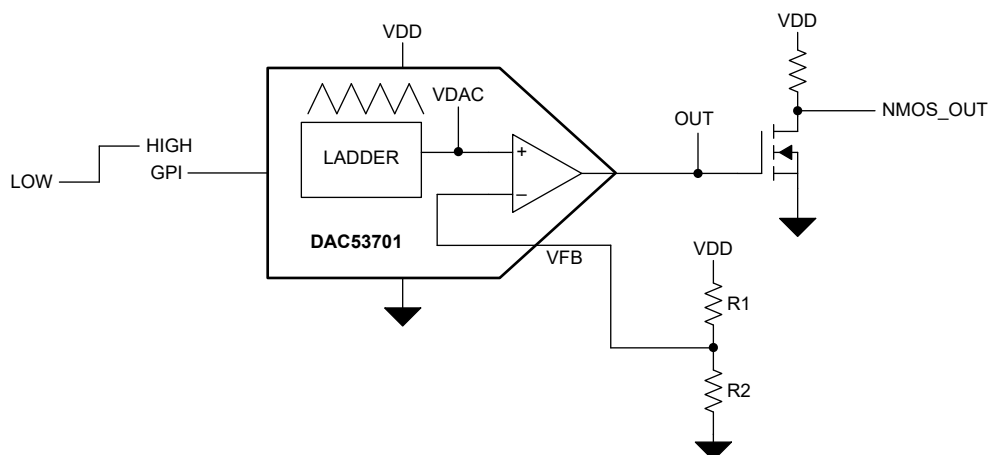
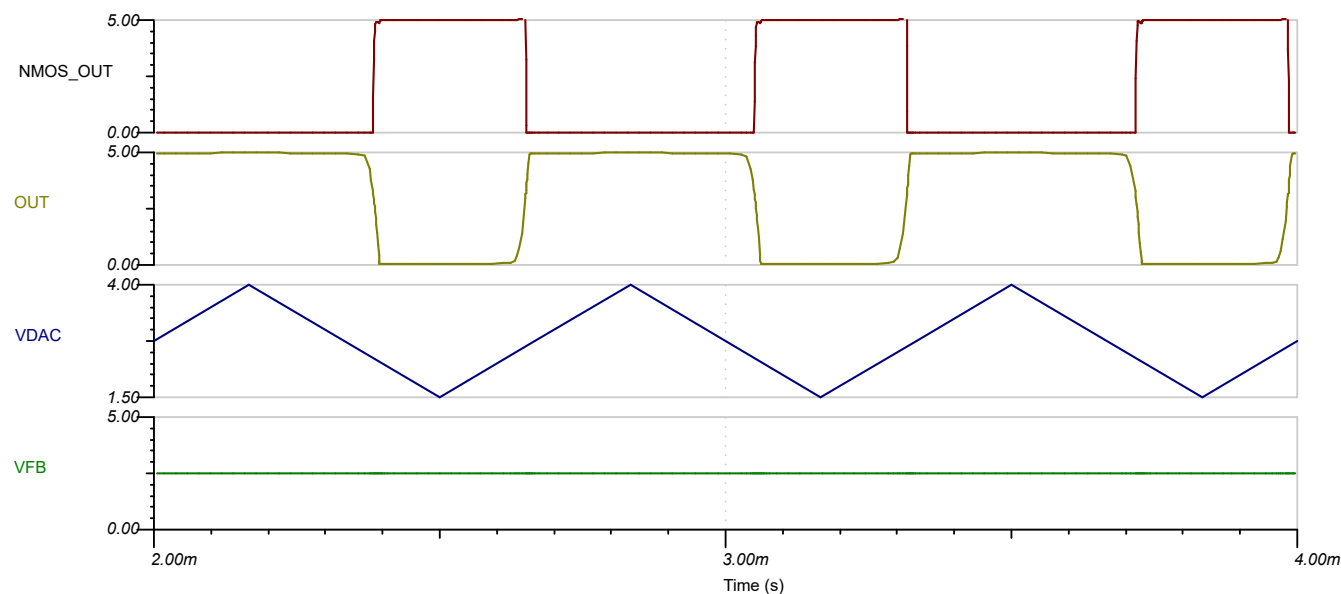


Figure 3-5. DAC53701 Configured for a Variable Duty Cycle Oscillator

Figure 3-6 shows the resulting waveforms for a 1.5-kHz output with a 60% duty cycle. An NMOS transistor may be added to the output of the [DAC53701](#) to sharpen the edges of the output, but note this will inverse the duty cycle as shown in the simulation.



VS = 5 V, MARGIN_HIGH_CODE = 810, MARGIN_LOW_CODE = 310, CODE_STEP = 32, SLEW_RATE = 4 μ s/step,
MARGIN_HIGH = 4 V, MARGIN_LOW = 1.5 V, VDAC = 1.5-kHz triangle wave, and VFB = 2.5 V

Figure 3-6. TINA-TI Simulation Results for a Variable Duty Cycle Oscillator Using a DAC53701

The 555 timer relies on an external capacitor as its core timing element and these components often have large tolerances on the order of 20%, leading to large variation in the output frequency. The smart DAC presents a superior option due to the internal oscillator having an accuracy of 5%.

4 Analog Input to PWM Output

The designer can use the 555 timer in monostable operation to generate a PWM signal by applying a trigger input with the desired frequency on the TRIG pin and an analog-input modulation voltage on the CONT pin. [Figure 4-1](#) shows a configuration in which a negative transition on the TRIG pin goes below the trigger threshold of $\frac{1}{3} \times V_{DD}$, causing the flip-flop output ($\overline{Q}$) to transition low, which drives OUT high and turns off the discharge path. With the discharge path turned off, C is charged through R_A , and continues until the voltage of the capacitor on the THRESH pin exceeds that of the analog input applied to the CONT pin. When the input waveform on the TRIG pin has returned to a high level, the flip-flop is reset, $\overline{Q}$ transitions high, the output is driven low, and the capacitor discharges through the discharge path. The negative pulse on TRIG must be shorter than the shortest expected output pulse determined by RC and the voltage on the CONT pin, otherwise the device will retrigger and the output voltage will remain high.

The RC time constant of $R_A \times C$ should be selected to equal approximately $\frac{1}{4}$ of the period of the pulse train input to the TRIG pin. $4 \times R_A \times C$ is the estimated time to transition from 0 V to VDD, therefore selecting components with this relationship will allow for a full charge within one pulse train period input to the TRIG pin.

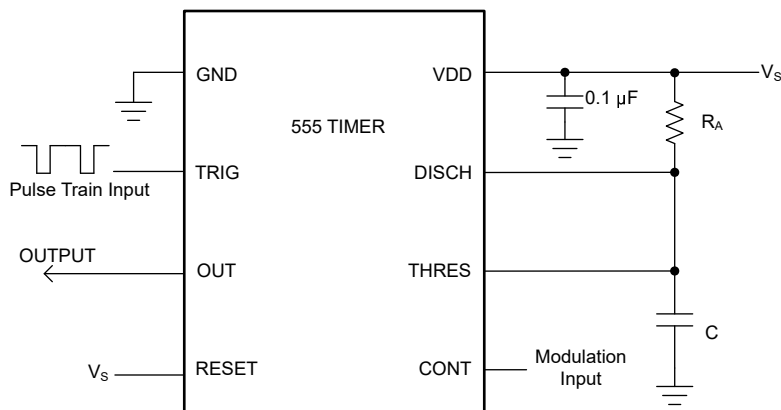
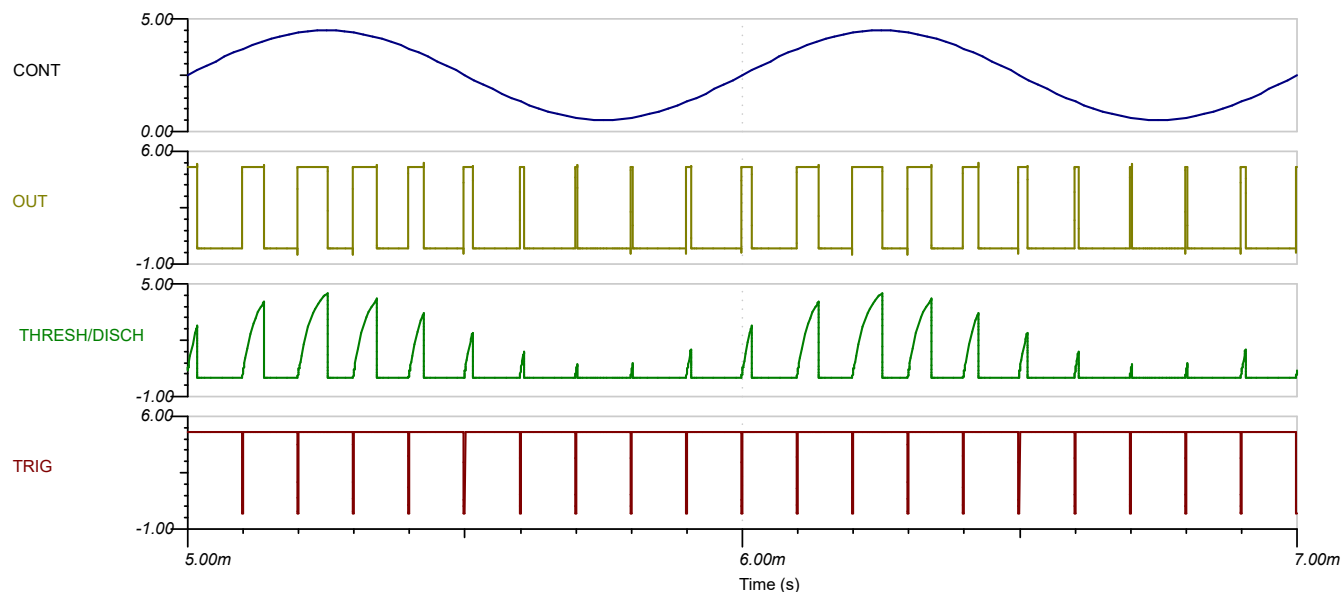


Figure 4-1. 555 Timer Configured for PWM

This combination of behaviors achieves a PWM function. The main limitation from this circuit is that a traditional PWM scheme relies on a linear function to modulate the analog input signal. In this case, the PWM transfer function is based on the exponential voltage response of the capacitor charging — this aligns with a linear function for lower voltages applied to the CONT pin, but begins to deviate from the linear function for higher voltages.

Figure 4-2 shows the resulting waveforms for PWM applied to a 1-kHz input sine wave with a trigger frequency of 100-kHz.



VS = 5 V, $R_A = 12 \text{ k}\Omega$, $C = 2 \text{ nF}$, TRIG = 100-kHz square wave with 98% duty cycle, and CONT = 4-Vpp 1-kHz sine wave with a 2.5-V DC offset

Figure 4-2. TINA-TI Simulation Results for Analog Input to PWM Output Using a 555 Timer

Smart DACs are superior for creating PWM signals. A PWM output is generated by using the DAC53701 in CWG mode and applying a modulation input voltage, VFB, to the feedback pin of the DAC as shown in Figure 4-3. The equations for frequency and duty cycle will be the same as Equation 11 and Equation 12. The duty cycle will have a linear relationship with the modulation input.

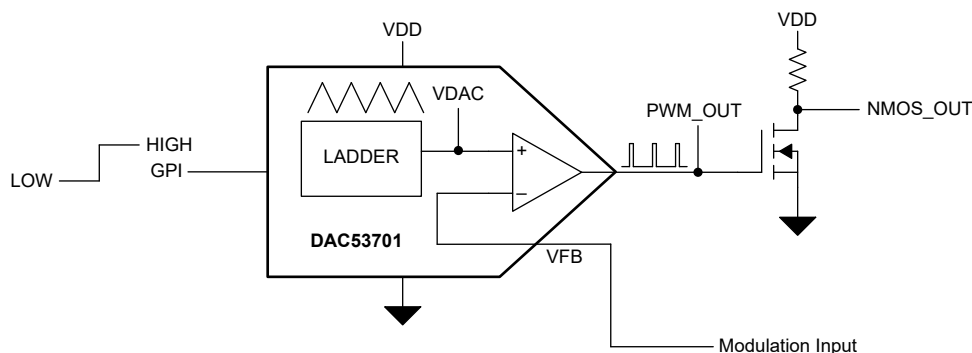


Figure 4-3. DAC53701 Configured for PWM

Figure 4-4 shows a 10-kHz triangle wave produced by the DAC53701 and a 1-kHz, 700 mV peak input sine wave centered at 3 V applied to the modulation input. To achieve a faster PWM signal, the slew rate can be lowered, the code step can be increased, or the number of codes between margin-high and margin-low can be minimized. The modulation input must also be scaled accordingly to not exceed the margin-high and margin-low voltages.

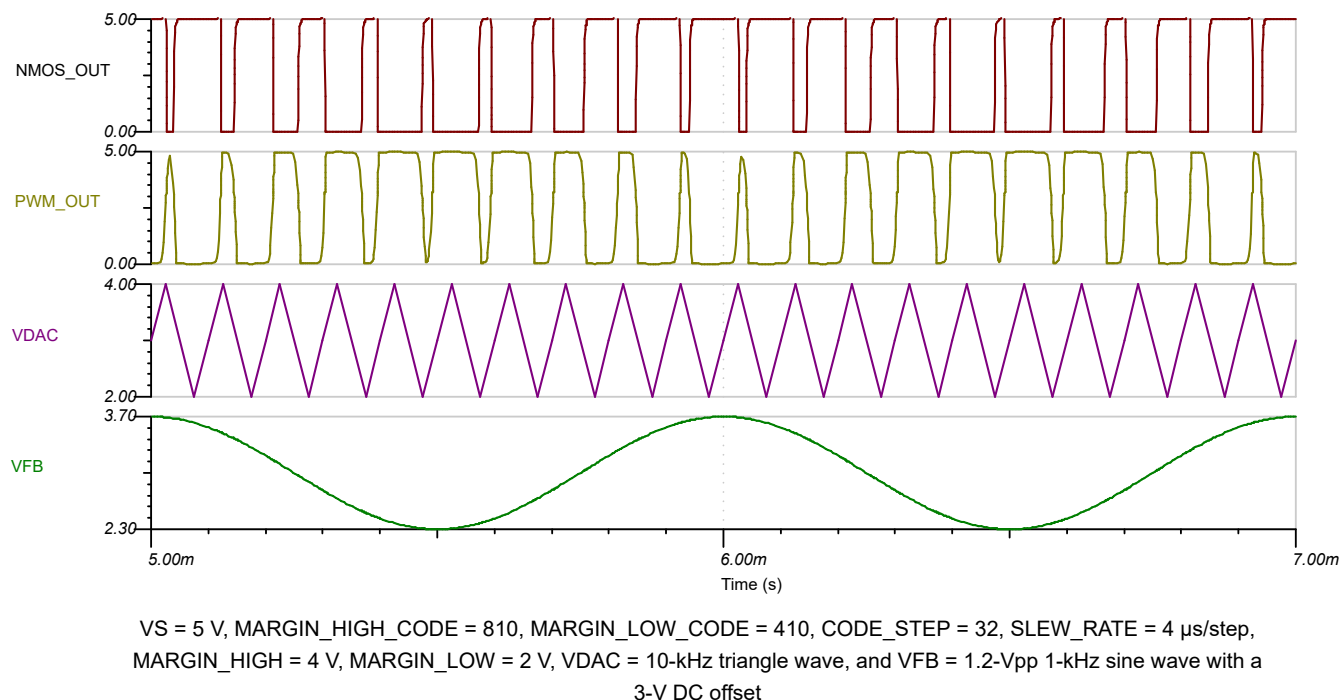


Figure 4-4. TINA-TI Simulation Results for Analog Input to PWM Output Using a DAC53701

5 General Purpose Input (GPI) to PWM Output

Using a principle of operation similar to the analog input to PWM output circuit, it is possible for the system designer to create fixed PWM outputs based on a combination of GPIs. The CONT input to the 555 timer has an internal resistor divider with a nominal pull-up value of 100 k Ω and a pull-down value of 200 k Ω . Figure 5-1 shows a circuit where GPI1 and GPI2 can be driven to states of 0 V or VDD to adjust the voltage at the CONT pin based on the collective impedance of the internal voltage divider circuit.

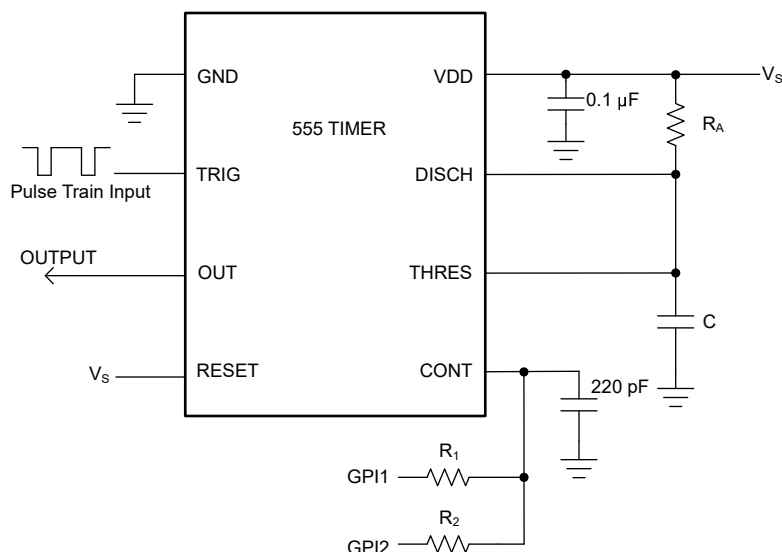
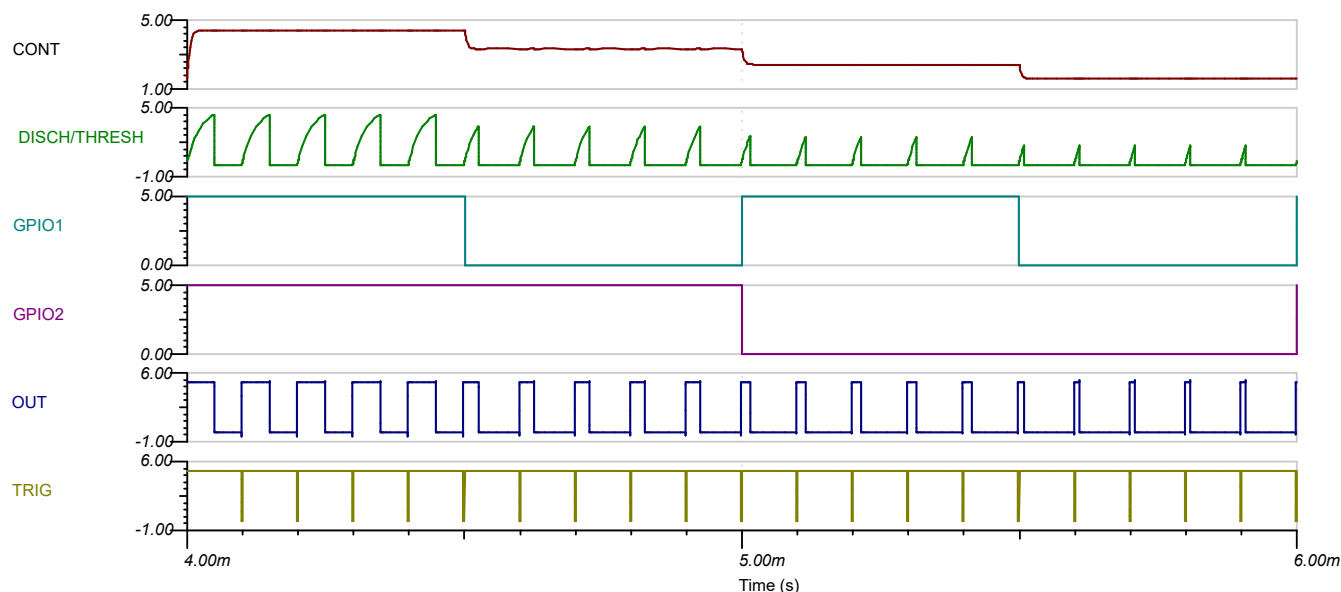


Figure 5-1. 555 Timer Configured for General Purpose Input to PWM

The TINA-TI simulation results shown in Figure 5-2 use $R_1 = 100$ k Ω and $R_2 = 50$ k Ω to create four fixed CONT input voltage levels of 4.39 V, 3.33 V, 2.42 V, and 1.6 V based on the four states of GPI1 and GPI2. A decoupling capacitor is connected to the CONT pin to reduce glitches on the pin during transitions. The circuit then converts these fixed voltages at the CONT pin to PWM outputs using the same principle of operation as the analog input to PWM output circuit.



VS = 5 V, $R_A = 12$ k Ω , $C = 2$ nF, TRIG = 100-kHz square wave with 98% duty cycle, $R_1 = 100$ k Ω , $R_2 = 50$ k Ω

Figure 5-2. TINA-TI Simulation Results for GPI to PWM Output Using a 555 Timer

GPIs can also be added to a smart DAC to create multiple fixed duty cycle PWM outputs. Adding two resistors to the [DAC53701](#) feedback network shown in [Figure 5-3](#) creates two new GPI pins. The voltage at the feedback pin changes depending on the level of GPI1 and GPI2. The four resistors in the feedback network can be modified to get custom threshold levels at the [DAC53701](#) feedback pin. The voltage at the feedback pin, along with the margin-high and margin-low voltages of the triangular or sawtooth waveform being generated by the CWG, determine the duty cycle of the PWM output. The slew rate, code step, margin-high and margin-low codes determine the frequency.

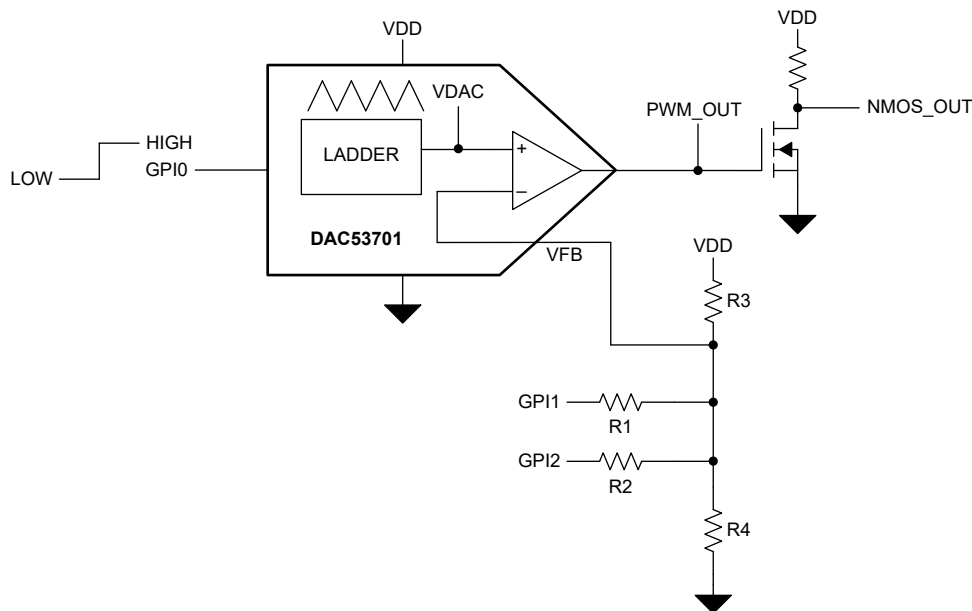
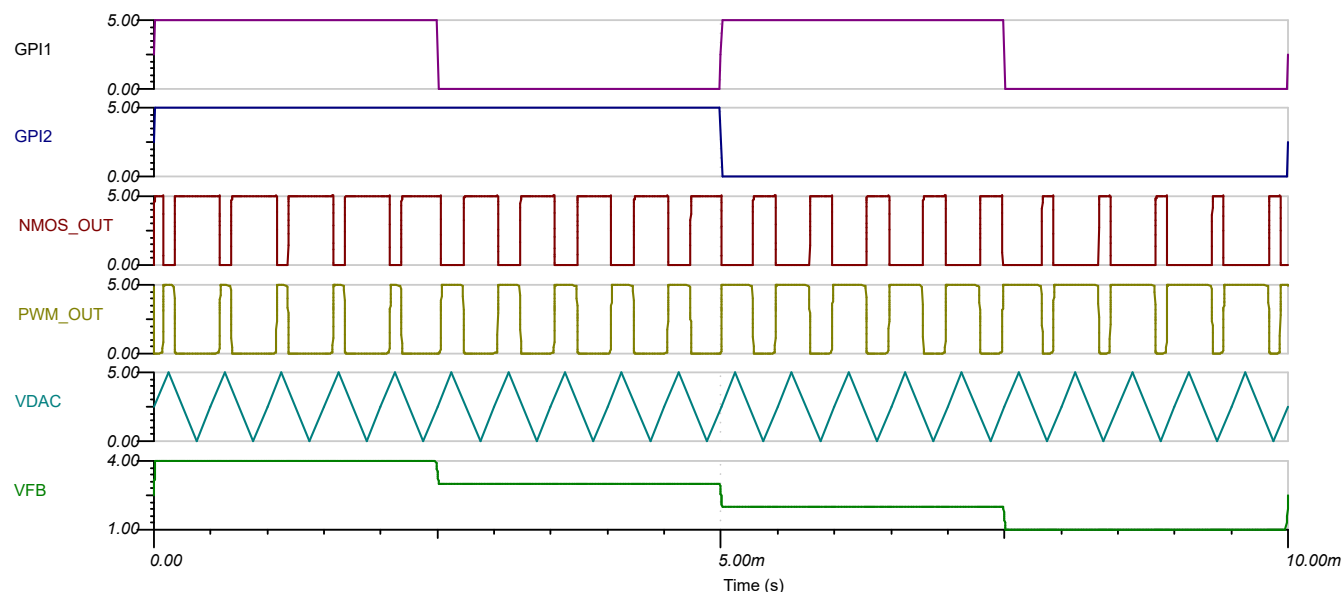


Figure 5-3. DAC53701 Configured for General Purpose Input to PWM

Figure 5-4 shows the simulation results with R_{1-4} creating 4 voltage steps at 4 V, 3 V, 2 V, and 1 V that produce corresponding PWM duty cycles of 20%, 40%, 60%, and 80% respectively on the DAC53701 output.



VS = 5 V, MARGIN_HIGH_CODE = 1023, MARGIN_LOW_CODE = 0, CODE_STEP = 16, SLEW_RATE = 4 μ s/step, MARGIN_HIGH = 5 V, MARGIN_LOW = 0 V, VDAC = 2-kHz triangle wave, $R_1 = 5 \text{ k}\Omega$, $R_2 = 2.5 \text{ k}\Omega$, $R_3 = 5 \text{ k}\Omega$, $R_4 = 5 \text{ k}\Omega$

Figure 5-4. TINA-TI Simulation Results for GPI to PWM Output Using a DAC53701

In both the analog input to PWM and GPI to PWM applications, the voltage to duty-cycle function is non-linear in 555 timers and creates duty-cycle error on the order of 5%. The DAC53701 smart DAC voltage presents a superior solution by having linear duty-cycle function with a less than 1% duty-cycle error.

6 Comparator with Hysteresis

The designer can use the 555 timer without an external timing element to create a comparator with input hysteresis. In the configuration shown in Figure 6-1, the internal resistor divider presents thresholds of $\frac{2}{3} \times V_{DD}$ for the high comparator and $\frac{1}{3} \times V_{DD}$ for the low comparator. When an input voltage is applied to the connected TRIG and THRESH pins, the circuit functions as a comparator with input hysteresis. The high threshold for a positive-transitioning input signal is $\frac{2}{3} \times V_{DD}$ and the low threshold for a negative-transitioning input signal is $\frac{1}{3} \times V_{DD}$. Upon transitioning beyond either threshold, the internal flip-flop latches the output state and will not clear unless the input signal transitions beyond the other threshold or if RESET is toggled. Due to the fixed configuration of the 555 timer, the comparator circuit functions with inverse polarity as seen in the simulation in Figure 6-2.

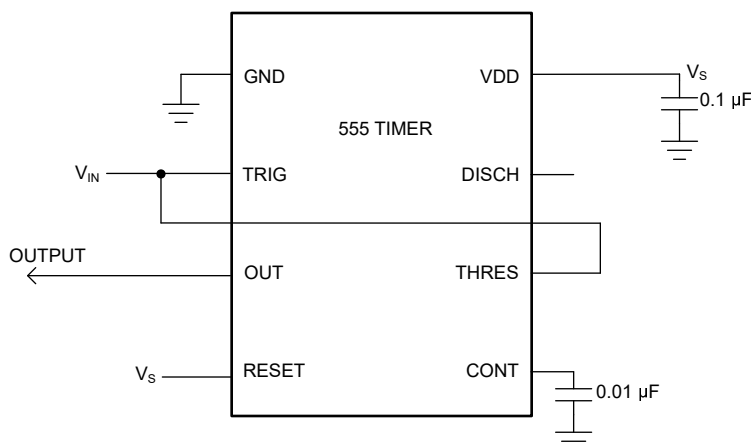


Figure 6-1. 555 Timer Configured for a Comparator with Hysteresis

The main limitation of this circuit is that the designer cannot independently adjust the high and low threshold levels, as they are fixed by the internal resistor divider. Note that there is some flexibility to be had with the use of the CONT pin, as any impedance on this node will adjust the high and low thresholds and can be calculated using simple resistor divider math. Connecting a resistor from the CONT pin to ground will lower both the high and low thresholds, whereas connecting a resistor from the CONT pin to VDD will increase both the high and low thresholds. The designer can also apply a voltage directly to the CONT pin to adjust the threshold voltages. In all cases, it is not possible to independently adjust one threshold without impacting the other.

The TINA-TI simulation results presented in [Figure 6-2](#) displays the output for a 1-kHz input sine wave with an amplitude of 4.5 Vpp and a DC offset of 2.5 V.

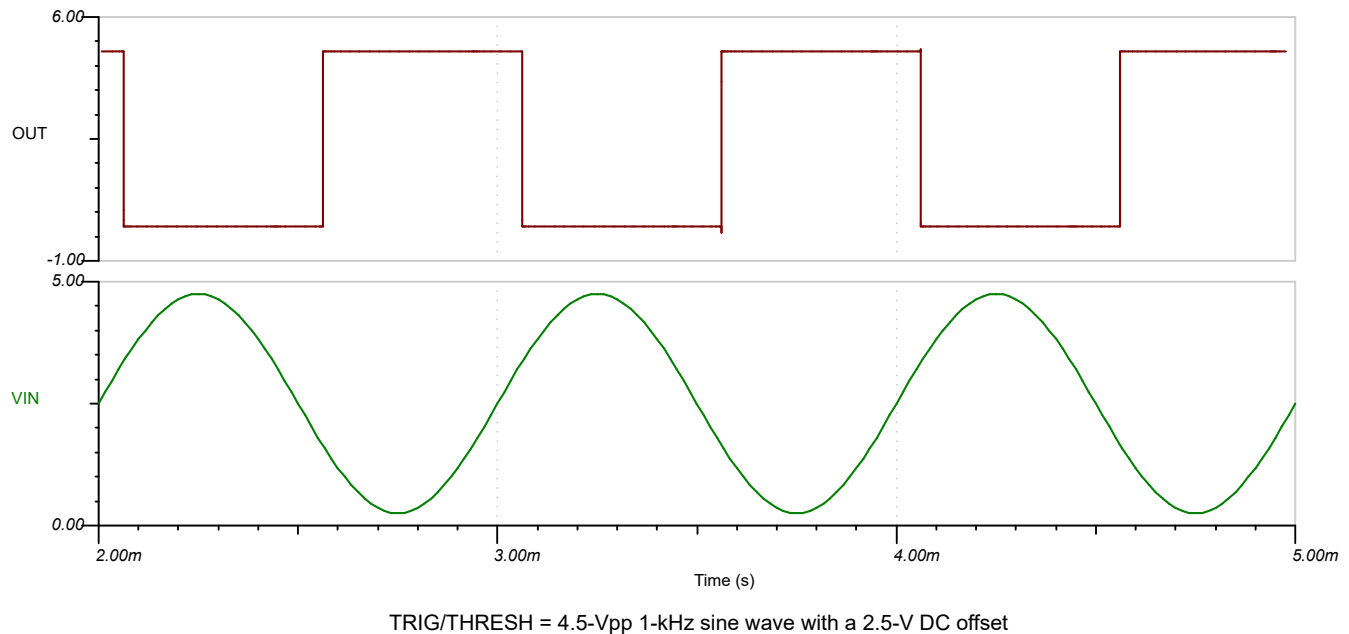


Figure 6-2. TINA-TI Simulation Results for a Comparator with Hysteresis Using a 555 Timer

Smart DACs can be configured to act as a comparator with hysteresis with two independent threshold voltages. The input voltage applied to the [DAC53701](#) feedback pin is compared against the threshold voltage set in the DAC. The GPI pin on the [DAC53701](#) can be programmed to switch between two threshold voltages. If the output of the DAC is connected to the GPI pin, the DAC will switch threshold voltages when the output changes due to the voltage on VFB, creating the hysteresis. These two threshold voltages are programmed into the margin-high and margin-low registers, and the GPI is enabled for margin-high, margin-low function. An RC filter can be added to the GPI feedback as seen in [Figure 6-3](#) to provide a small delay to avoid any instability on the GPI pin due to noise.

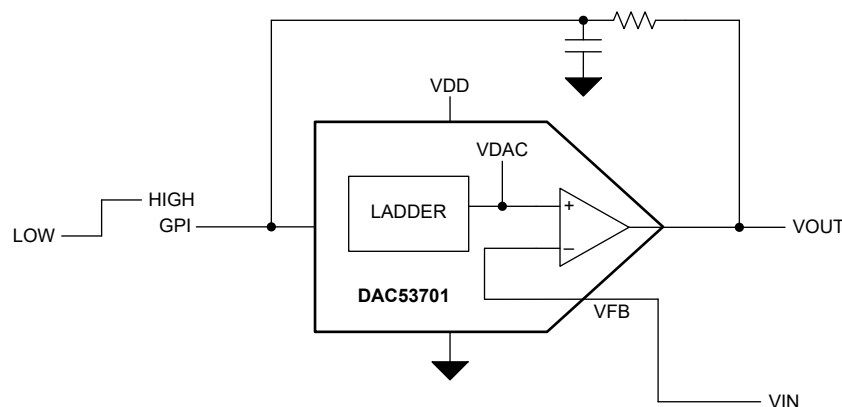


Figure 6-3. Smart DAC Configured for a Comparator with Hysteresis

Figure 6-4 shows a simulation of the DAC53701 output responding to the sine wave applied to the feedback pin and the 3-V and 1-V threshold values.

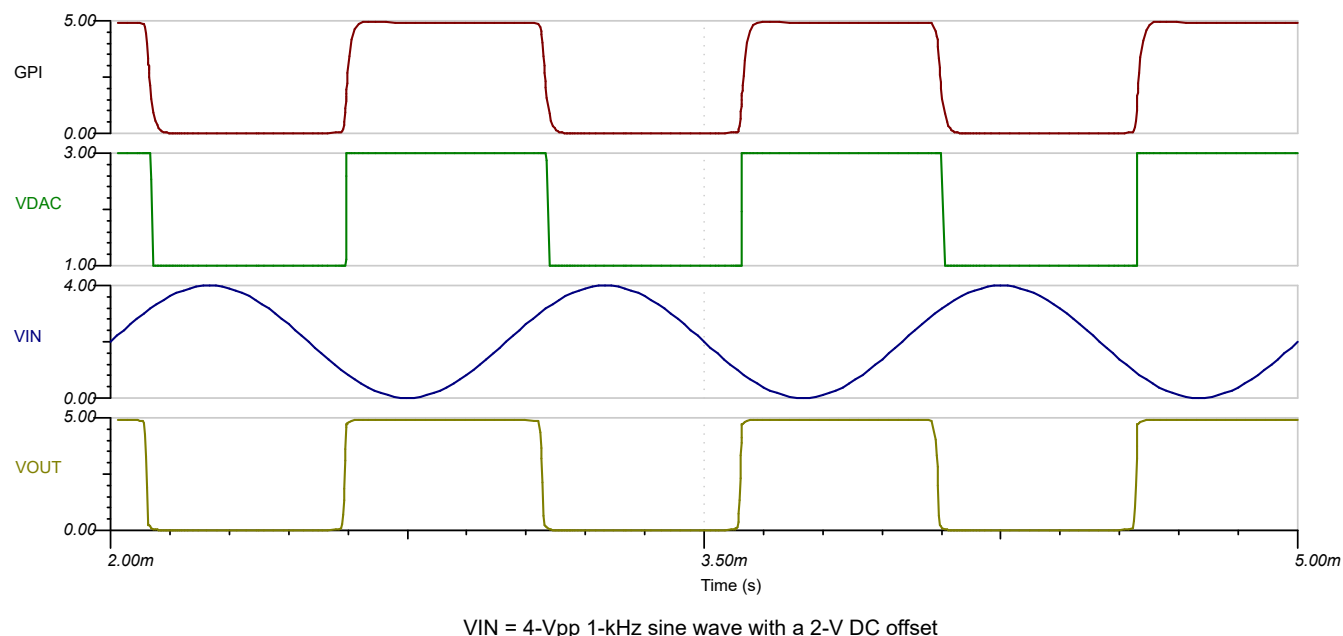


Figure 6-4. TINA-TI Simulation Results for a Comparator with Hysteresis Using a DAC53701

The smart DAC presents a superior solution when used as a comparator with hysteresis by offering independently configurable thresholds, whereas the 555 timer is limited in threshold configurability by its fixed internal resistor dividers.

7 Trade-offs and Conclusions

Using four common application circuits, it has been shown that smart DACs can provide superior performance when compared to 555 timers. There are still be use cases in which a 555 timer is the preferred device if the application calls for high voltage and/or high output current. TI has 555 timers with minimum supplies of 1.5 V ([LMC555](#)) or maximum supplies of 18 V ([SE555](#)) while smart DACs have a supply voltage range of 1.8 V to 5.5 V across the same temperature range. 555 timers can output as much as 200 mA of current, while smart DACs can output 10 mA.

For cost-effective solutions that do not require high accuracy, the 555 timer is still a useful building block, specifically if working with high voltage and or high output current applications. However, many modern use cases are for lower voltage supplies with lower output current requirements, and the smart DAC offers considerable benefits in these cases. Smart DACs can provide competitive pricing against 555 times, so for these applications contact factory for a quote.

Waveform creation with 555 timers relies on a collection of external components which — specifically in the case of external capacitors — can have wide tolerance variation. Smart DACs remove the need to rely on the variation of external capacitors for timing elements and can achieve much higher accuracy. Most errors can be calibrated out in production by reprogramming the device to achieve the desired output. In PWM applications, the [DAC53701](#) smart DAC voltage to duty-cycle is a linear function with a less than 1% duty-cycle error while it is non-linear in the 555 timer with about a 5% duty-cycle error. The waveform timings are programmable in smart DACs using I²C or SPI and they can be recalled directly from EEPROM without a processor whereas 555 timers need a hardware update for every change.

For low voltage, low output current use cases, the combination of a smart DAC's programmability, high accuracy with limited external components, and stored EEPROM configurations make it a superior choice to the 555 timer.

Table 7-1. Smart DAC vs. 555 Timer Comparison Table

	Smart DAC (DAC53701)	555 Timer (LMC555)	555 Timer (SE555)
Accuracy	<1% total unadjusted error (TUE) over temperature.	17% initial device accuracy plus timing capacitor and resistor tolerance at room temperature.	1.5% initial device accuracy plus timing capacitor and resistor tolerance at room temperature.
Solution size	2.00mm × 2.00 mm package.	1.43mm × 1.41 mm package plus external timing capacitor and resistors.	4.90mm × 3.91 mm package plus external timing capacitor and resistors.
Configurability	EEPROM to store timing settings. Reconfigurable using I ² C or SPI communication.	Timing settings defined by hardware. A hardware change is required to reconfigure the timing.	Timing settings defined by hardware. A hardware change is required to reconfigure the timing.
Max Frequency (square wave mode)	250kHz	3MHz	100kHz
Max Frequency (PWM mode)	2.5kHz (1% to 99% duty cycle)	16.7 kHz (12% to 98% duty cycle). Duty cycle range improves at lower frequencies.	16.7 kHz (25% to 95% duty cycle). Duty cycle range improves at lower frequencies.
Voltage to duty cycle function type	Linear	Non-linear	Non-linear
Operating power supply	1.8 V to 5.5 V	1.5 V to 15 V	4.5 V to 18 V
Operating temperature	-40°C to 125°C	-40°C to 125°C	-40°C to 125°C
Static Current (output high, no load)	225µA	100µA	2mA
Current Output	10mA source and sink	50mA source, 10 mA sink	200mA source and sink

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