EVM User's Guide: AMP-PDK-EVM

Amplifier Performance Development Kit Evaluation Module

Description

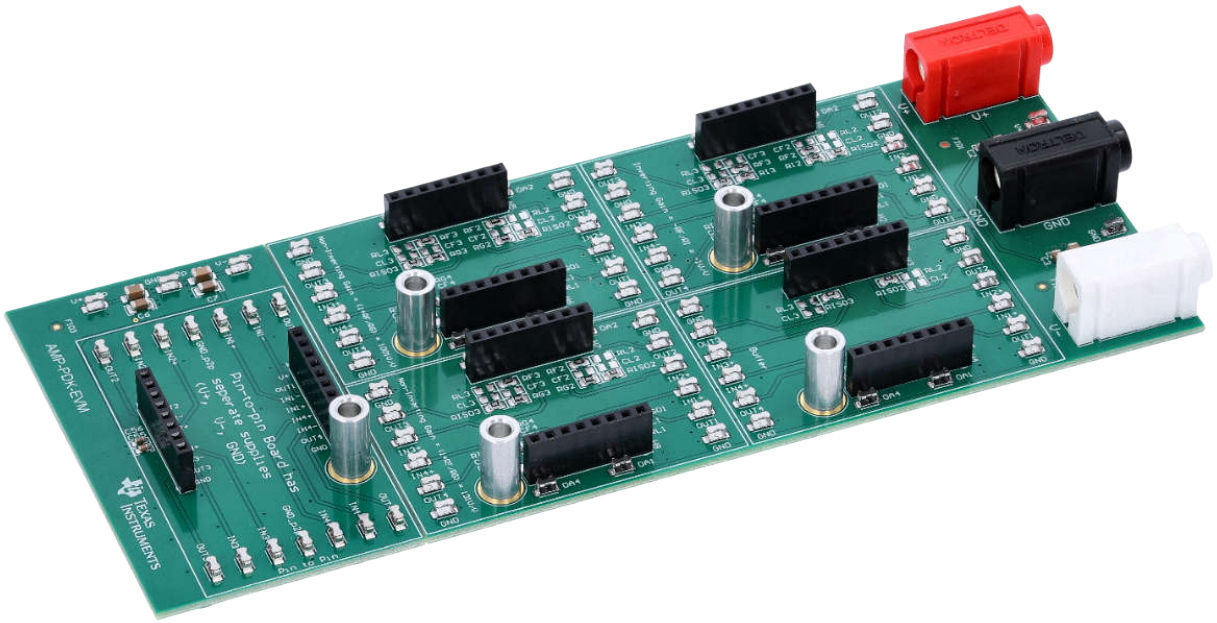
The Amplifier Performance Development Kit (AMP-PDK-EVM) is an evaluation module (EVM) kit to test common operational amplifier (op amp) parameters and is compatible with most op amps and comparators. The EVM kit offers a main board with several socketed daughtercard options to fit package needs, allowing engineers to quickly evaluate and verify device performance.

Get Started

1. Order the main board: AMP-PDK-EVM.
2. Order socketed daughtercard.
3. Order devices to be evaluated from ti.com.
4. For step-by-step instructions, download the user's guide.
5. Reference training videos on ti.com for common amplifier parameter tests.

Features

- Solderless platform to quickly evaluate most op amps and comparators
- Four preconfigured op amp circuits of inverting and non-inverting gains
- Optional breakaway pin-to-pin circuit to test both op amps and comparators
- Schematics of preconfigured circuits are provided on the silkscreen of the AMP-PDK-EVM



AMP-PDK-EVM

1 Evaluation Module Overview

1.1 Introduction

This user's guide contains support documentation for the AMP-PDK-EVM. This EVM kit is compatible with most op amps and comparators in various packages. The EVM is designed for quick evaluation of common op amp parameters and to verify device performance.

This document includes descriptions of how to use the EVM kit, contents, schematics, printed circuit board (PCB) layouts, and bill of materials (BOM).

Throughout this document the terms *evaluation board*, *evaluation module*, *development kit, main board, motherboard,* and *EVM* are synonymous with the AMP-PDK-EVM. The terms *daughtercard, socket board, socketed daughtercard, socketed adapter board,* and *package variants* are synonymous with the options listed in Table 1-1.

1.2 Kit Contents

The orderable AMP-PDK-EVM contains only the main board. The daughtercard options for the different package variants are not included. Ordering the AMP-PDK-EVM main board with at least one daughtercard (Table 1-1) for full functionality is required. Devices must be ordered separately.

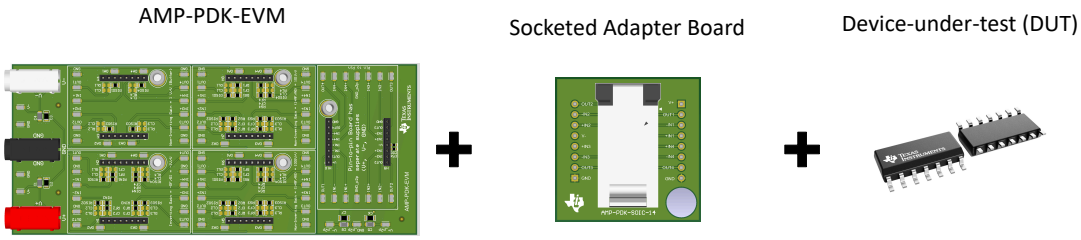


Figure 1-1. Components Required for Device Evaluation

The available daughtercards with the package descriptions are listed in Table 1-1, showing each corresponding orderable part number, package family, TI package designator, number of channels, and pin count.

The shutdown and non-shutdown variants of a device are supported (as seen by the pin-count). An example is using the AMP-PDK-SC70-6 with the TLV9001 available in non-shutdown TLV9001I**DCK**R (SOT-SC70 (DCK) | 5) and in shutdown TLV9001SI**DCK**R (SOT-SC70 (DCK) | 6).

A device's package designators and pin count can be found on ti.com.

Table 1-1. AMP-PDK-EVM Daughtercard Options

Orderable Part Number	Package Family	TI Package Designator	No. Of Channels in Device	Pin Count (Non-Shutdown | Shutdown Variant)
AMP-PDK-SC70-6	SOT-SC70	DCK	1	5 | 6
AMP-PDK-SOT23-6	SOT-23	DBV	1	5 | 6
AMP-PDK-VSSOP-8	VSSOP	DGK	2	8
AMP-PDK-SOIC-8	SOIC	D	2	8
AMP-PDK-SOIC-14	SOIC	D	4	14
AMP-PDK-TSSOP-14	TSSOP	PW	4	14

1.3 Specification

The AMP-PDK-EVM is capable of testing op amp or comparators available in the provided package options. The EVM can be used to verify common data sheet parameters and to troubleshoot some application circuits (capacitive load drive).

1.4 Device Information

The AMP-PDK-EVM main board contains four preconfigured common amplifier circuits and one pin-to-pin board that can be leveraged by both op amps and comparators. For ease of use, metal alignments have been installed to verify correct daughtercard orientation. If necessary, the prepopulated circuits can be modified to evaluate different gains, loads, and circuit stability compensation options.

2 Hardware

2.1 Additional Images

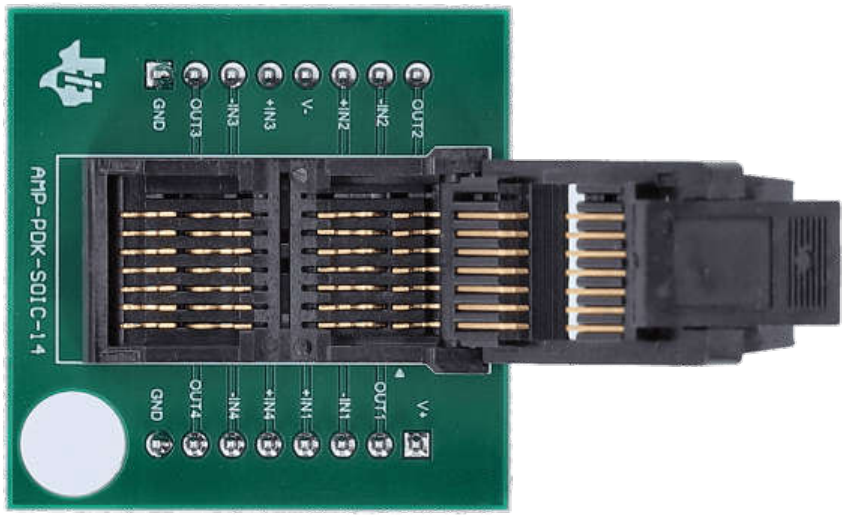


Figure 2-1. AMP-PDK-SOIC-14

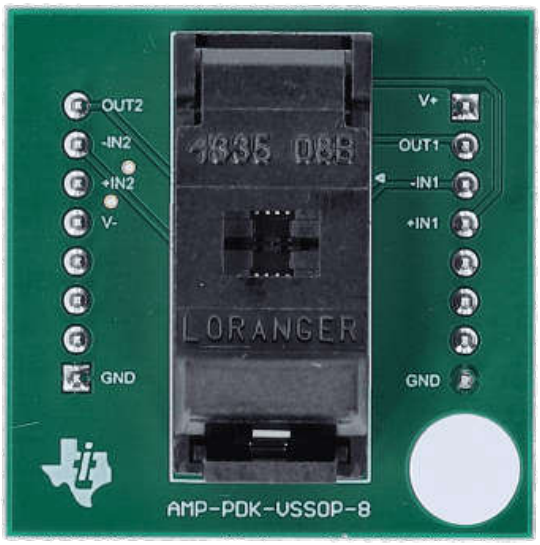


Figure 2-2. AMP-PDK-VSSOP-8

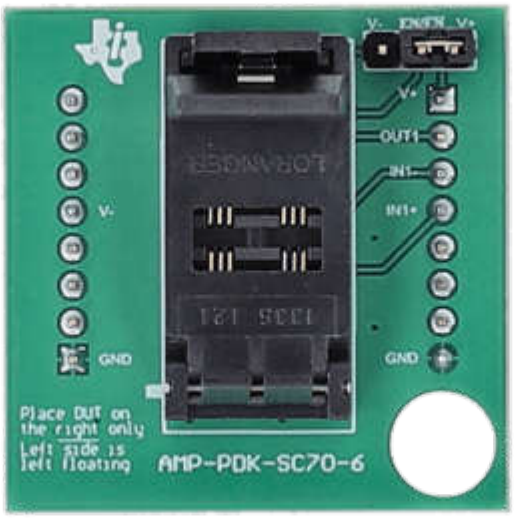


Figure 2-3. AMP-PDK-SC70-6

Figure 2-4. AMP-PDK-SOIC-8

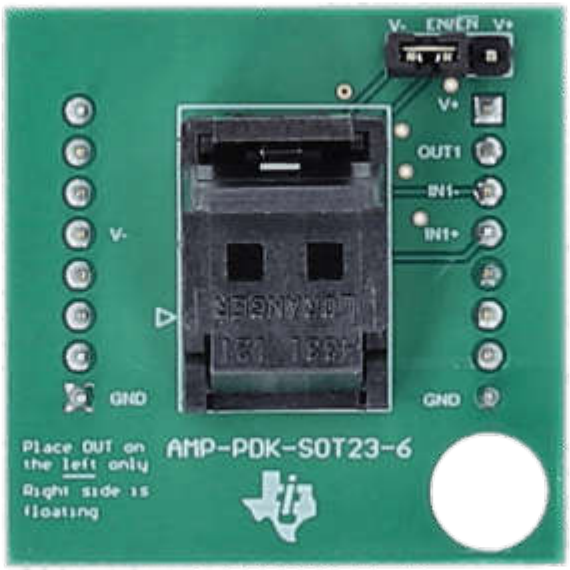


Figure 2-5. AMP-PDK-SOT23-6

Figure 2-6. AMP-PDK-TSSOP-14

2.2 How to Setup

The AMP-PDK-EVM comes with four preconfigured common op amp circuits and one pin-to-pin circuit that can be used to accommodate both op amps and comparators.

The pin-to-pin partition at the bottom can be separated by flexing along the scored edge (shown in Figure 2-7 as a dashed line). There are completely separate power supplies in this partition discussed in further detail in Section 2.4.

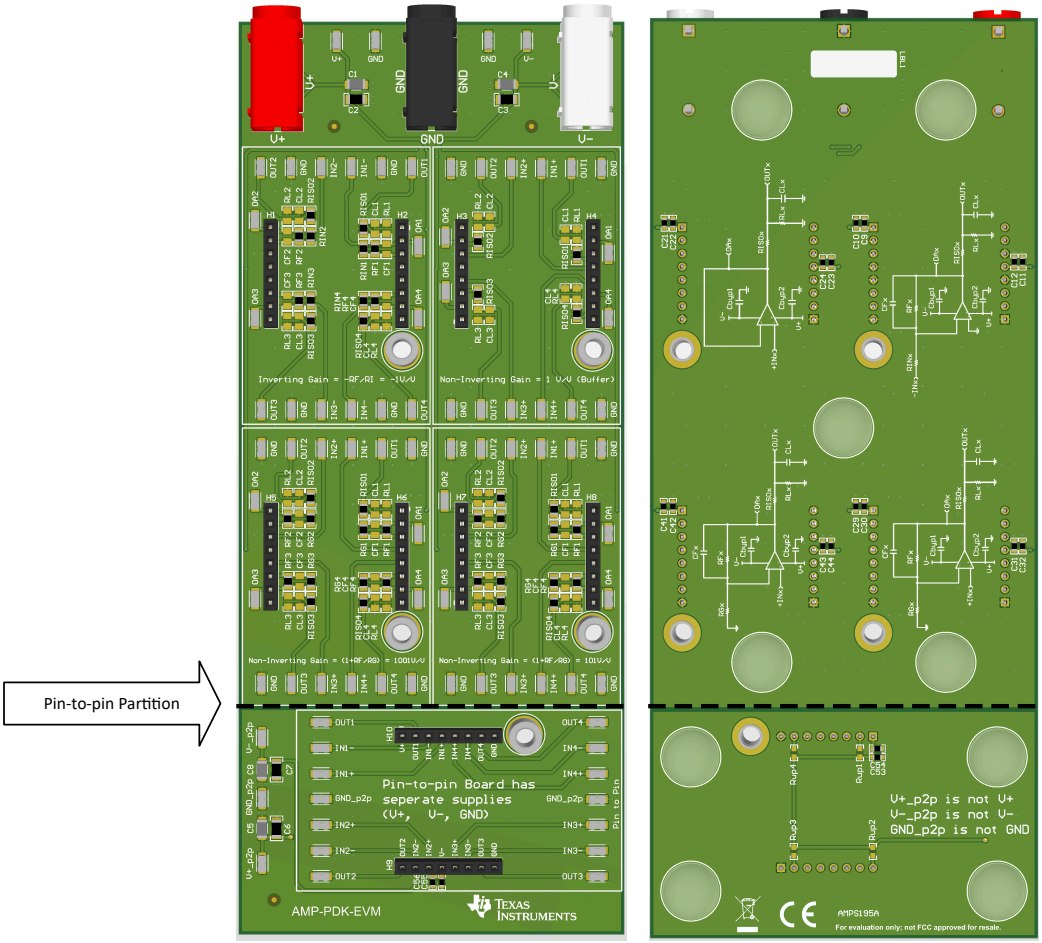


Figure 2-7. AMP-PDK-EVM Main Board - Left (Top), Right (Bottom)

2.3 Assembly Instructions

For best practice, follow the recommended assembly procedure:

1. Find which preconfigured circuit or pin-to-pin circuit is most appropriate. Common op amp parameter setups are described in detail in Section 2.5.
2. Install daughtercard onto the selected circuit on AMP-PDK-EVM by aligning both black headers and the alignment metal guide. Apply equal pressure to all four corners of the daughtercard until securely in place.
3. Using ESD safety precautions, place device into the socket with pin 1 alignment. If needed, then reference pin 1 alignment for all daughtercards in Section 2.7.
4. Connect power to the board, this is discussed in further detail in Section 2.4.
5. Connect input and output equipment to the surface mount test points, this is discussed in further detail in the Section 2.6. Common op amp parameter tests setups can be found in Section 2.5.

2.4 Power Requirements

The four preconfigured op amp test circuits are powered by *V+* (positive supply), *GND* (ground reference), and *V-* (negative supply). The triple power supply connection is required for proper biasing of the preconfigured circuits. The power connection can be accessed either through banana jack connectors or surface mount test points, both are not required.

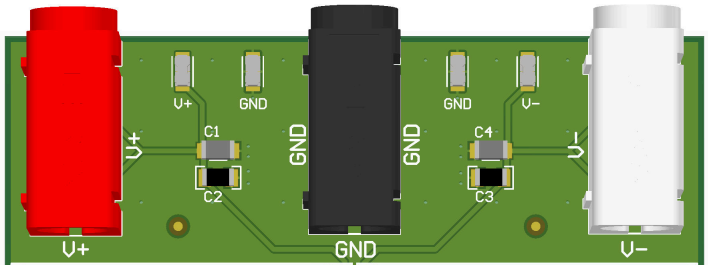


Figure 2-8. V+, V-, GND Available in Banana Jack Connectors or Surface Mount Test Points

The pin-to-pin partition has separate power supplies and ground. The pin-to-pin circuit is powered by *V+_p2p* (positive supply), *GND_p2p* (ground reference), and *V-_p2p* (negative supply). A requirement is to access the pin-to-pin power connection through the surface mount test points.

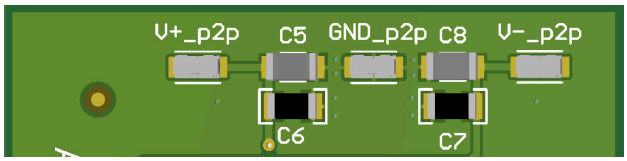


Figure 2-9. V+_p2p, V-_p2p, GND_p2p Available in Surface Mount Connectors

2.5 Setup

To test the parameters of the op amp, the test conditions must match those listed in the electrical characteristics table of the device. The following materials are required for all setup:

- AMP-PDK-EVM main board
- Package variant daughtercard
- Device-under-test (DUT)
- Triple power supply

Once the assembly instructions in Section 2.3 have been implemented, the following test setups can be referenced for common op amp parameters.

In addition to this section, step-by-step instructional videos are available on ti.com.

The equipment shown in these examples are for illustration purposes only.

Quiescent Current per Amplifier (I_Q)

I_Q is measured in series with the power supply source and the AMP-PDK-EVM.

Additional equipment needed for this test:

- Digital multimeter (DMM) or an ammeter

While referencing Section 2.3 to measure I_Q,

1. Install a daughtercard onto the *Non-Inverting Gain = 1V/V (Buffer)* preconfigured circuit.
2. Connect the positive power supply in series with a DMM:
   a. Connect *V-* and *GND* on AMP-PDK-EVM to the supplies on the triple power supply while matching the device's data sheet conditions. The current limit of the power supply must be set to at least 10 times the I_Q (considering all channels).
   b. Connect *V+* on AMP-PDK-EVM to the appropriate port on the DMM.
   c. Connect the other port from the DMM to the positive power supply on the triple power supply. Limit the output current to at least 10 times the I_Q (considering all channels).
3. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All *INx+* pins on the sub-circuit must be connected to *GND*.
4. Configure the DMM to measure DC current.
5. Turn on the power supply output.
6. On the DMM, divide the observed current by the number of channels in the op amp.

With all other data sheet conditions matched, this test setup helps verify the quiescent current in the data sheet with the one calculated. [1]

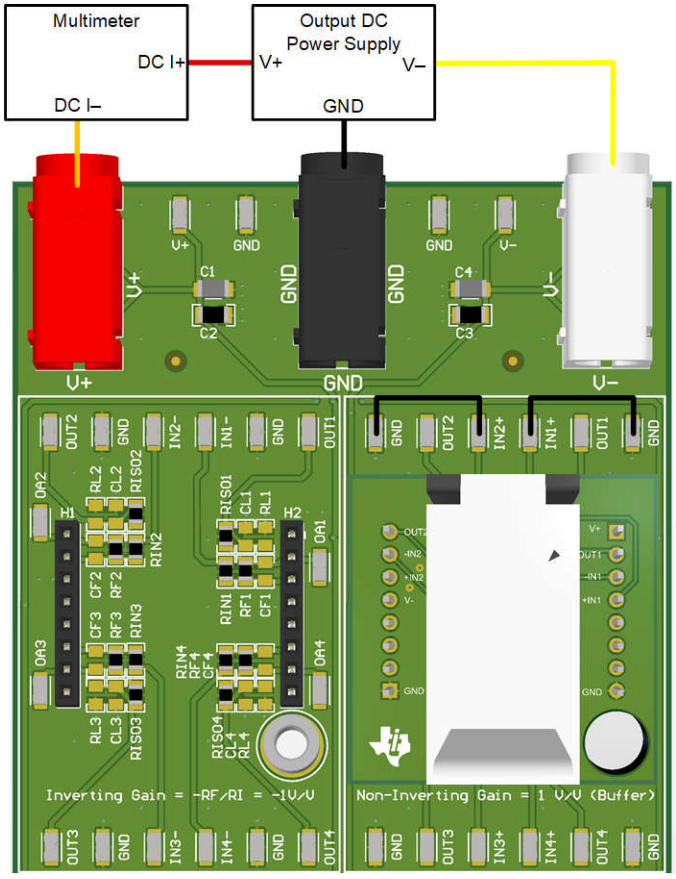


Figure 2-10. Iq Measurement Example Setup for a Dual Channel Device

[1] Some devices have *ultra-low* quiescent currents; therefore require DMM with additional digits (> 6.5 digits).

Continuity

Most op amp pins have ESD protection diodes to either power supply rail (V+ or V-). To check for the presence and operation of these diodes, follow this procedure.

Additional equipment needed for this test:

- Digital multimeter (DMM) or an ammeter

Note

This is a single supply test and therefore does not require a triple power supply.

While referencing Section 2.3 to measure continuity,

1. Install a daughtercard onto the pin-to-pin circuit.
2. Connect the power supply's positive supply to the appropriate port of the DMM. The current limit of the power supply must be set to 9mA.
3. The ground from the power supply and the other port on the DMM are the two points of continuity, due to the nature of ESD diodes, one must be referenced to a power supply *V+_p2p* or *V-_p2p*; the other is the *pin-under-test*.
4. Turn on the power supply output.
5. Manually increase the power supply output voltage in small increments, recording the current between increments, until the measured current reaches a maximum of 9mA. Do not exceed 2-3V in either direction.
6. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All *INx+* , *INx-*, and *OUTx* pins can be tested against *V+_p2p* or *V-_p2p*.

Alternatively, this test can be automated with a source meter.

This test setup helps verify the presence and operation of ESD diodes.

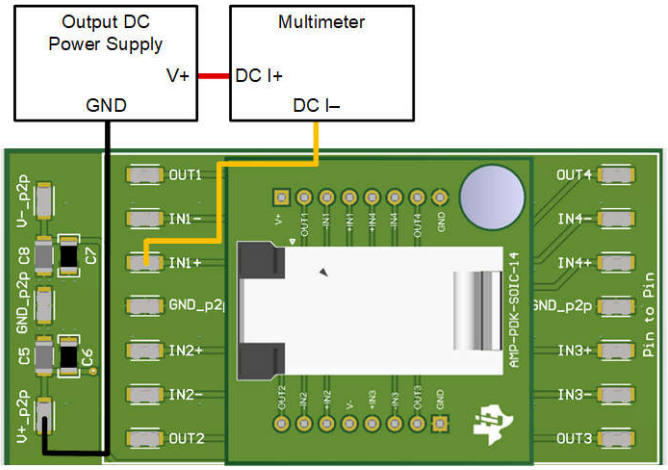


Figure 2-11. Continuity Measurement Example Setup for a Quad Channel Device

Input Offset Voltage (V_{OS})

V_{OS} is an error source at the input stage of the op amp, quantified as the differential input voltage needed to force the op amp's output to 0V.

Additional equipment needed for this test:

- Digital multimeter (DMM) or a voltmeter

While referencing Section 2.3 to measure V_{OS},

1. Install a daughtercard onto the *Non-Inverting Gain = 1001V/V* or *Non-Inverting Gain = 101V/V* preconfigured circuit depending on the typical or expected offset voltage of the device. In general, use the *Non-Inverting Gain = 1001V/V* for precision op amps and *Non-Inverting Gain = 101V/V* for general purpose op amps.
2. Connect the triple power supply to the *V+*, *GND*, and *V-* of AMP-PDK-EVM while matching the data sheet conditions of the device. The current limit of the power supply can be set to the I_{SC} + I_Q of the device (considering all channels).
3. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All *INx+* pins on the sub-circuit needs to be connected to *GND*.
4. Connect one port of the DMM to *OUTx* and the other to *GND*.
5. Configure the DMM to measure DC voltage.
6. Turn on the power supply output.
7. Multiply the voltage measurement of DMM by the gain of the preconfigured circuit.

With all other data sheet conditions matched, this test setup helps verify the input offset voltage in the data sheet with the one calculated.

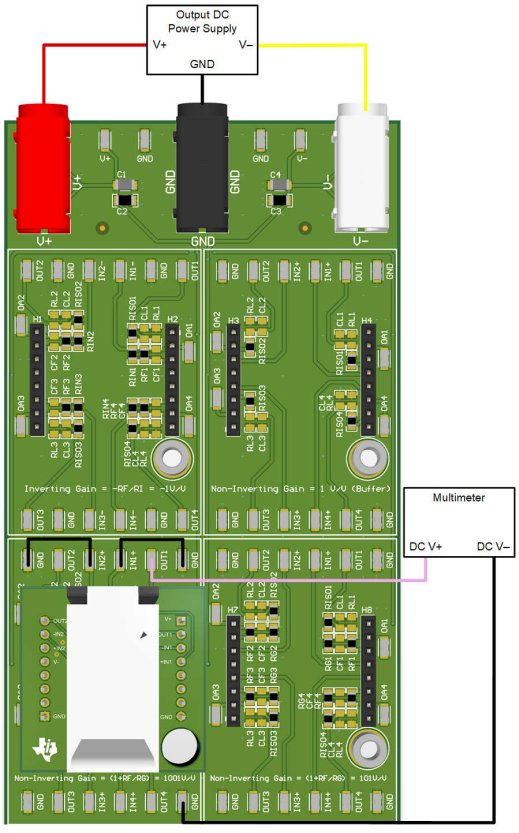


Figure 2-12. Vos Measurement Example Setup for a Dual Channel Device

Voltage Output Swing from Supply Voltages (V_{OL}/V_{OH})

V_{OH} and V_{OL} are the voltage limit of the output of the op amp as the output approaches the V+ and V- of the device.

Additional equipment needed for this test:

- Digital multimeter (DMM) or a voltmeter

While referencing Section 2.3 to measure V_{OH} and V_{OL}

1. Install a daughtercard onto the *Non-Inverting Gain = 1V/V (Buffer)* preconfigured circuit. For non-rail-to-rail input op amps, the amplifier needs to be placed in a gain to try to force the output to either rail.
2. Connect the triple power supply to the *V+*, *GND*, and *V-* of AMP-PDK-EVM while matching the device's data sheet conditions. The current limit of the power supply needs to be set to the I_{SC} + I_Q of the device (considering all channels).
3. Connect the single power supply between *INx+* pin and *GND*. Set the single supply voltage to the *V+* value of the op amp. The current limit of the power supply must be set to 9mA.
4. Connect one port of the DMM to *OUTx* and the other to *GND*.
5. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All other *INx+* pins on the sub-circuit must be connected to *GND*quie.
6. Configure DMM to measure DC voltage.
7. Turn on the triple power supply first; subsequently, turn on the single power supply.
8. The V_{OH} is the difference between *V+* and the voltage measured on the DMM.
9. Swap the single supply connections listed in Step #3. The positive supply must be connected to *GND* and ground from the supply must be connected to *+INx* pin.
10. The V_{OL} is the difference between *V+* and absolute value of voltage measured on the DMM.

With all other data sheet conditions matched, this test setup helps verify the voltage output swing from rail in the data sheet with the calculated.

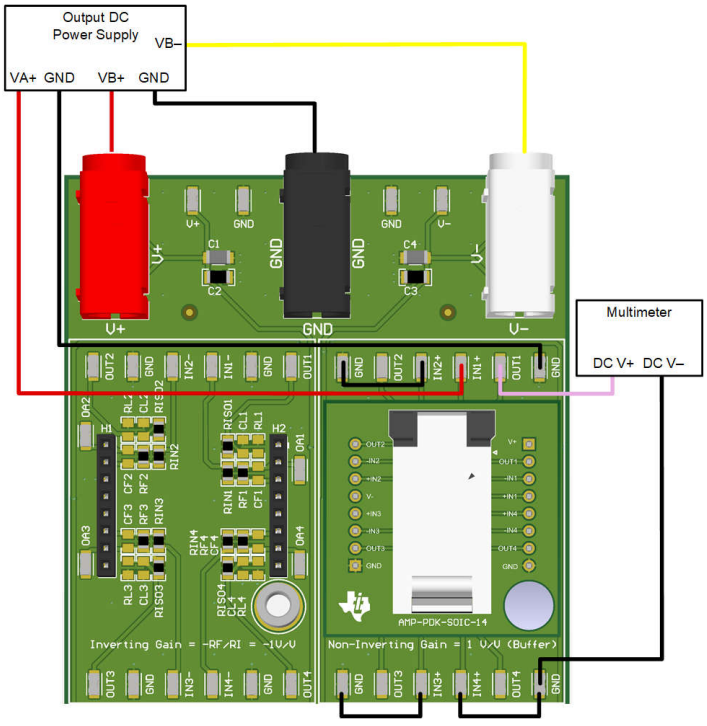


Figure 2-13. VOH Measurement Example for a Quad Channel Device

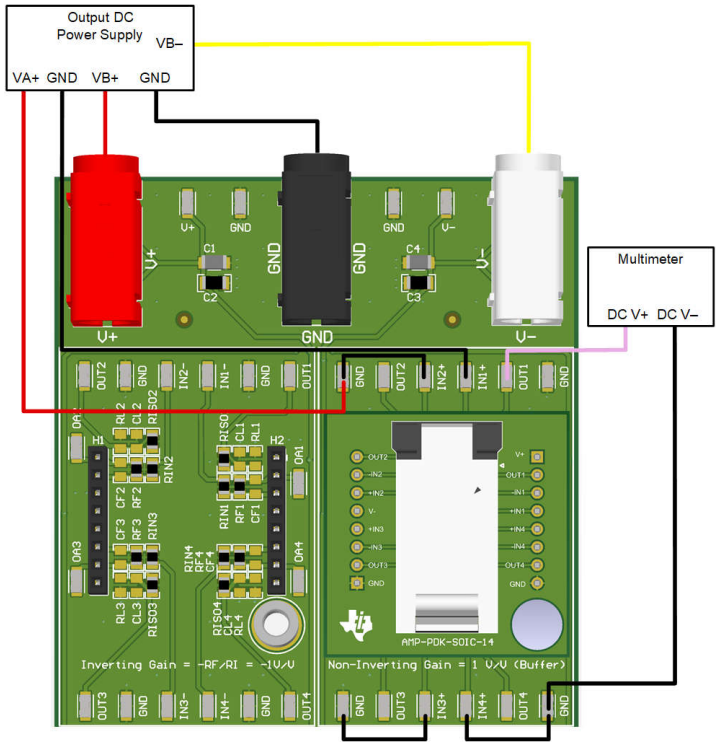


Figure 2-14. VOL Measurement Example for a Quad Channel Device

Gain Bandwidth Product (GBWP)

Additional equipment needed for this test:

- Digital multimeter (DMM) or a voltmeter
- Waveform function generator

While referencing Section 2.3 to measure GBW,

1. Install a daughtercard onto the *Non-Inverting Gain = 101V/V* preconfigured circuit.
2. Connect the triple power supply to the *V+*, *GND*, and *V-* of AMP-PDK-EVM while matching the device's data sheet conditions. The current limit of the power supply must be set to the I_{SC} + I_Q of the device (considering all channels).
3. Connect the output of the frequency generator to the *INx+* pin and reference to *GND*.
4. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All other *INx+* pins on the sub-circuit must be connected to *GND*.
5. Connect one DMM port to *OUTx* and the other to *GND*.
6. Turn on the power supply output.
7. Configure the waveform generator to output a small signal (20mVpp, 100Hz, 0 offset voltage).
8. Turn on the waveform function generator.
9. Configure DMM to measure AC voltage. Record the DMM voltage.
10. Increase the frequency on the waveform generator until the DMM reads 70.7% of the original DMM voltage. Record the frequency of the waveform generator.
11. Multiply the frequency by the gain of the preconfigured circuit.

With all other data sheet conditions matched, this test setup helps verify the gain bandwidth product in the data sheet with the calculated.

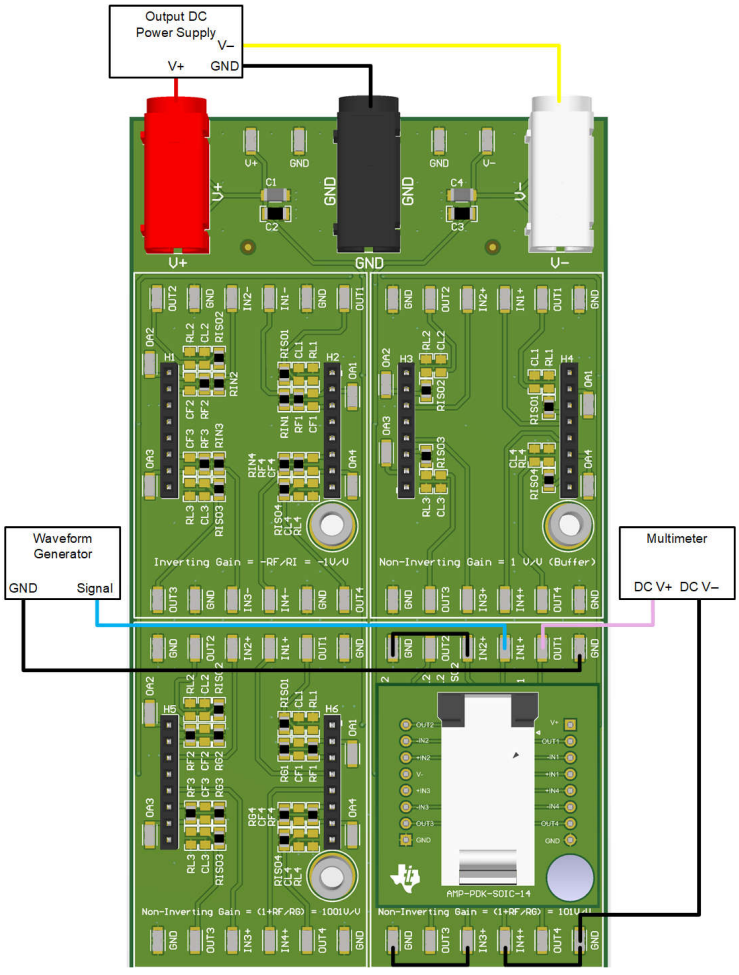


Figure 2-15. BW Measurement Example for Quad Channel Device

Slew Rate (SR)

SR is the maximum rate of change of an op amp's output voltage in volts per microsecond.

Additional equipment needed for this test:

- Oscilloscope
- Waveform function generator

While referencing Section 2.3 to measure SR,

1. Install a daughtercard onto the *Non-Inverting Gain = 1V/V (Buffer)* preconfigured circuit.
2. Connect the triple power supply to the *V+*, *GND*, and *V-* of AMP-PDK-EVM while matching the device's data sheet conditions. The current limit of the power supply must be set to the I_{SC} + I_Q of the device (considering all channels).
3. Connect the waveform generator to the *INx+* pin with a reference to *GND*. The input signal must be step function the size of the input voltage common mode listed in the data sheet.
4. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All other *INx+* pins on the sub-circuit must be connected to *GND*.
5. Connect an oscilloscope probe to the *OUTx* with a probe referenced to *GND*.
6. Turn on the power supply output.
7. Turn on the waveform function generator.
8. Configure the oscilloscope to measure approximately 10% and 90% of the output waveform, note the time differential. Slew rate is the rate of change in volts per microsecond.

With all other data sheet conditions matched, this test setup helps verify the slew rate in the data sheet with the one calculated.

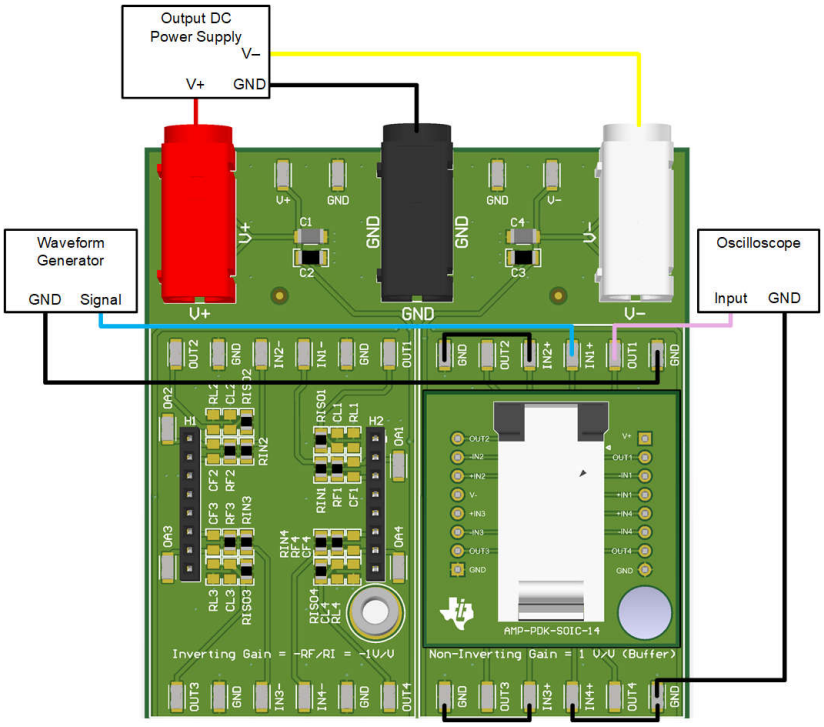


Figure 2-16. SR Measurement Example for a Single Channel Device

Comparators Setup

The AMP-PDK-EVM kit has the capability of testing basic functionality of comparators using the pin-to-pin circuit. Do not test a comparator device with any of the other gain configurations as this can result in measurement errors. Positive feedback or hysteresis setup is not available with the board.

The backside of the pin-to-pin board contains an option to populate pull-up resistors *Rupx* on the output of the comparator, as shown in Figure 2-17. By default, *Rupx* are unpopulated.

Rupx is required to populate for any comparator that has an open-drain/open-collector output type. Without the pull-up resistor, the output of the comparator can float to an unknown state. This resistor does not need to be populated when using push-pull devices. The output type of the comparator can be verified in the product page and data sheet.

For more information on comparators, please reference TI Precision Labs.

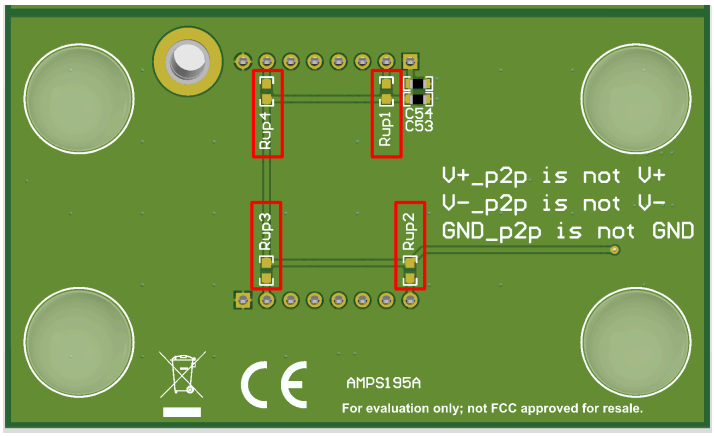


Figure 2-17. Pin-to-Pin Circuit (Back View)

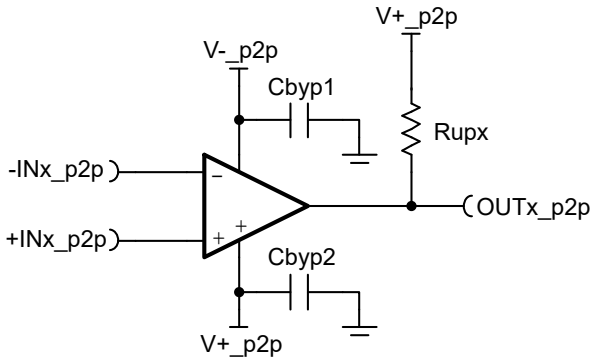


Figure 2-18. Pin-to-pin Schematic with Pull-Up Resistor Option

Advanced Test Setup

The above test setups are solderless preconfigured op amp designs with the options of a gain of 1, 101, 1001, and -1. The board can also be re-purposed in different gain ratios by changing the passive components. In addition to the existing populated passives, there is compensation circuitry options included to limit noise (C_F) and help improve stability (R_{ISO}) as seen in Schematics. The *OAx* test point is given to help verify amplifier stability. For more resources on op amp noise and stability, please reference TI Precision Labs.

2.6 Header Information

The AMP-PDK-EVM has surface mount test points populated on the board. The surface mount test points best connect to a banana jack to clip cable or an oscilloscope probe. There are also black headers in each circuit to allow the interface between the AMP-PDK-EVM and a daughtercard. If connecting a piece of equipment that has BNC connections, then TI recommends to use a *BNC-to-clip* adapter.

2.7 Interfaces

The AMP-PDK-EVM has hardware interfaces between the AMP-PDK-EVM, the daughtercard, and the device as seen earlier in Figure 1-1. The daughtercard can only be plugged in one way due to the metal alignment poles. The device can be plugged in several directions, therefore TI recommends to reference the figures below. Single channel daughtercards have a shutdown enable option via a header on the top right of the board. Refer to the corresponding device data sheet to determine which configuration to set the two-pin jumper to enable or disable shutdown mode.

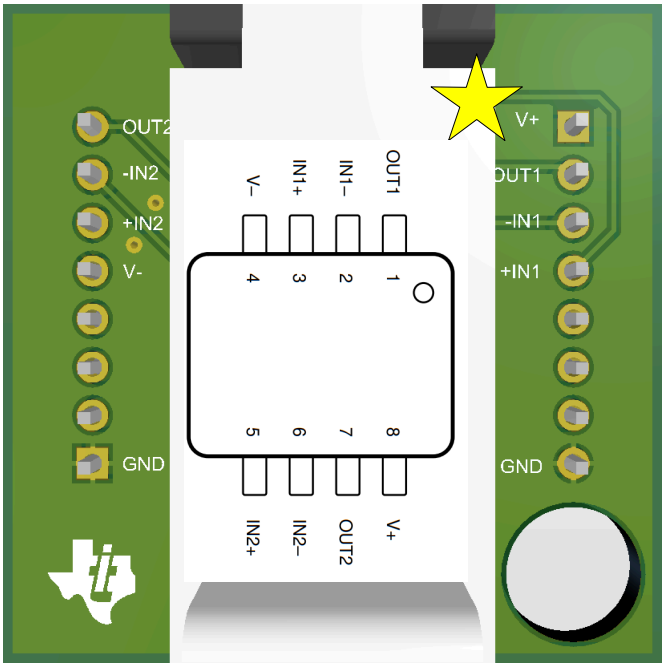


Figure 2-19. AMP-PDK-VSSOP-8 - Pin 1 Orientation Example

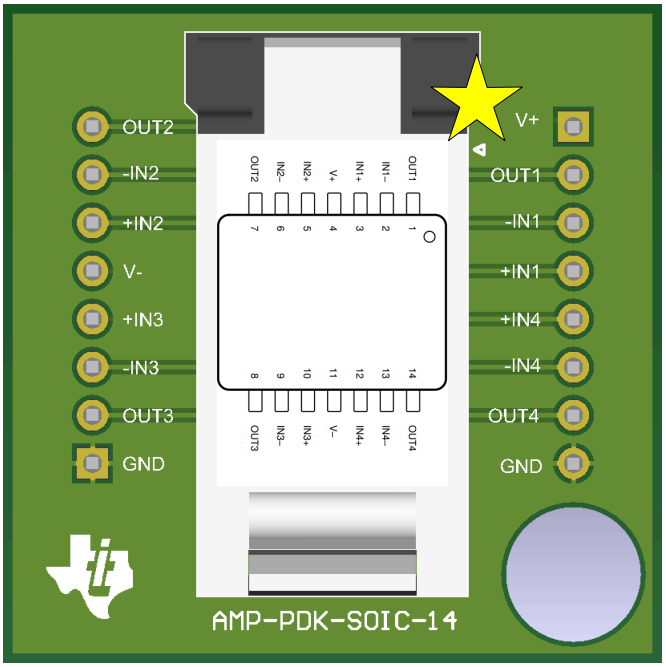


Figure 2-20. AMP-PDK-SOIC-14 - Pin 1 - Orientation Example

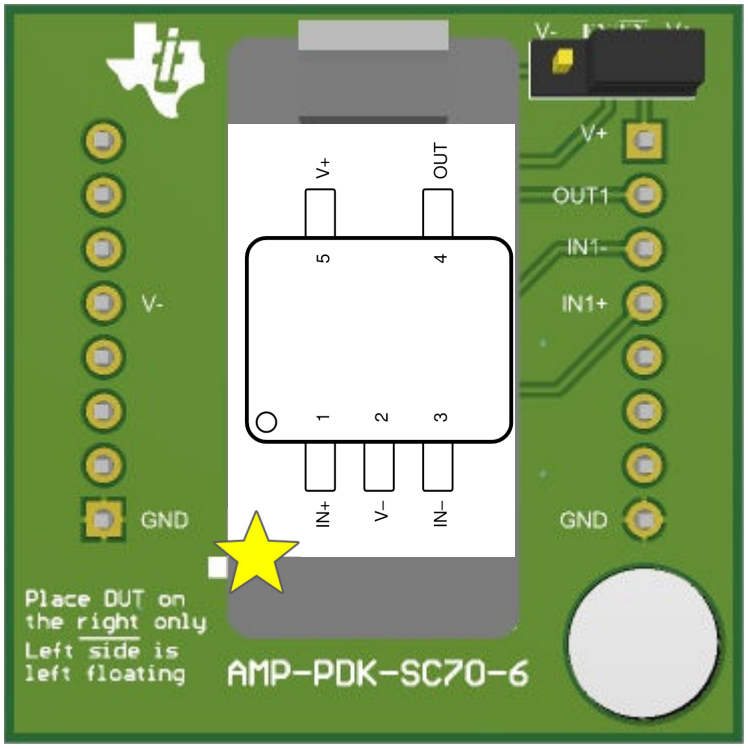


Figure 2-21. AMP-PDK-SC70-6 - Pin 1 - Orientation Example

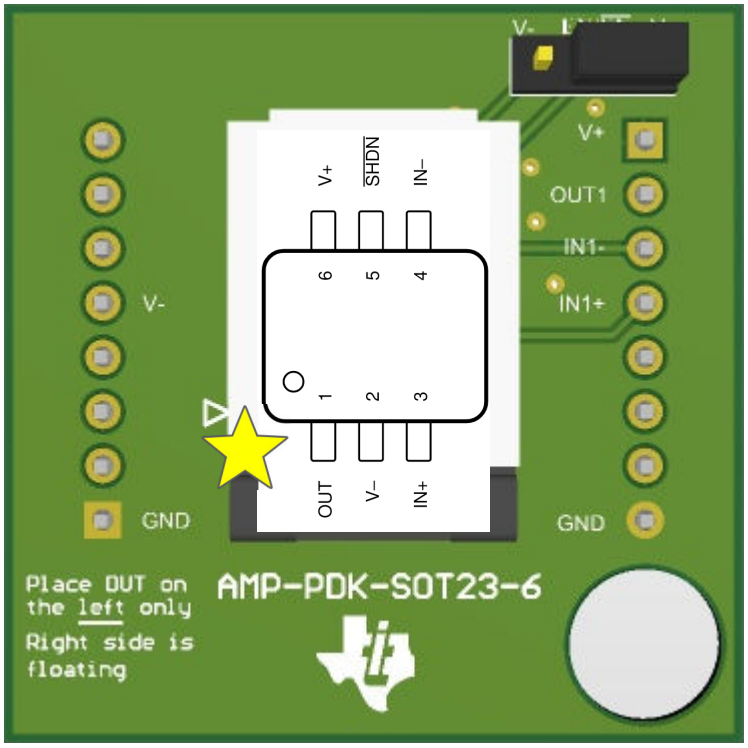


Figure 2-22. AMP-PDK-SOT23-6 - Pin 1 - Orientation Example

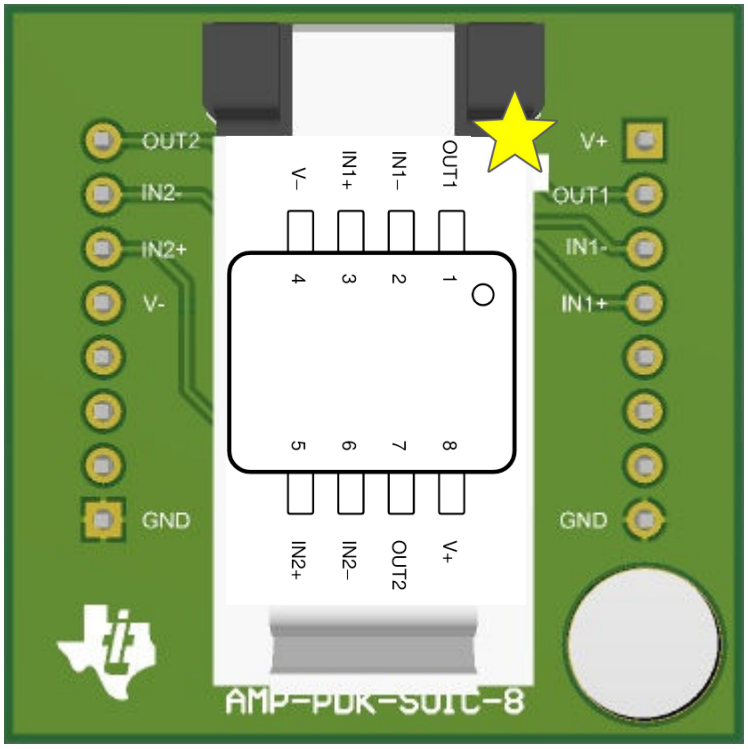


Figure 2-23. AMP-PDK-SOIC-8 - Pin 1 - Orientation Example

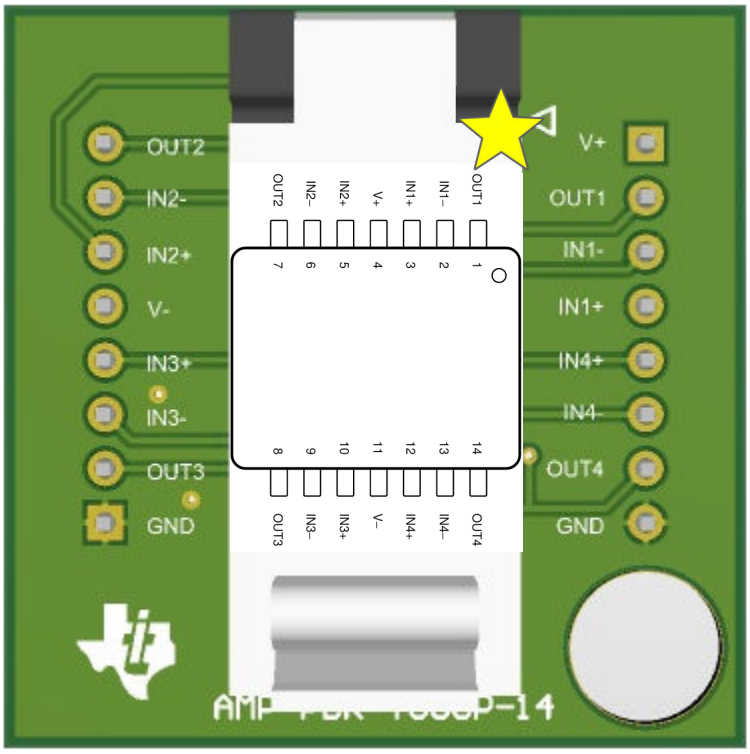


Figure 2-24. AMP-PDK-TSSOP-14 - Pin 1 - Orientation Example

2.8 Best Practices

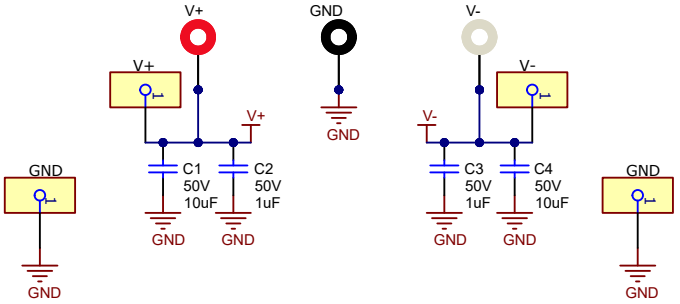
For best user-experience, the following are recommended:

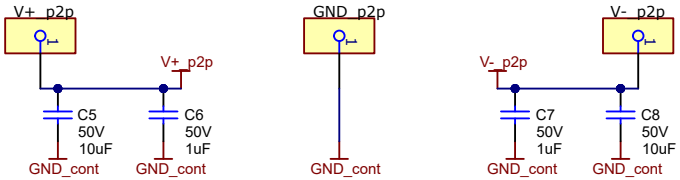
1. Implement Section 2.3.
2. If not already populated, solder on bypass capacitors on daughter card and the main board.
3. Reference stability resources for robust op amp designs.
4. Only utilize the ground surface mount test points as a ground reference. Avoid connecting *GND* and *GND_p2p* to the metal alignment poles. The alignment metal poles are mechanically but not electrically connected and can introduce a ground shift potential.

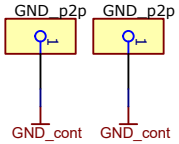
3 Hardware Design Files

3.1 Schematics

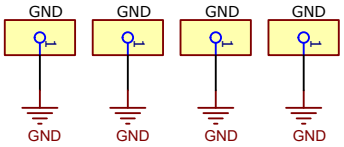
Power Supplies



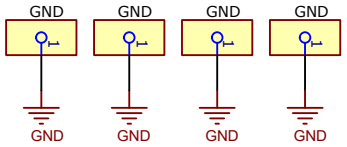




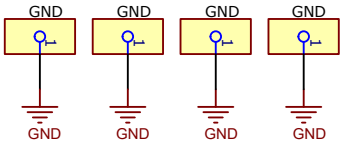
Non-inverting gain of 1 (Buffer)



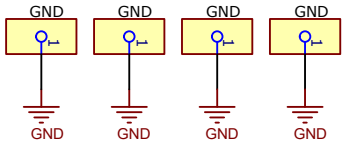
Inverting gain of -1



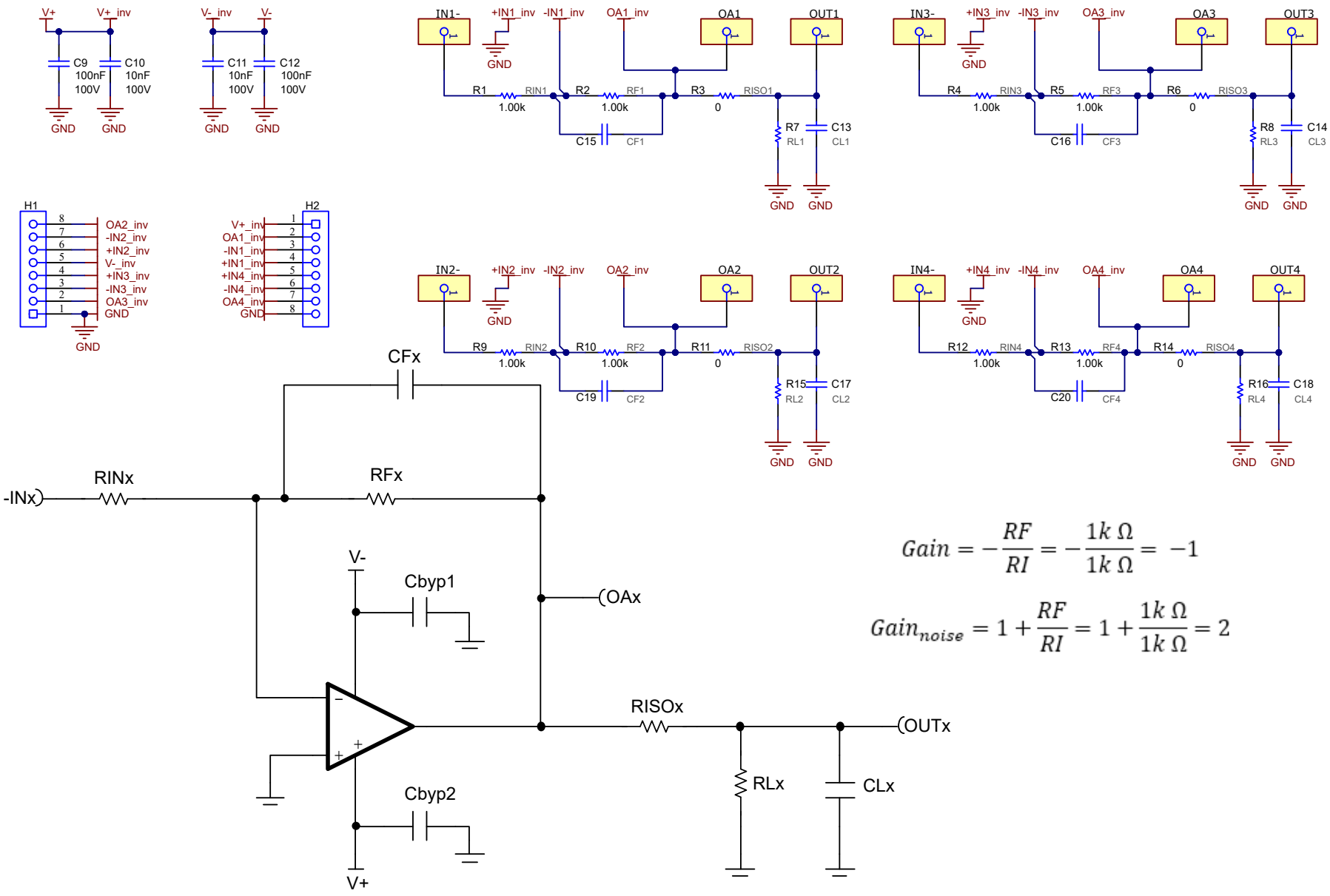
Non-inverting gain of 101



Non-inverting gain of 1001



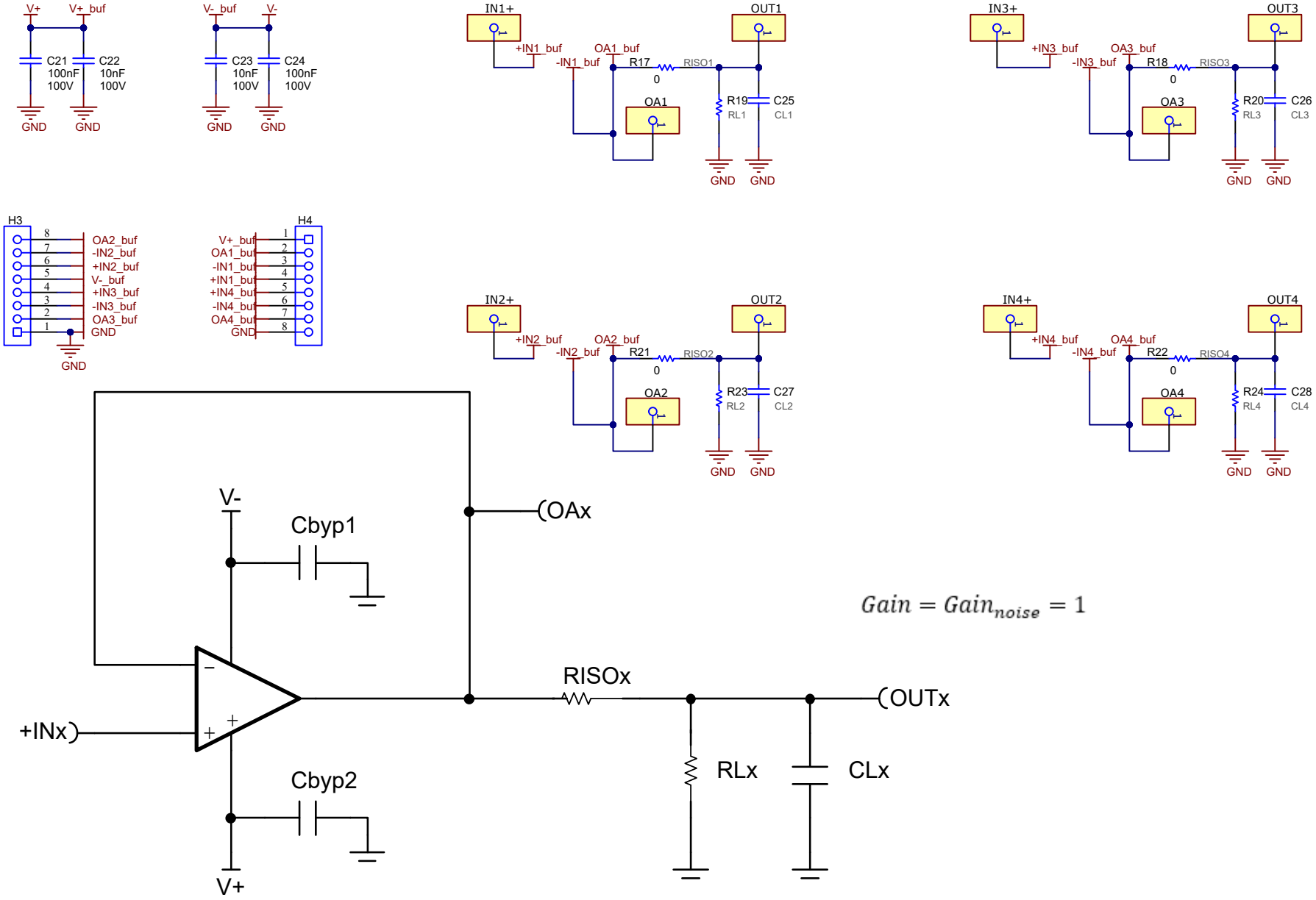
Inverting Gain of -1



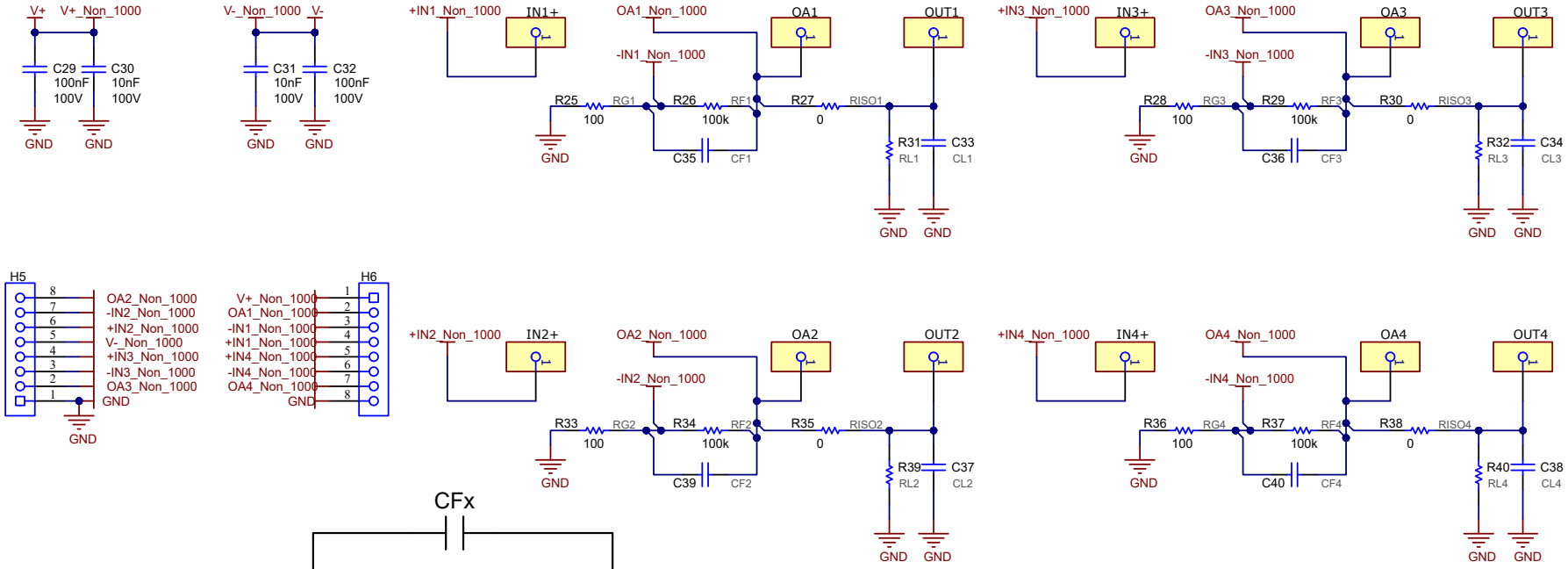
$$Gain = -\frac{RF}{RI} = -\frac{1k\,\Omega}{1k\,\Omega} = -1$$

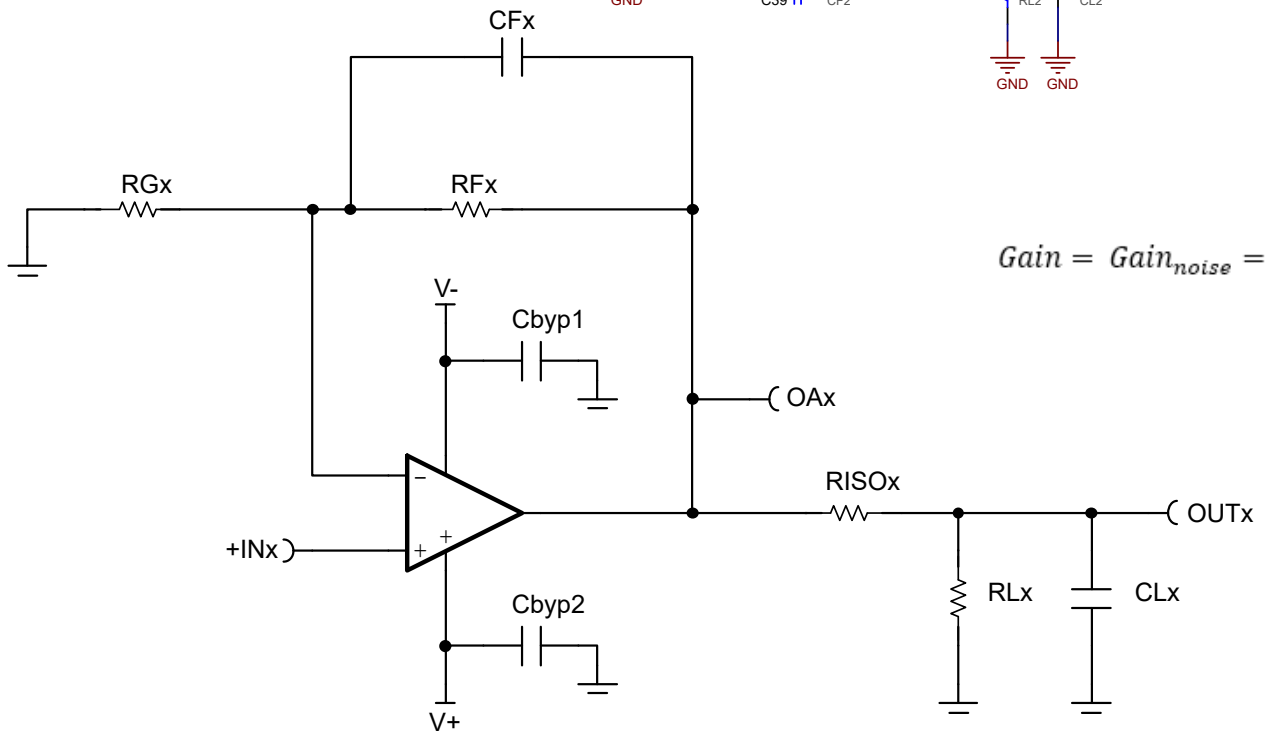
$$Gain_{noise} = 1 + \frac{RF}{RI} = 1 + \frac{1k\,\Omega}{1k\,\Omega} = 2$$

Non-inverting gain of 1 (Buffer)



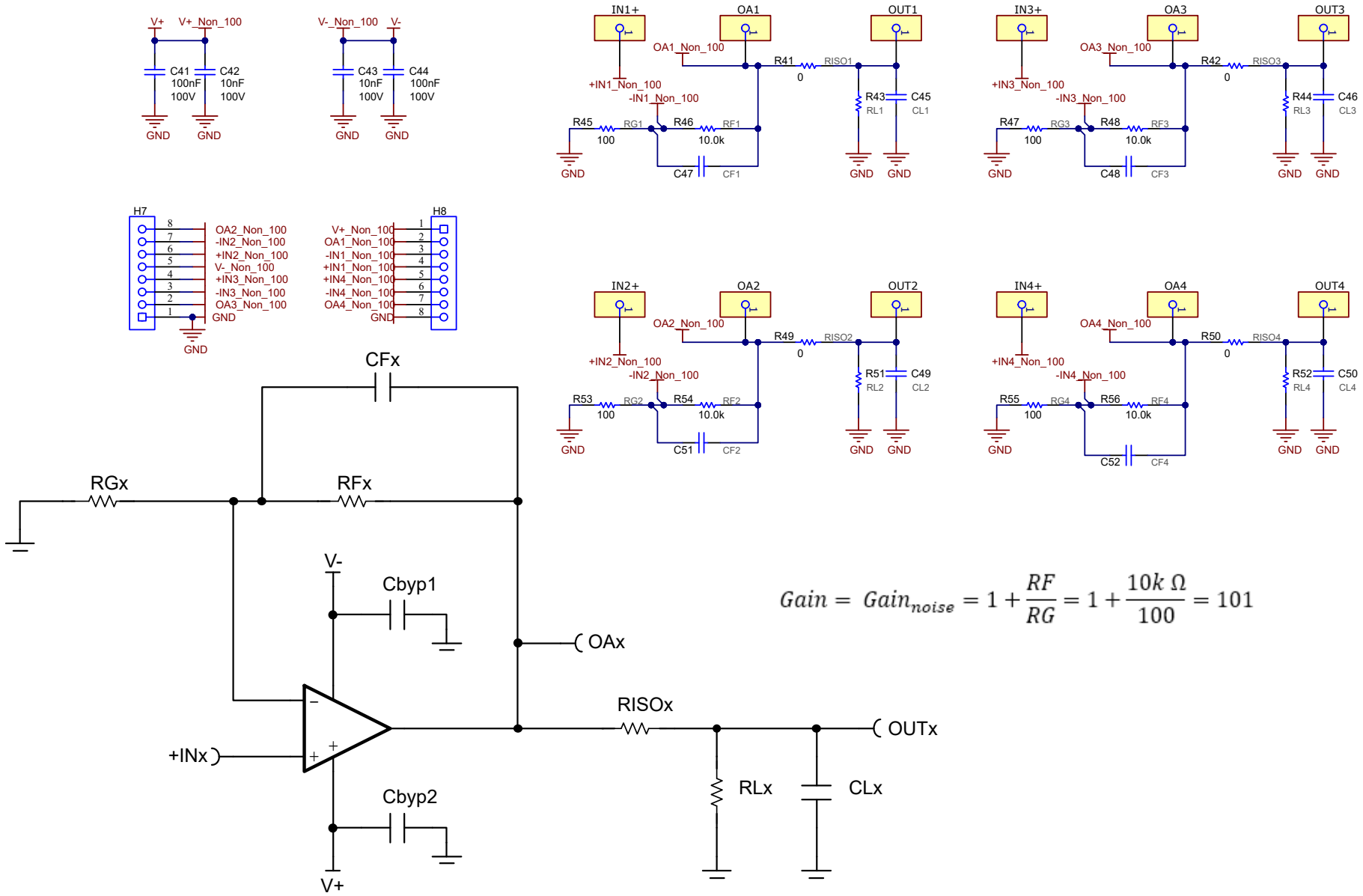
Non-inverting gain of 1001





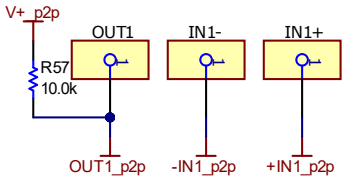
$$Gain = Gain_{noise} = 1 + \frac{RF}{RG} = 1 + \frac{100k\ \Omega}{100\ \Omega} = 1001$$

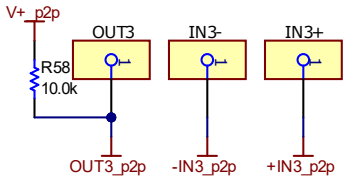
Non-inverting gain of 101

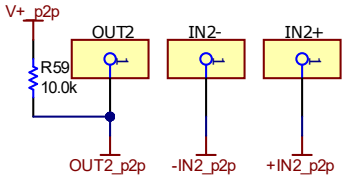


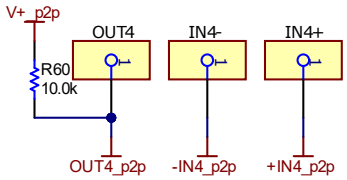
$$Gain = Gain_{noise} = 1 + \frac{RF}{RG} = 1 + \frac{10k\,\Omega}{100} = 101$$

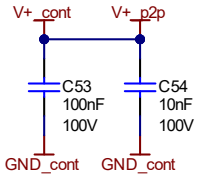
Pin-to-pin

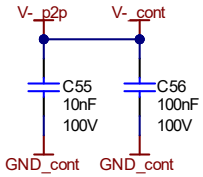


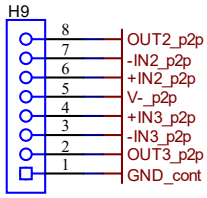


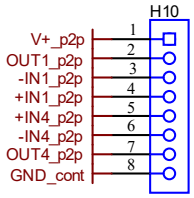




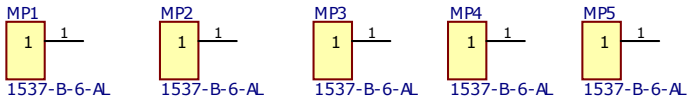


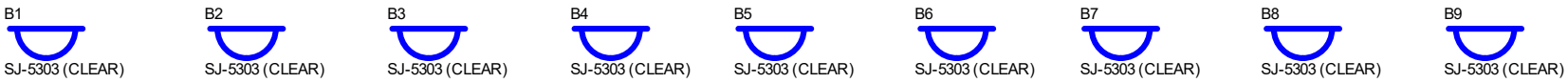






Hardware





PCB Number: AMPS195
PCB Rev: A

PCB
LOGO
Texas Instruments

CE Mark

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

Variant/Label Table	
Variant	Label Text
001	AMPS195A

LBL1
PCB Label
AMPS195A
Size: 0.65" x 0.20 "

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ4
Label Assembly Note
This Assembly Note is for PCB labels only

3.2 PCB Layouts

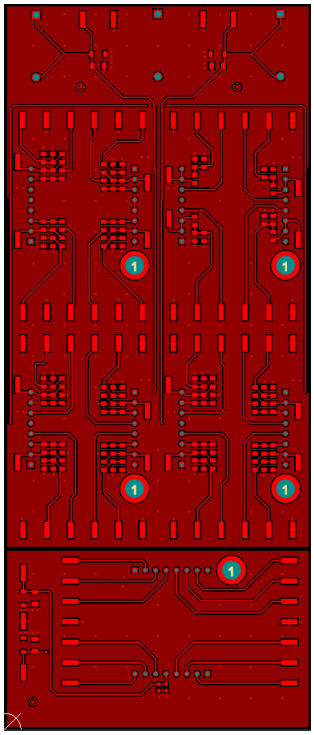


Figure 3-1. AMP-PDK-EVM Top Layer

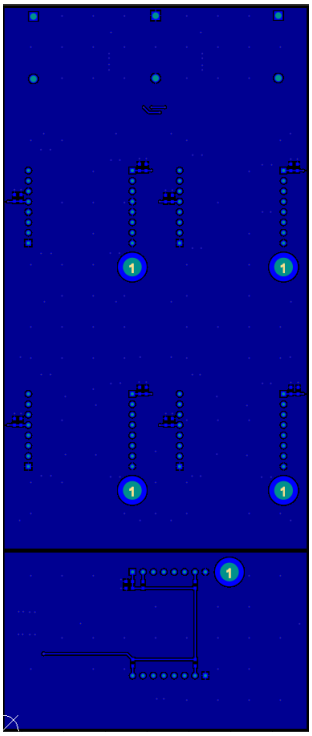


Figure 3-2. AMP-PDK-EVM Bottom Layer

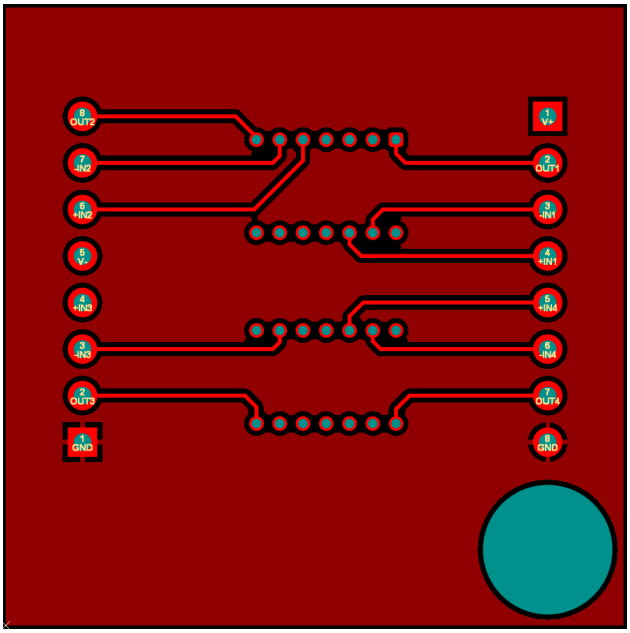


Figure 3-3. AMP-PDK-SOIC-14 Top Layer

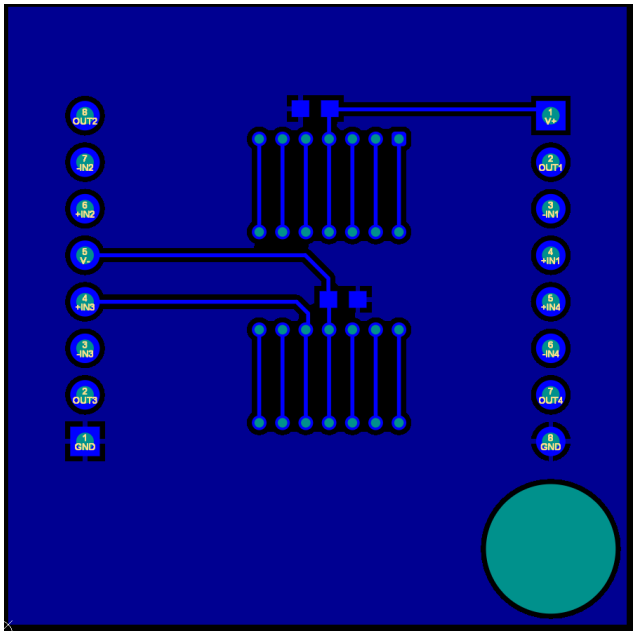


Figure 3-4. AMP-PDK-SOIC-14 Bottom Layer

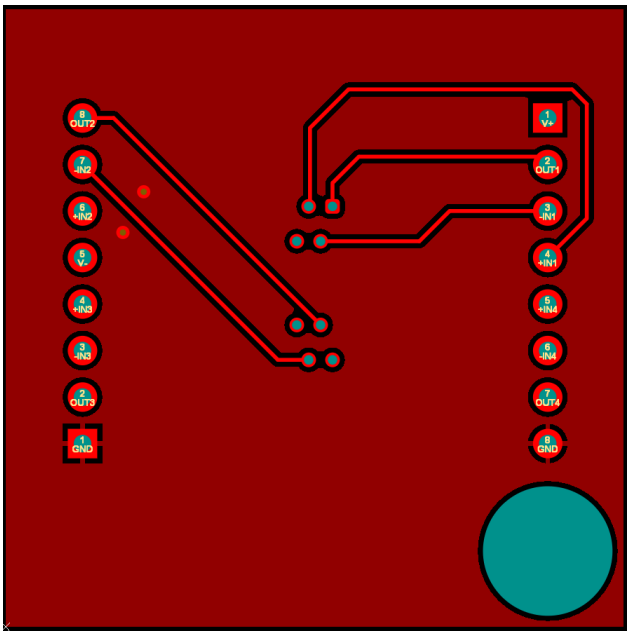


Figure 3-5. AMP-PDK-VSSOP-8 Top Layer

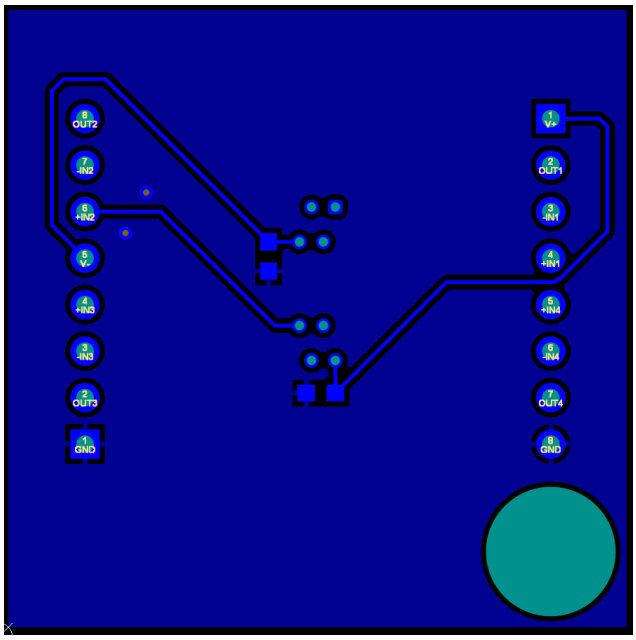


Figure 3-6. AMP-PDK-VSSOP-8 Bottom Layer

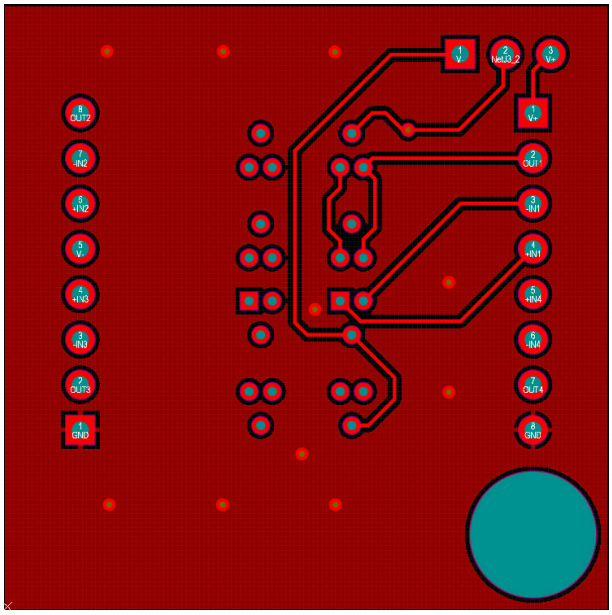


Figure 3-7. AMP-PDK-SC70-6 Top Layer

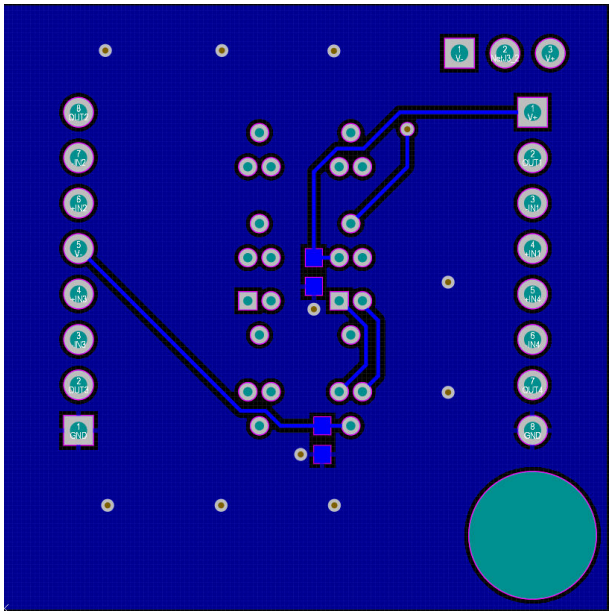


Figure 3-8. AMP-PDK-SC70-6 Bottom Layer

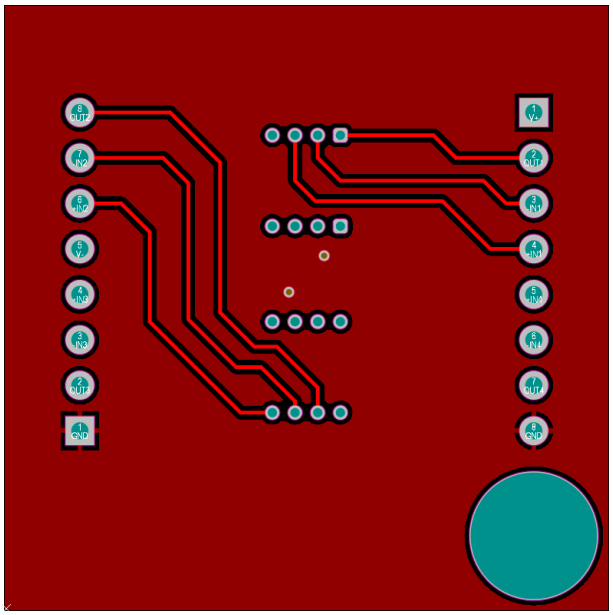


Figure 3-9. AMP-PDK-SOIC-8 Top Layer

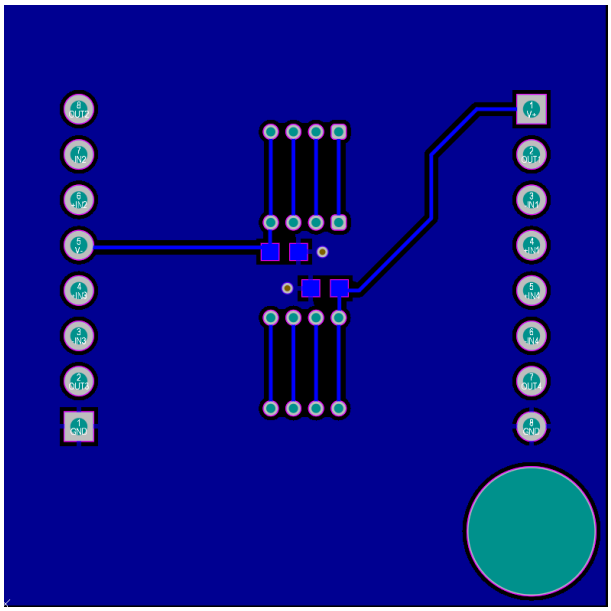


Figure 3-10. AMP-PDK-SOIC-8 Bottom Layer

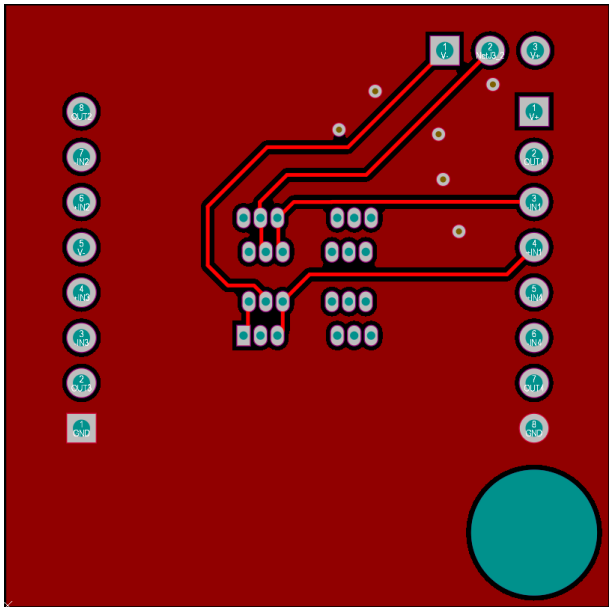


Figure 3-11. AMP-PDK-SOT23-6 Top Layer

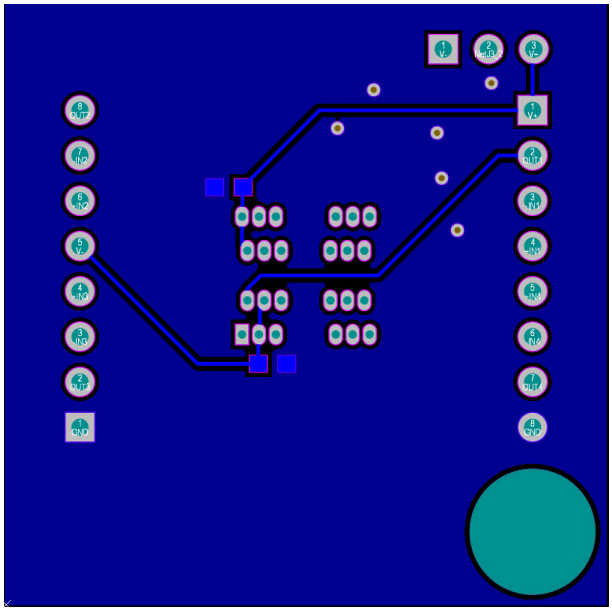


Figure 3-12. AMP-PDK-SOT23-6 Bottom Layer

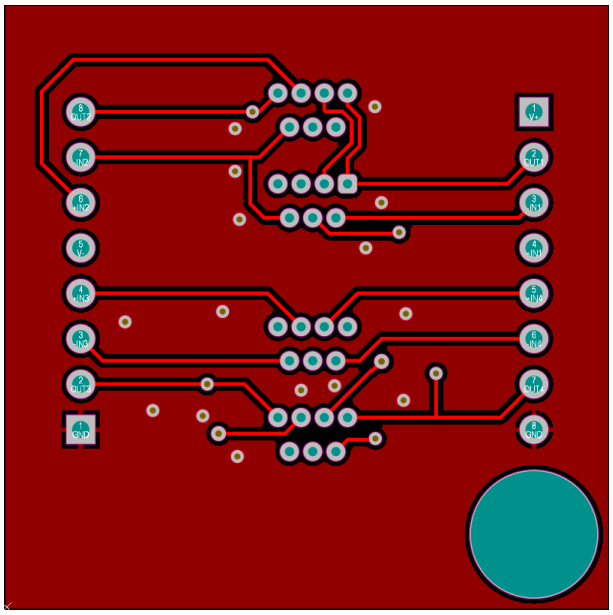


Figure 3-13. AMP-PDK-TSSOP-14 Top Layer

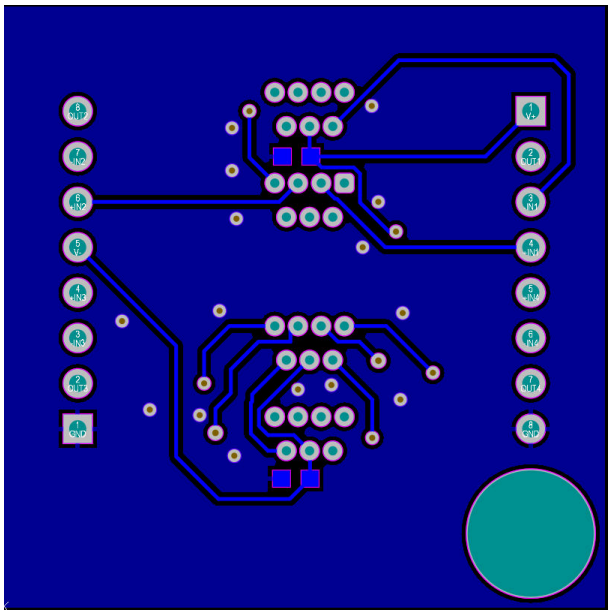


Figure 3-14. AMP-PDK-TSSOP-14 Bottom Layer

3.3 Bill of Materials (BOM)

Table 3-1. AMP-PDK-EVM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1	AMP-PDK-EVM	Printed Circuit Board		AMP-PDK-EVM	Any
B1, B2, B3, B4, B5, B6, B7, B8, B9	9		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
C1, C4, C5, C8	4	10uF	CAP, CERM, 10uF, 50V, +/- 10%, X5R, AEC-Q200 Grade 1, 1206	1206	GRT31CR61H106KE01L	MuRata
C2, C3, C6, C7	4	1uF	CAP, CERM, 1uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	GCM31MR71H105KA55L	MuRata
C9, C12, C21, C24, C29, C32, C41, C44, C53, C56	10	0.1uF	CAP, CERM, 0.1uF, 100V, +/- 10%, X7R, 0603	603	GRM188R72A104KA35D	MuRata
C10, C11, C22, C23, C30, C31, C42, C43, C54, C55	10	0.01uF	CAP, CERM, 0.01uF, 100V, +/- 10%, X7R, 0603	603	C0603X103K1RACTU	Kemet
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4, H5, H6, H7, H8, H9, H10	10		Receptacle, 2.54mm, 8x1, Tin, TH	Receptacle, 2.54mm, 8x1, TH	PPTC081LFBN-RC	Sullins Connector Solutions
J1	1		Standard Banana Jack, insulated, 10A, red	571-0500	571-0500	DEM Manufacturing
J2	1		Standard Banana Jack, insulated, 10A, black	571-0100	571-0100	DEM Manufacturing
J3	1		Standard Banana Jack, insulated, 10A, white	571-0600	571-0600	DEM Manufacturing
J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88	85		PC Test Point Plating Surface Mount Mounting Type	SMT_TP	RCWCTE	KOA Speer

Table 3-1. AMP-PDK-EVM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1, MP2, MP3, MP4, MP5	5			SPACER_0IN25	1537-B-6-AL	RAF Electronic
R1, R2, R4, R5, R9, R10, R12, R13	8	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1001V	Panasonic
R3, R6, R11, R14, R17, R18, R21, R22, R27, R30, R35, R38, R41, R42, R49, R50	16	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic
R25, R28, R33, R36, R45, R47, R53, R55	8	100	RES, 100, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEYJ101V	Panasonic
R26, R29, R34, R37	4	100k	RES, 100 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1003V	Panasonic
R46, R48, R54, R56	4	10.0k	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1002V	Panasonic
C13, C14, C15, C16, C17, C18, C19, C20, C25, C26, C27, C28, C33, C34, C35, C36, C37, C38, C39, C40, C45, C46, C47, C48, C49, C50, C51, C52	0	100pF	CAP, CERM, 100pF, 50V,+/- 5%, C0G/NP0, 0805	805	8.85012E+11	Wurth Elektronik
R7, R8, R15, R16, R19, R20, R23, R24, R31, R32, R39, R40, R43, R44, R51, R52	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic
R57, R58, R59, R60	0	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0FKEA	Vishay-Dale

Table 3-2. AMP-PDK-SOIC-14

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS197	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1µF, 25V,+/- 10%, X7R, 0603	603	GRM188R71E104KA01D	MuRata
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
U1	1		Socket, SOIC-14 Kelvin, 1.27mm Pitch	Socket, SOIC-14, 1.27mm Pitch	04337 161 6218F	Loranger

Table 3-3. AMP-PDK-VSSOP-8

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS201	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1µF, 25V,+/- 10%, X7R, 0603	603	GRM188R71E104KA01D	MuRata
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
XU1	1		Socket, MSOP-8, 25.6mil Pitch	Socket, MSOP-8, 25.6mil Pitch	04335 081 6218B	Loranger

Table 3-4. AMP-PDK-SC70-6

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS196	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
J3	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
U1	1		Socket, Kelvin, 2x6 Lead SOIC, TH	510x740x1050 mil Socket	04335 121 X215	Loranger

Table 3-5. AMP-PDK-SOIC-8

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS198	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
U1	1		Socket, SOIC-8 Kelvin, 1.27mm Pitch	Socket, SOIC-8 Kelvin, 1.27mm Pitch	04337 081 6218A	Loranger

Table 3-6. AMP-PDK-SOT23-6

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS199	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1µF, 25V,+/- 10%, X7R, 0603	603	GRM188R71E104KA01D	MuRata
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
J3	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
XU1	1		Socket, 2xSOT-23-6, 0.95mm Pitch	Socket, 2xSOT-23-6, 0.95mm Pitch	04331 121 6217	Loranger

Table 3-7. AMP-PDK-TSSOP-14

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS200	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
XU1	1		Socket, TSSOP-14 Kelvin, 0.65mm Pitch	Socket, SOP-14 Kelvin, 0.65mm Pitch	04335 161 6218B	Loranger

4 Additional Information

4.1 Trademarks

All trademarks are the property of their respective owners.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2024) to Revision B (September 2024)	Page
• Changed the steps in the *Gain Bandwidth Product (GBWP)* setup section	7

Changes from Revision * (April 2024) to Revision A (July 2024)	Page
• Added AMP-PDK-SC70-6, AMP-PDK-SOIC-8, AMP-PDK-SOT23-6, and AMP-PDK-TSSOP-14 throughout document	1

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