Application Report
SBOA135–May 2013

Considerations for High-Gain Multistage Designs

ABSTRACT

Amplifying a voltage signal by more than 100 V/V using a single operational amplifier while maintaining several MHz, or even tens of MHz of bandwidth, can prove difficult to both design and to implement. This application report discusses the noise, bandwidth, and stability requirements prior to developing physical implementation.

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1 Signal-Chain Considerations

1.1 Input Noise

Starting with the traditional gain-bandwidth product (GBWP), where the product of the gain and the bandwidth is constant for a voltage-feedback amplifier (as shown in Equation 1), a quick survey of nonunity gain stable amplifiers that achieve the highest possible GBWP and low noise yields the results shown in Table 1.

$$Gain \times Bandwidth = GBWP \quad (1)$$

Table 1. High GBWP Product and Low-Noise Devices

Part Number	Input Voltage Noise Density (nV/√Hz)	GBWP (MHz)
OPA847	0.85	3900
OPA846	1.1	1800
LMH6629	0.69	3900

Note that FET input devices have not been considered here because the input voltage noise tends to be high, while input current noise is low. Because low value resistors are used to minimize noise contribution, the low input bias current of a FET amplifier is not needed here; only relatively low input impedance voltage sources are considered.

1.2 Noise Considerations

Consider using a noninverting amplifier architecture, allowing its input impedance to be matched to any source impedance as well as minimizing system noise. Also at high-gain, the output voltage noise density can be approximated as shown in Equation 2:

$$e_o \cong \left(e_n + \sqrt{4kTR_S}\right) \times \left(1 + \frac{R_F}{R_G}\right) \quad (2)$$

where

- k = 1.380658 × 10^{-23}
- T = temperature in kelvins

Note that in this model, both the current noise and the resistor noise are considered negligible.

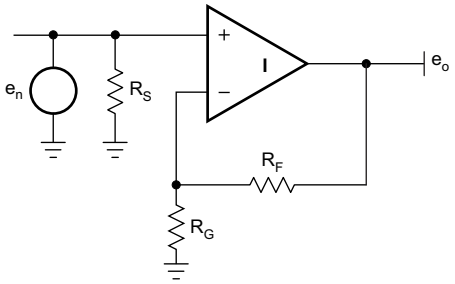

Figure 1. Simplified Noise Model

The SNR for such a configuration is shown in Equation 3

$$SNR_{(dB)} = 20 \times log\left(\frac{V_{orms}}{e_o \times \sqrt{NPWB}}\right)$$

where NPBW = the noise power bandwidth of the stage. (3)

Each stage amplifies the noise from the previous stage and adds its own noise. For two stages, the result is shown in Equation 4 or Equation 5:

$$e_{o\_2-stages\left(\frac{nV}{rtHz}\right)}^{2} = e_{o\_stage1(\frac{nV}{rtHz})}^{2} + \left(e_{o\_stage1(\frac{nV}{rtHz})}^{2} \times G_{Stage1}^{2}\right) + e_{o\_stage2(\frac{nV}{rtHz})}^{2} \quad (4)$$

$$e_{o\_2-stages\left(\frac{nV}{rtHz}\right)}^{2} = e_{o\_stage1(\frac{nV}{rtHz})}^{2} \times \left(1 + G_{Stage1}^{2}\right) + e_{o\_stage2(\frac{nV}{rtHz})}^{2} \quad (5)$$

The gain combines as the sum (in dB) of the gain of each stage as shown in Equation 6:

$$G_{Multi-Stage(dB)} = G_{Stage\_1(V/V)} \times G_{Stage\_2(V/V)} \times .. \times G_{Stage\_n(V/V)} \quad (6)$$

1.3 Other Stages

Because the noise of the first stage is the limiting factor from a noise perspective, any stage other than the first stage does not require very low noise. The entire current-feedback amplifier portfolio is now available for selection. Table 2 provides a selection of amplifiers suited to both high-gain and high-bandwidth applications.

Table 2. High Gain with High BW Portfolio

Part Number	Gain at BW (V/V)	BW (MHz)	Comment
OPA683	100	35	Lowest power solution
OPA684	100	70	Highest equivalent GBWP
OPA695	16	350	Highest BW solution

Note either inverting or noninverting gain circuits can be considered, depending on the amplifier and the desired bandwidth. The OPA695 achieves lower noise in an inverting configuration; whereas, the OPA683 and OPA684 achieve lower noise in the noninverting configuration.

Because we are set to achieve high gain on a single stage (100 V/V), the gain resistor can be as low as 10 Ω. In an inverting topology, this setting can place an additional constraint on the driving stage. In practice, keep the gain resistor between 10 Ω and 50 Ω, and do not exceed 1.5 kΩ for the feedback resistor. Remember that the frequency response is limited by the feedback resistor (R_F) and the feedback capacitor (C_F) pole; you will always have a parasitic feedback capacitor as a result of the component, layout, and so forth.

In the second section of this application report, the focus is on output offset voltage and stability issues and implementation.

2 Implementation and Stability Considerations

In the first section, this application report discussed signal-chain considerations to match required gain and bandwidth while maintaining sufficient SNR. Two issues remain to make this circuit easily implementable: the dc accuracy requirements and amplifier power-supply rejection ratio (PSRR).

2.1 Output Offset Voltage

The gain can be very large; therefore, any dc error in the first or even the second stage can prove fatal to any implementation. Care must be taken to make sure that the output offset voltage of the multistage amplifier is sufficient. AC-coupling, or making sure that the dc gain is in unity, is the simplest approach. (Implementing a dc-feedback loop is another option, but is beyond the scope of this discussion.)

2.2 Power-Supply Rejection Ratio (PSRR)

As a result of the high gain, the signal in the load creates some disturbance in the power supply, as shown in Figure 2. However, this disturbance does not appear in the simulation unless the line regulation of a nonideal power supply is implemented.

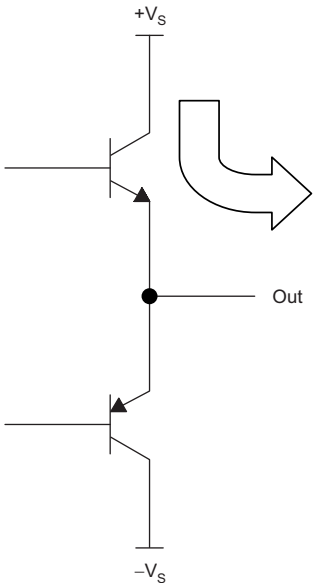

Figure 2. Operational Amplifier Emitter Output Stage

Such disturbance is seen by the first stage, and if the PSRR of the first amplifier is insufficient at the frequency of interest, the disturbance finds its way into the signal path, resulting in oscillations.

Preventing these oscillations requires careful planning in regards to the power supply. The power supply is connected directly to the last amplifier of the high-gain signal chain. From this last amplifier to the previous one, an inductor is placed in series in the power supply path. This inductor combined with the local bypass capacitor forms a low-pass filter and attenuates the disturbance. In the implementation shown, inductors are placed only in the positive supply.

A positive feedback loop created in the supply can happen on both positive and negative supplies; therefore, it may be necessary to implement this scheme on both supplies.

Additionally, a single operational amplifier must be used; oscillation occurs when using dual, triple, or quad amplifiers because they share the power supplies internally.

The schematic shown in Figure 3 reflects all the items discussed here, and shows a possible implementation for a +5-V single supply, providing 100,000-V/V amplification for a 10-µV source signal. Additional RC filters were added between stages to maximize SNR.

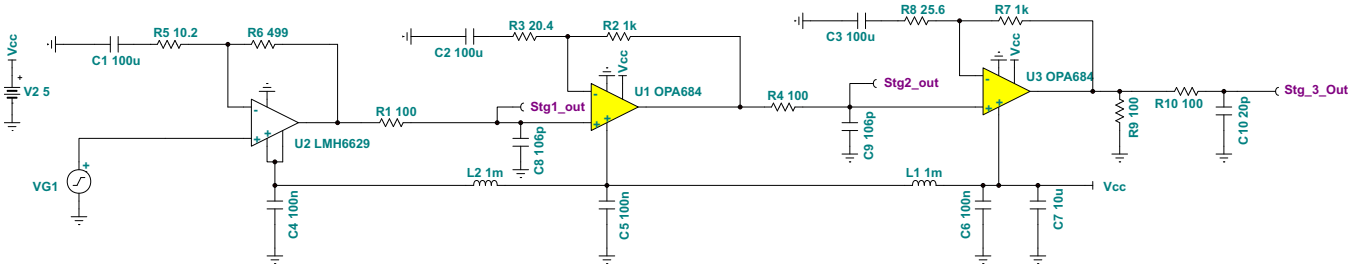

Figure 3. Final Simulation Schematic

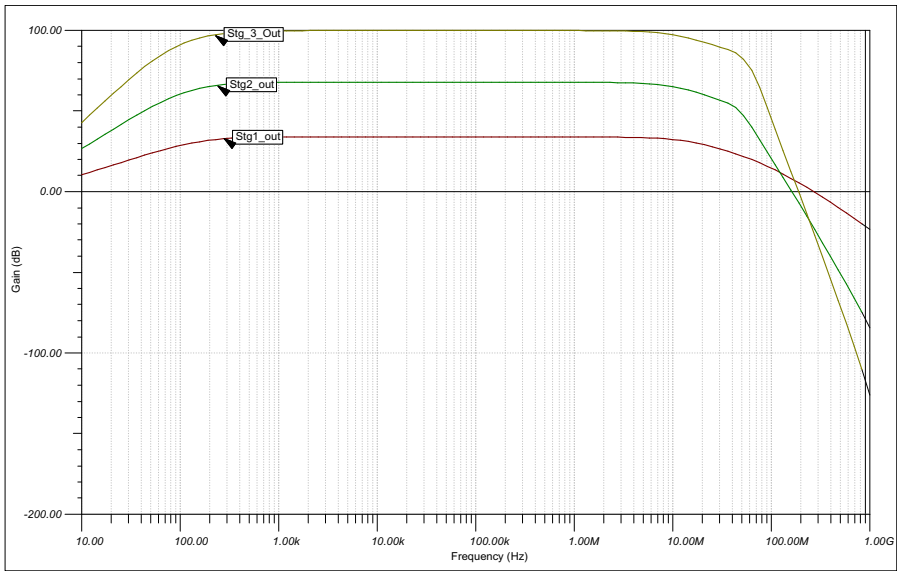

Figure 4. Simulated Frequency Response

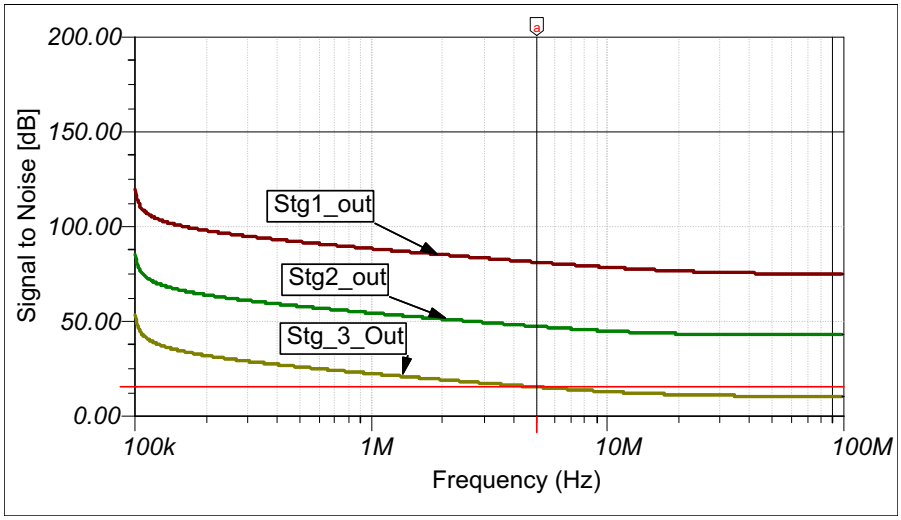

Figure 5. Simulated SNR

3 Circuit Implementation

Simulations are only proof of concepts and should be considered with caution. Therefore, a dedicated board for this circuit was designed to verify functionality.

The circuit is shown in Figure 6. Note there are two principal distinctions between the schematic simulated and its implementation:

1. The power supplies are bipolar.
2. The inductors on the negative supply are explicitly shown here.

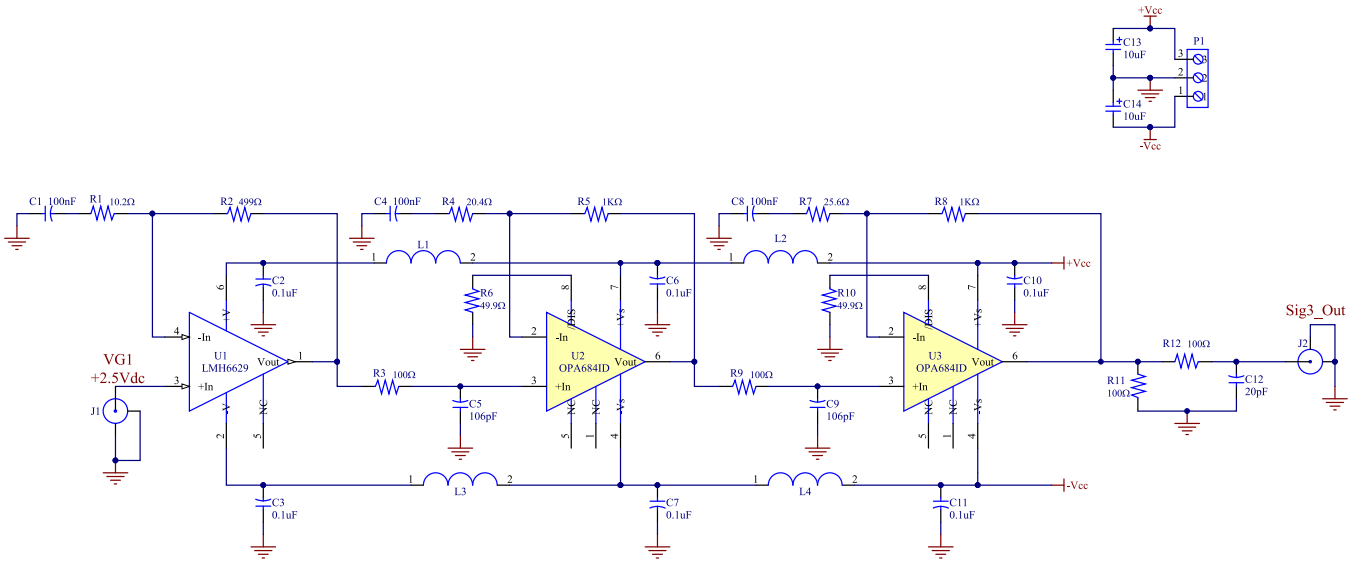

Figure 6. Implemented High-Gain, High-Bandwidth Circuit

The layout has three layers. The top layer has most of the circuitry, as shown in Figure 7. The middle layer contains the power supplies, as shown in Figure 8. The bottom layer is used for the ground plane, as well as component placement and is shown in Figure 9.

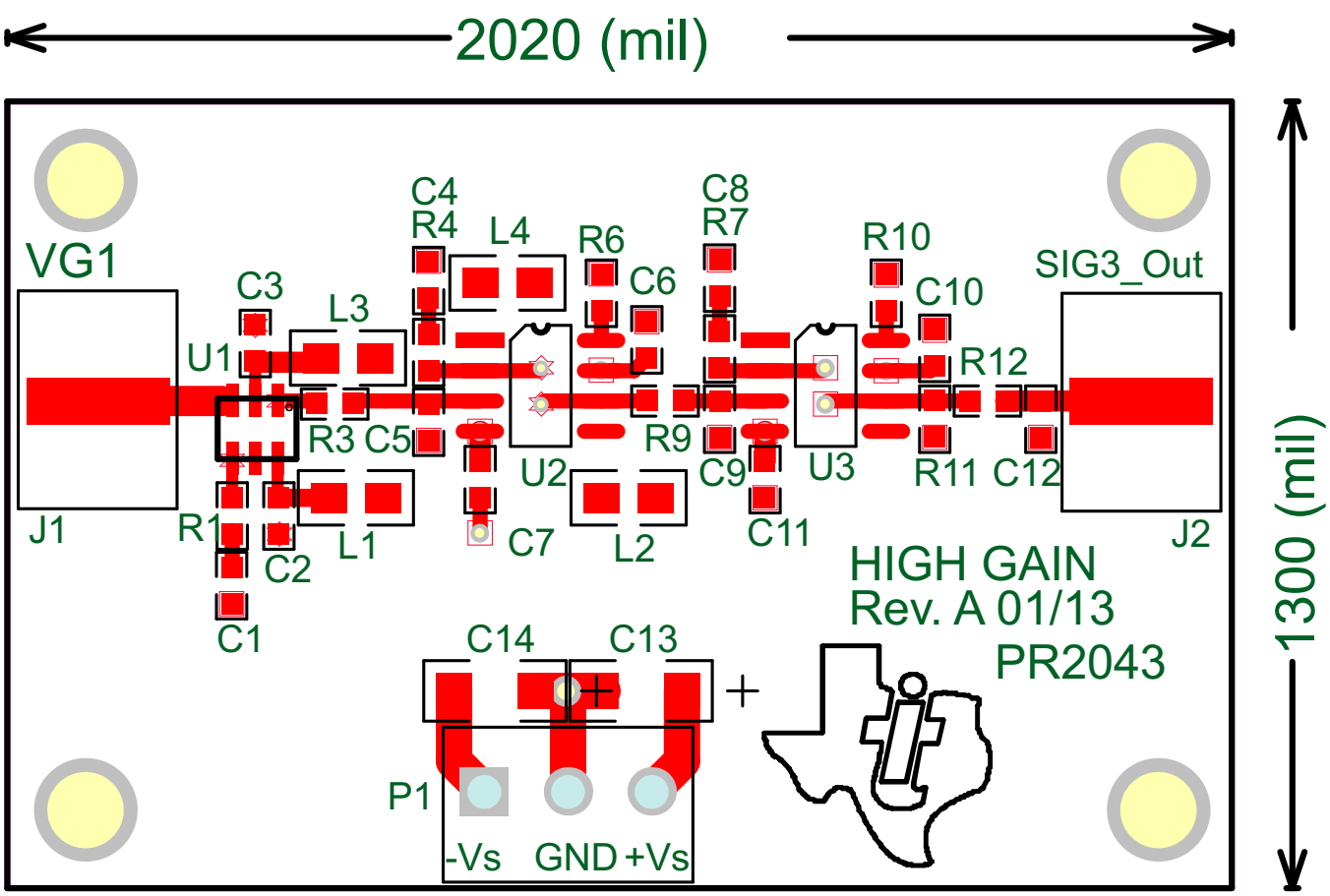

Figure 7. Top Layer

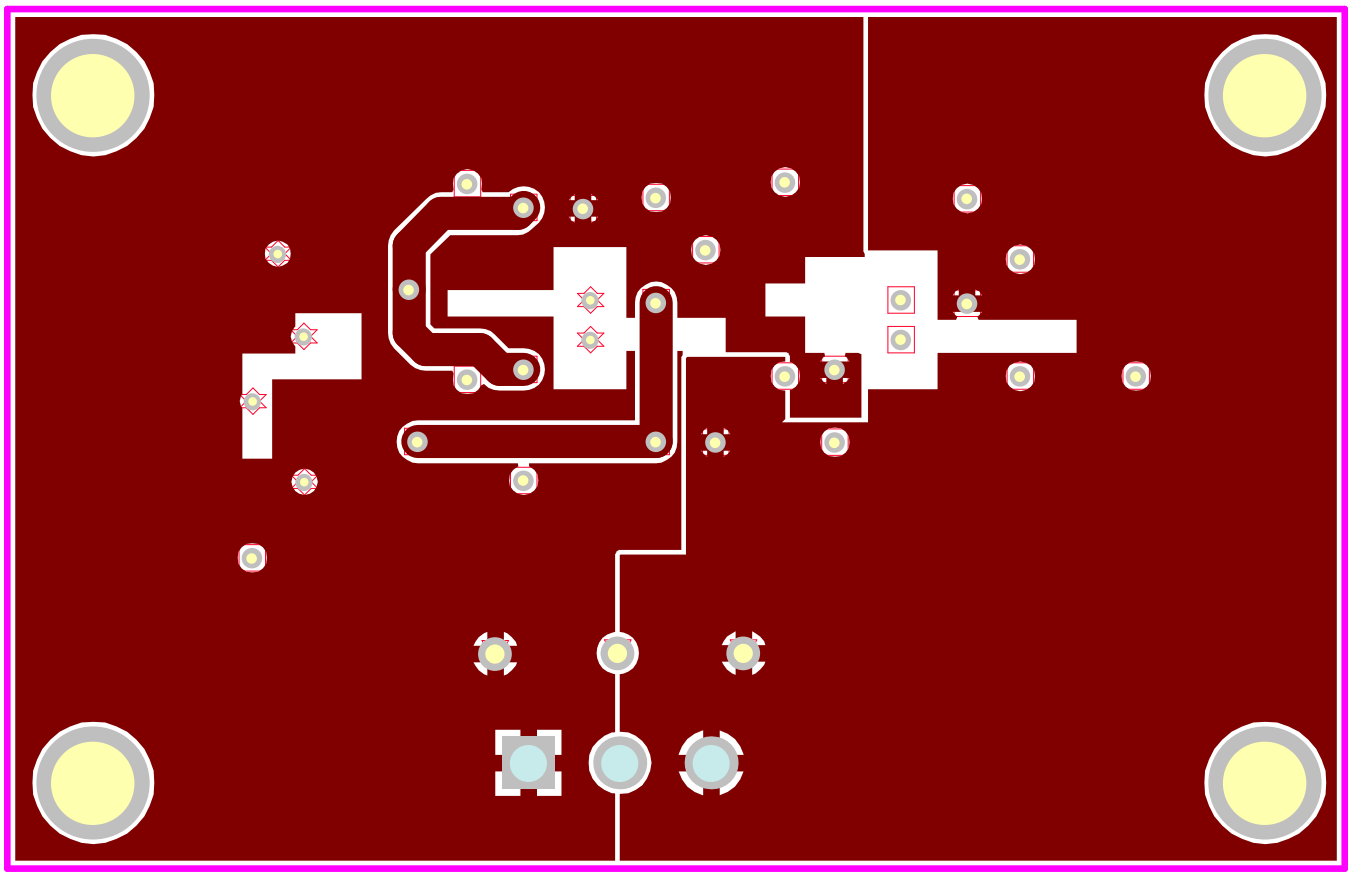

Figure 8. Middle Layer

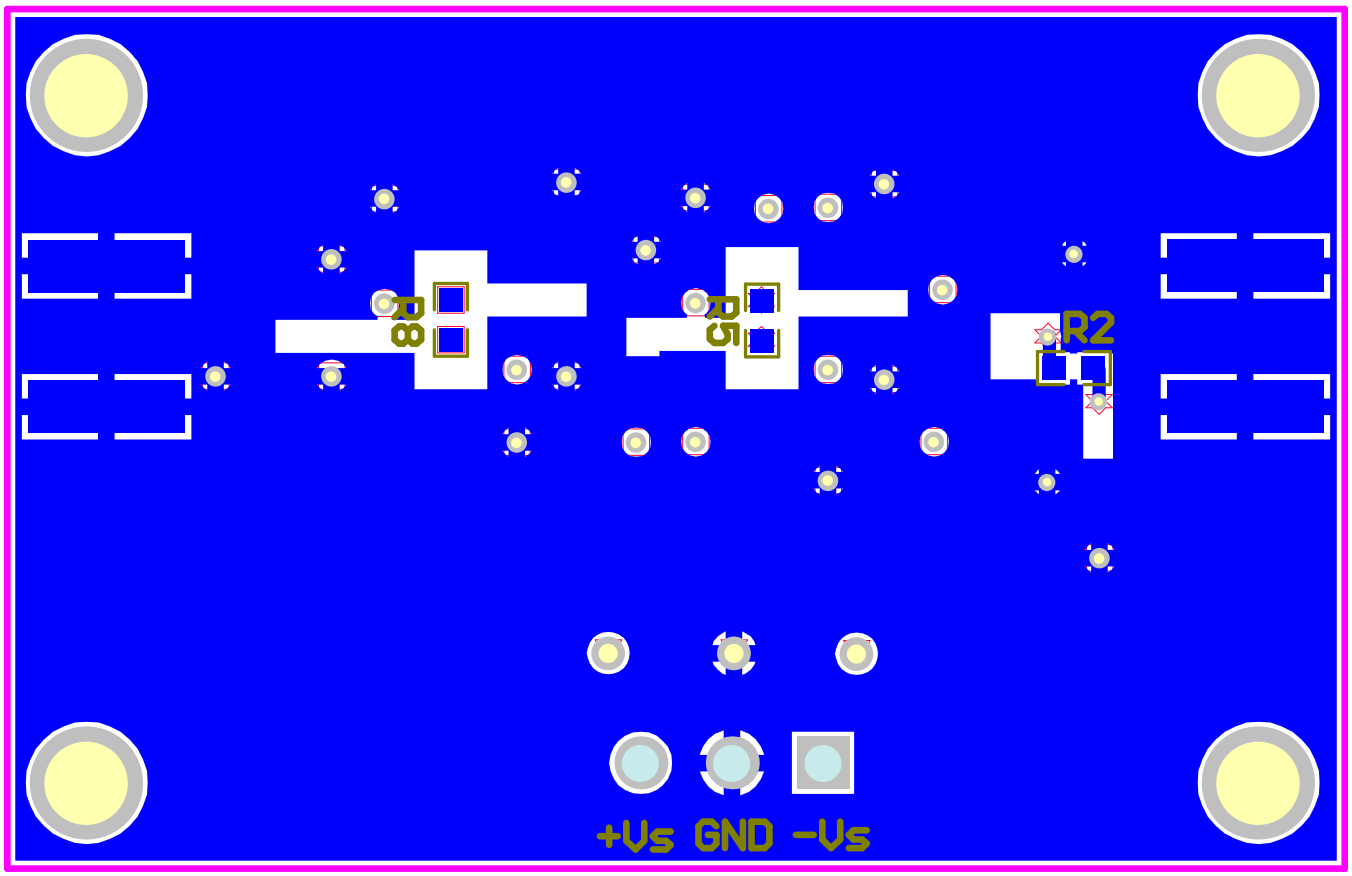

Figure 9. Bottom Layer (Inverted)

In order to minimize stray capacitance in this layout, no plane was present on the inverting input pins of any amplifier, or at the output. The OPA684, a current feedback amplifier with very low output impedance on its inverting input pin, is very sensitive to stray capacitance on that node.

The evaluation was a slightly difficult because it required finding an arbitrary waveform generator (ARB) with sufficiently-low signal amplitude control and noise. A suitable ARB could not be found in the lab; therefore, a steep band-pass filter (eighth order) was connected on the ARB output followed by two 40-dB attenuation pads to achieve the desired 20-μV_{PP} signal generator.

To look at the signal, use a simple oscilloscope. Results are shown in Figure 10 and Figure 11 for 1-MHz and 5-MHz signals with a 512x averaging to extract the signal from the noise floor.

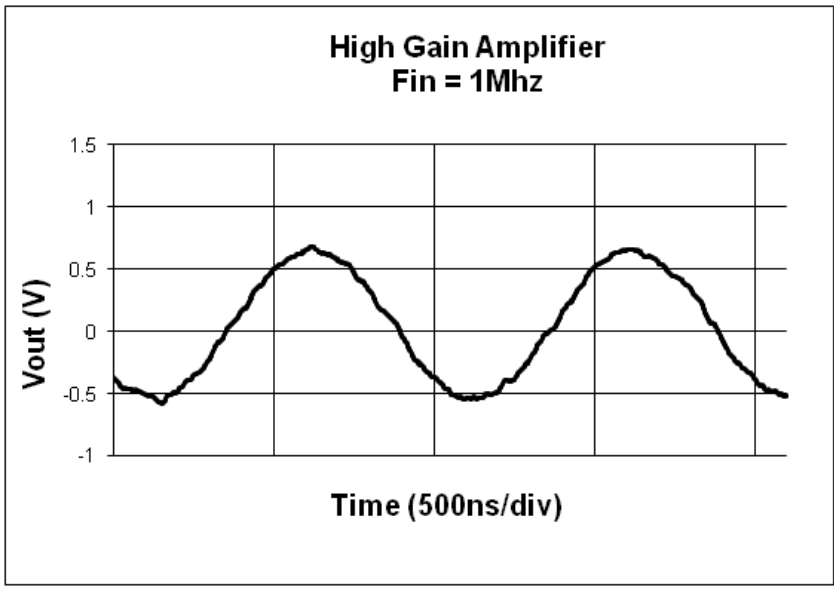

Figure 10. 1-MHz Output for a 20-μV_{PP} Input Signal

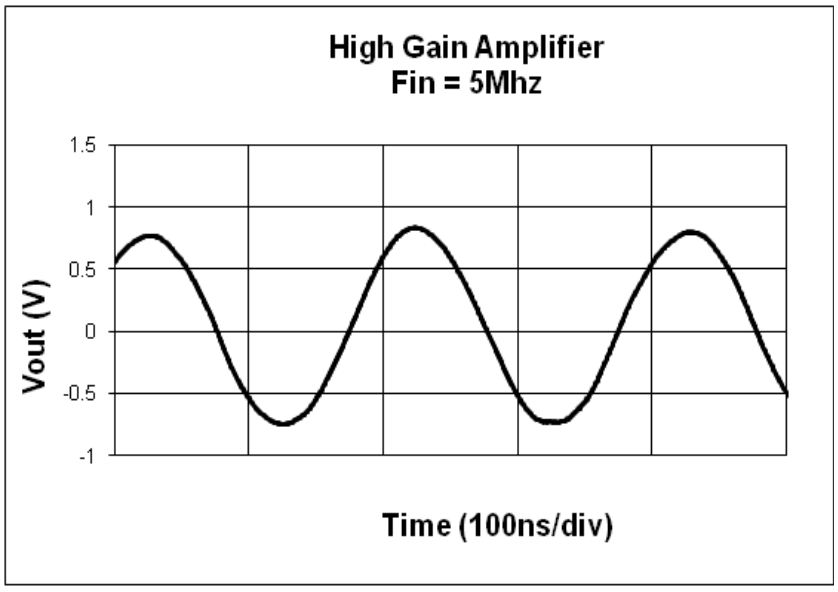

Figure 11. 5-MHz Output for a 20-μV_{PP} Input Signal

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