Measuring Board Parasitics in High-Speed Analog Design

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ABSTRACT

Successful circuit designs using high−speed amplifiers can depend upon understanding and identifying parasitic printed circuit board (PCB) components. Simulating a design while including PCB parasitics can protect against unpleasant production surprises. This application report discusses an easy method for measuring parasitic components in a prototype or final PC board design by using a standard oscilloscope and low frequency waveform generator to collect valuable information for SPICE simulation.

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1 High Speed Circuit Design

IC vendors and manufacturers frequently publish recommendations for proper PCB layout of a given IC device so that a circuit design will be more likely to enable the device to achieve its specified performance. As a circuit design is tweaked for a particular application, trouble can often appear in the form of parasitic board components. For example, the circuit shown in Figure 1 uses a 900MHz, gain of 2 amplifier; any amplifier with > 200MHz bandwidth will be very sensitive to PCB parasitics.

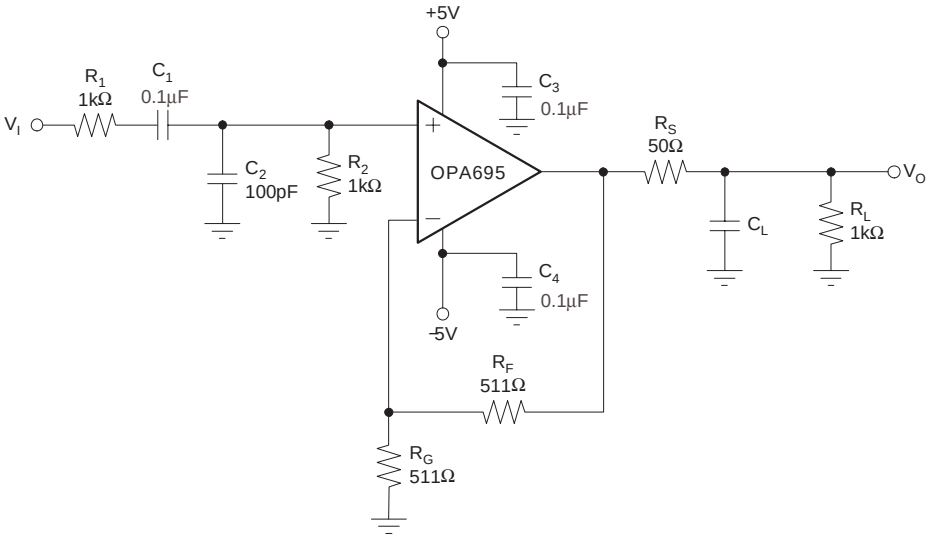

Figure 1. Example Circuit for 900MHz Frequency Amplifier, Gain 2 Stage

At first inspection, this amplifier design appears to be relatively sound. However, this circuit has multiple issues, not only in the layout of the PCB but also in the selected components' actual high frequency model. It is generally not difficult to obtain high frequency models for the component values; these models are available from the manufacturer's data sheets. They can also be measured using an impedance function found in some network analyzers. Figure 2 shows just the amplifier and the parasitic capacitance added from the printed circuit trace connecting to the inverting input of the amplifier. This slight capacitance, C_M, can have a significant effect on the amplifier's performance. The task here will be to measure the PCB trace capacitance and/or inductances that come with a high-speed layout that can affect performance.

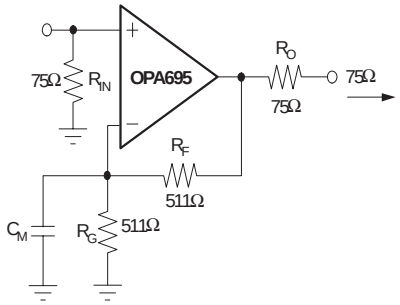

Figure 2. Example Circuit for 900MHz, Gain = 2, Video Line Driver, with Parasitic Inverting Node Capacitance

It can be very difficult to extract the correct parasitic components at high frequency from a PCB. This iterative process can involve many hours of careful measurements. High-speed amplifiers are considerably more sensitive to the parasitic capacitance found at the I/O pins. Excess capacitance at the inverting node of a current feedback amplifier, for instance, results in the ringing of the amplifier output. This effect can be seen in the time-domain plot of Figure 3, where three different layout parasitic C_M values are assumed in the simulation of Figure 2.

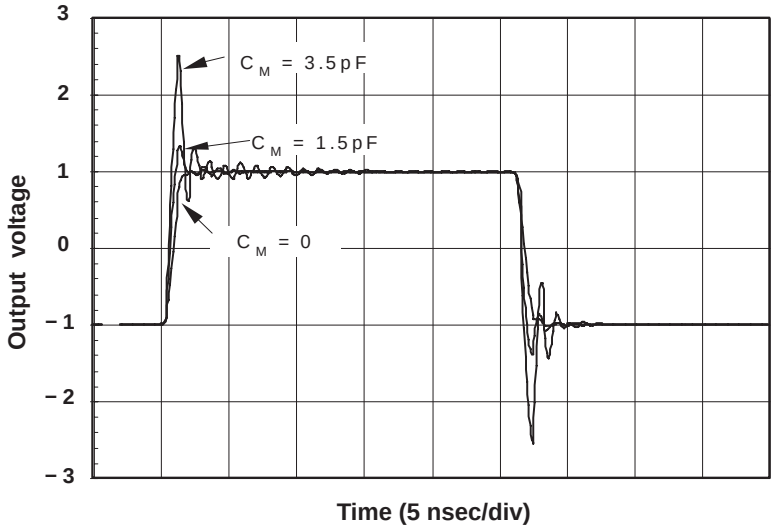

Figure 3. Time-Domain Plot for Current Feedback Amplifier

2 Determining the Source of the Capacitance

Regardless of whether or not one is an experienced engineer, it is easy to overlook these parasitics for high-speed current feedback op amps (CFA) or voltage feedback op amps (VFA). Adding parasitic capacitance in parallel with the low resistor values (Rg) will produce undesirable results. When capacitance is in parallel to the Rf (feedback resistor), then one questions why the full bandwidth was not obtained. How then does the engineer or designer determine parasitic capacitance and its influence on the final board design? By measuring the capacitance and including this data in the simulation circuits.

As a typical example, Figure 2 is an OPA695 high-bandwidth amplifier, at a gain of 2, which uses a feedback resistor (Rf) of 511Ω and gain setting resistor (R_g) of less than or equal to 511Ω. Adding a few pF in the wrong place (as shown in Fig. 2) will generate widely variant results when one is trying to obtain fast settling for an A/D, D/A or video line driver application.

The initial circuit analysis most likely did not account for any parasitic capacitance due to the board layout. These values frequently change from the prototype layout to the eventual final design. By using some simple circuit theory, one can develop a straightforward measurement system to determine this capacitance or inductance.

3 Capacitive and Inductive Measurement Techniques

A very easy way to measure layout capacitance and inductance is to use large signal triangle waves as a test waveform. The first step in this process is to isolate the parasitic capacitance, as shown in Figure 4. From this simple circuit, one can define an extraction technique for the unknown parasitic in the circuit, C_M.

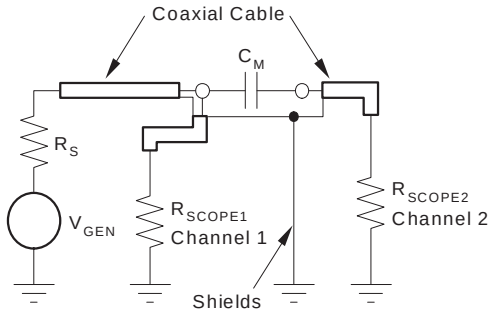

Figure 4. Capacitance Test Measurement Circuit Using an HP8116A Function Generator

In this example, an HP8116A function generator (Vgen) is connected as shown in Figure 4. The center conductor of two coaxial cables is soldered to the PCB trace and sense line into Channel Two to ground (or other planes/traces of interest). The shields are tied together as shown in Figure 4. The two measurement cables are connected to Channel One and Two of the oscilloscope, set to show an input 50Ω termination (R_{scope1}, R_{scope2}).

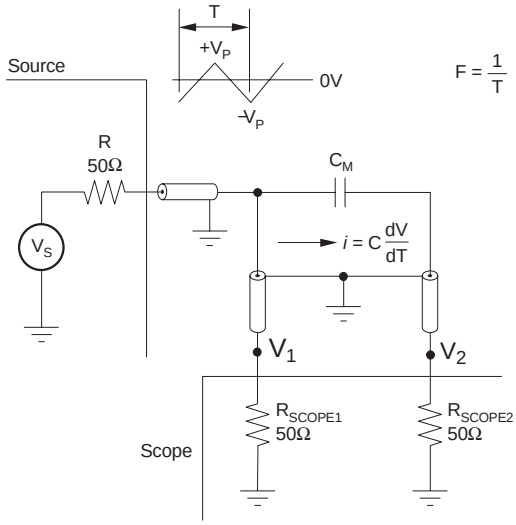

Figure 5. Computing V_2 for Triangle Wave V_1

Looking at the analysis circuit of Figure 5, and recognizing that V_1 is a triangle wave, we can easily compute the current through the unknown capacitance as simply:

$$i = C\frac{dV}{dt} \tag{1}$$

The total dV/dT for the triangle wave is twice the slope on each one half-cycle if peak-to-peak values are used for analysis. For a triangle wave of total period *T*, the dV/dT is easily derived as:

$$\frac{dV}{dT} = \frac{2 \cdot V_{1_{pp}}}{\frac{T}{2}} = V_{1_{pp}} \cdot F \cdot 4 \tag{2}$$

Since it is only the current due to this dV/dT at V_1 that gets through the unknown parasitic capacitance to the termination resistor (the other 50Ω scope input), the measured voltage at this second scope input will be

$$V_{2_{pp}} = (50\Omega)C\frac{dV}{dT} = (50\Omega)C \cdot V_{1_{pp}} \cdot F \cdot 4 \tag{3}$$

This can be solved to give an expression for the unknown C as an equation based on the ratio of the peak-to-peak voltages at measurement points V_1 and V_2.

$$C_M = \frac{V_{2_{pp}}}{V_{1_{pp}}} \cdot \frac{1}{4(50\Omega)F} \tag{4}$$

For example, using a 2Vpp triangle wave at 10MHz to measure the parasitic capacitor on the inverting node of a manufacturer−supplied demo board showed the waveforms of Figure 6.

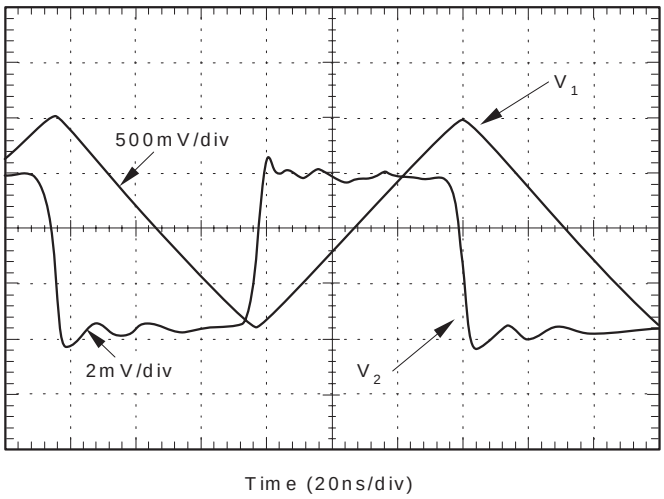

Figure 6. Oscilloscope Graph Showing 2V Ramp and Output Square Wave

Plugging this data into Equation 4 gives:

$$C_M = \frac{5.8mV}{1.9V} \cdot \frac{1}{4(50\Omega)F} \tag{5}$$

$$or \quad C_M = 1.5pF \quad \text{(with F = 10MHz)} \tag{6}$$

A similar technique may be used to estimate the trace inductance where we must now generate a dI/dT times an unknown L to produce a voltage. Figure 7 shows the measurement circuit used. Here, the source drives a triangle wave current into what looks very much like a dead short, while the scope input is set up to measure the small voltage produced by the two voltage components. In this case, there will be both an IR component due the small trace resistance (R_M) and an L*dI/dT term due to the trace inductance (L_M).

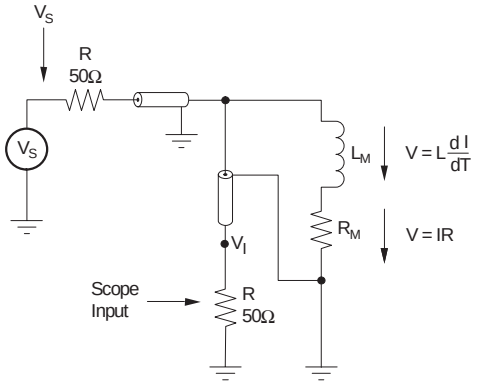

Figure 7. Measuring a Parasitic Trace Inductance

Figure 8 shows the resulting waveform that will be seen at V_1. The large step in voltage (V_{Lpp}) may be attributed to the shift from a positive dI/dT to a negative dI/dT at the triangle peaks. The small ramp will be due to the resistance element over each half−cycle of ramping current into the trace under test. The current into the trace can be estimated very nearly as simply the source voltage (V_S) divided by its 50Ω output impedance. The 50Ω measurement path into the scope does not enter into the equations because it is essentially shunted by a much lower impedance. It is critical here to use the correct value for the stimulus V_{Spp}. For instance, programming the HP8116 to a produce a 5Vpp output is actually producing a 10Vpp stimulus for the purposes of Figure 8.

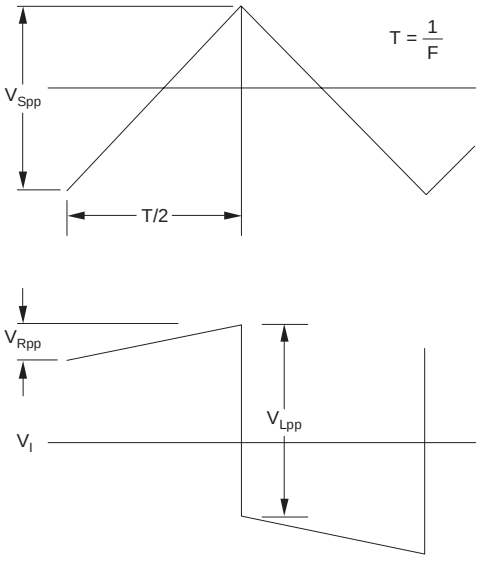

Figure 8. Stimulus and Response Waveforms for Parasitic Inductance Test

Each triangle half-cycle produces a

$$\frac{V_{S_{pp}}}{R} = I_{test} \tag{7}$$

ramp into the trace under test. Over a half-cycle, this dI/dT will be V_{Spp}/(R*T/2). At each peak in the stimulus triangle wave, the slope changes polarity, giving us double the dI/dT to produce the V_{Lpp} step in Figure 8. That step is then given by:

$$V_{L_{pp}} = \frac{L_m \cdot 2 \cdot V_{S_{pp}}}{\frac{R \cdot T}{2}} = \frac{L_m \cdot 4 \cdot V_{S_{pp}}}{R \cdot T} = \frac{L_m \cdot 4 \cdot F \cdot V_{S_{pp}}}{R} \tag{8}$$

Solving for Lm,

$$L_M = \frac{V_{I_{pp}} \cdot R}{4 \cdot V_{S_{pp}} \cdot F} \tag{9}$$

The total change in current over one half-cycle will produce the resistive part of the response waveform in Figure 8.

$$V_{R_{pp}} = \frac{V_{S_{pp}}}{R} \cdot R_m \tag{10}$$

Solving for Rm,

$$R_m = R \cdot \frac{V_{R_{pp}}}{V_{S_{pp}}} \tag{11}$$

4 Measurement Notes and Aids

To keep the cable capacitances from interacting with this measurement technique, relatively low frequencies (<10MHz, and preferably < 2MHz) but high amplitudes are used. The resulting measured voltages, however, can be quite small. Using a very high gain bandwidth, low noise, high DC precision scope preamp can improve measurement accuracy when very low capacitances or inductances are being measured. Figures 9 and 10 show an excellent choice for this scope preamp, where they differ only in how DC bias current cancellation is achieved given the different source impedances of the capacitive or inductive tests. The 50Ω resistor shown in Figure 5 as R_{scope2} and R in Figure 7 becomes the input termination 50Ω in Figures 9 and 10.

The OPA847, used in this example preamp, provides 3.9GHz gain bandwidth product with < 0.9nV√ Hz input noise voltage and exceptional DC accuracy. At the very high gains shown in Figures 9 and 10 (201V/V for the amplifier), the bandwidth will be reduced to approximately 18MHz. With stimulus triangle waves of < 2MHz frequency, this should be adequate to pass enough harmonics of the response to measure the desired voltage steps. To limit noise on the scope waveform, using its 20MHz bandwidth option is also recommended. The preamp of Figure 9 would be inserted at V_2 in Figure 5, while the preamp of Figure 10 would be inserted at V_1 in Figure 7.

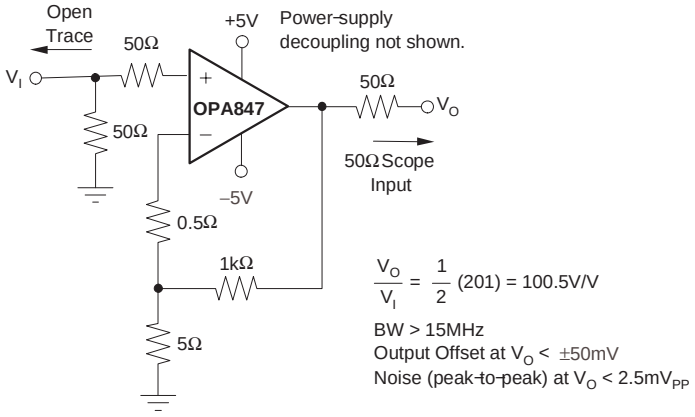

Figure 9. Scope Preamp for Capacitance Measurement

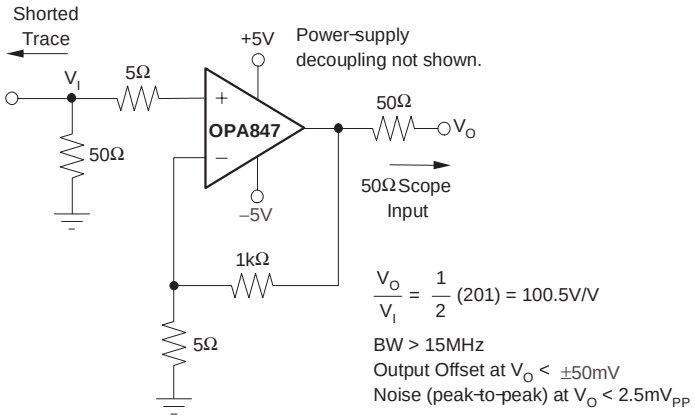

Figure 10. Scope Preamp for Inductance Measurement

References

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