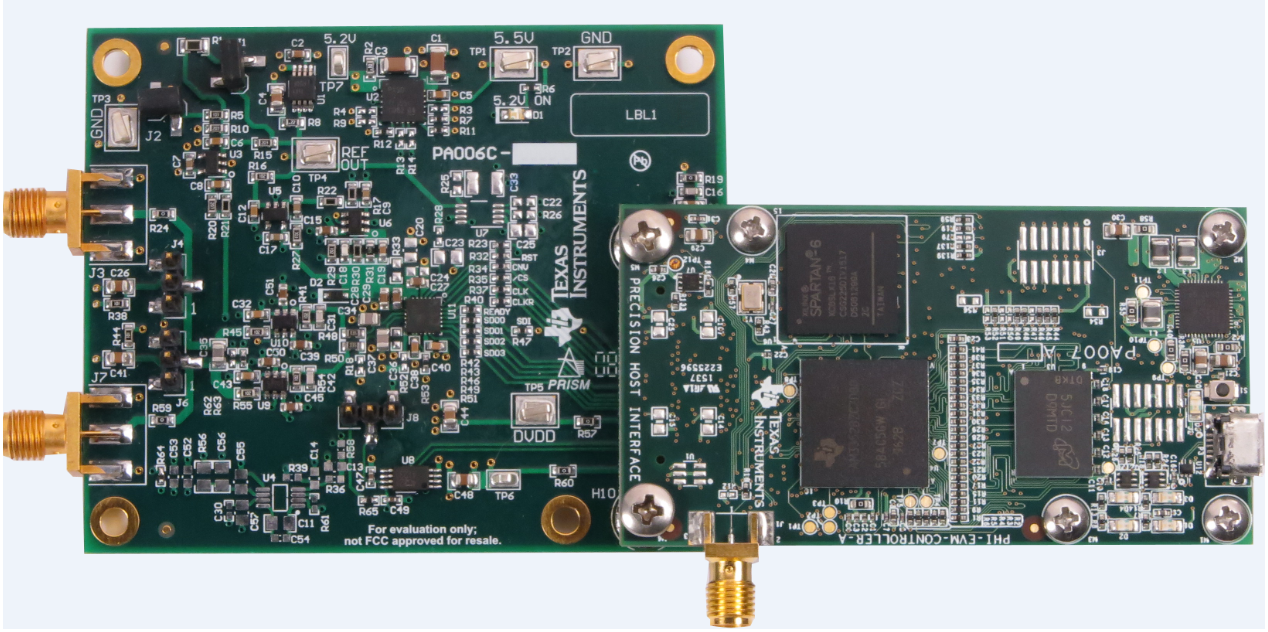
ADS9120EVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS9120 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS9120, which is an 16-bit, 2.5-MSPS, fully-differential input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an enhanced serial multiSPI® digital interface. The EVM-PDK eases the evaluation of the ADS9120 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.



The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS9120	SBAS710
OPA625	SBOS688
OPA376	SBOS406
OPA378	SBOS417
REF5050	SBOS410
TPS7A4700	SBVS204

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1 Overview

The ADS9120EVM-PDK is a platform for evaluating the performance of the ADS9120 SAR ADC, which is a fully-differential input, 16-bit, 2.5-MSPS device. The evaluation kit includes the ADS9120EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS9120EVM board includes the ADS9120 SAR ADC, all the peripheral analog circuits, and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS9120EVM
- Supplies power to all active circuitry on the ADS9120 board

Along with the ADS9120EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS9120EVM-PDK Features

The ADS9120EVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS9120 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS9120 ADC over a USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, Windows® 8, 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS9120EVM Features

The ADS9120EVM includes the following features:

- Onboard low-noise and low distortion ADC input drivers optimized to meet ADC performance
- Onboard precision 5.0-V voltage reference filtered and followed by a low-noise, low-offset and low-impedance buffer. The reference driver circuit is optimized for 1-LSB voltage regulation under maximum loading conditions at full device throughput of 2.5 MSPS.
- Jumper-selectable 0-V and 2.5-V input common-mode options allow unipolar and bipolar inputs.
- Onboard ultralow noise low-dropout (LDO) regulator for excellent 5.2-V single-supply regulation of all operation amplifiers and voltage reference.

2 Analog Interface

As an analog interface, the evaluation board uses operational amplifiers in a variety of configurations to drive the ADS9120 input signal and reference inputs. This section covers driver details including jumper configuration for different input signal common modes and board connectors for a differential signal source.

2.1 Connectors for Differential Signal Source

The ADS9120EVM is designed for easy interfacing to an external analog differential source via a subminiature version A (SMA) connector or 100-mil headers. J7 and J3 are SMA connectors that allow analog source connectivity through coaxial cables. Also, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to the J4:2 and J6:2 pins.

NOTE: The input does not support single-ended signals. The external source must be differential or balanced keeping the negative and positive inputs to the board symmetric such that Vs(+) = –Vs(–) at any given time.

Table 1. J7 and J3 SMA Connectors Description

Pin Number	Signal	Description
J3	Vs(–)	Negative differential board input, 1-kΩ input impedance
J7	Vs(+)	Positive differential board input, 1-kΩ input impedance

Table 2. J4 and J6 Headers Description

Pin Number	Signal	Description
J4:3	TEST 0.23 V	Do not use: diagnostic use only
J4:2	Vs(–)	Negative differential board input, 1-kΩ input impedance
J4:1	AGND	Analog ground
J6:3	AGND	Analog ground
J6:2	Vs(+)	Positive differential board input, 1-kΩ input impedance
J6:1	TEST 4.77 V	Do not use: diagnostic use only

2.2 ADC Differential Input Signal Driver

The differential signal inputs of the ADS9120 are not dynamically high impedance. SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed that effectively make the ADC inputs dynamically low impedance. Thus, the evaluation board has low impedance on board drivers that maintain ADC performance with maximum loading at the full device throughput of 2.5-MSPS for signal.

2.2.1 Input Signal Path

Figure 1 shows the signal path for the differential signal applied at the board inputs. The board input impedance is 1-kΩ with 10-nF differential filtering that keeps noise in external cabling common. The overall signal path bandwidth is limited to 160-kHz by the anti-aliasing filter formed from 1-kΩ resistor and 1-nF capacitor at the amplifier feedback. Finally, the two OPA625 operational amplifiers drive the ADS9120 differential inputs with 2.2-Ω impedance up to 7-MHz that properly drives the low dynamic impedance of the ADC inputs at 2.5-MSPS.

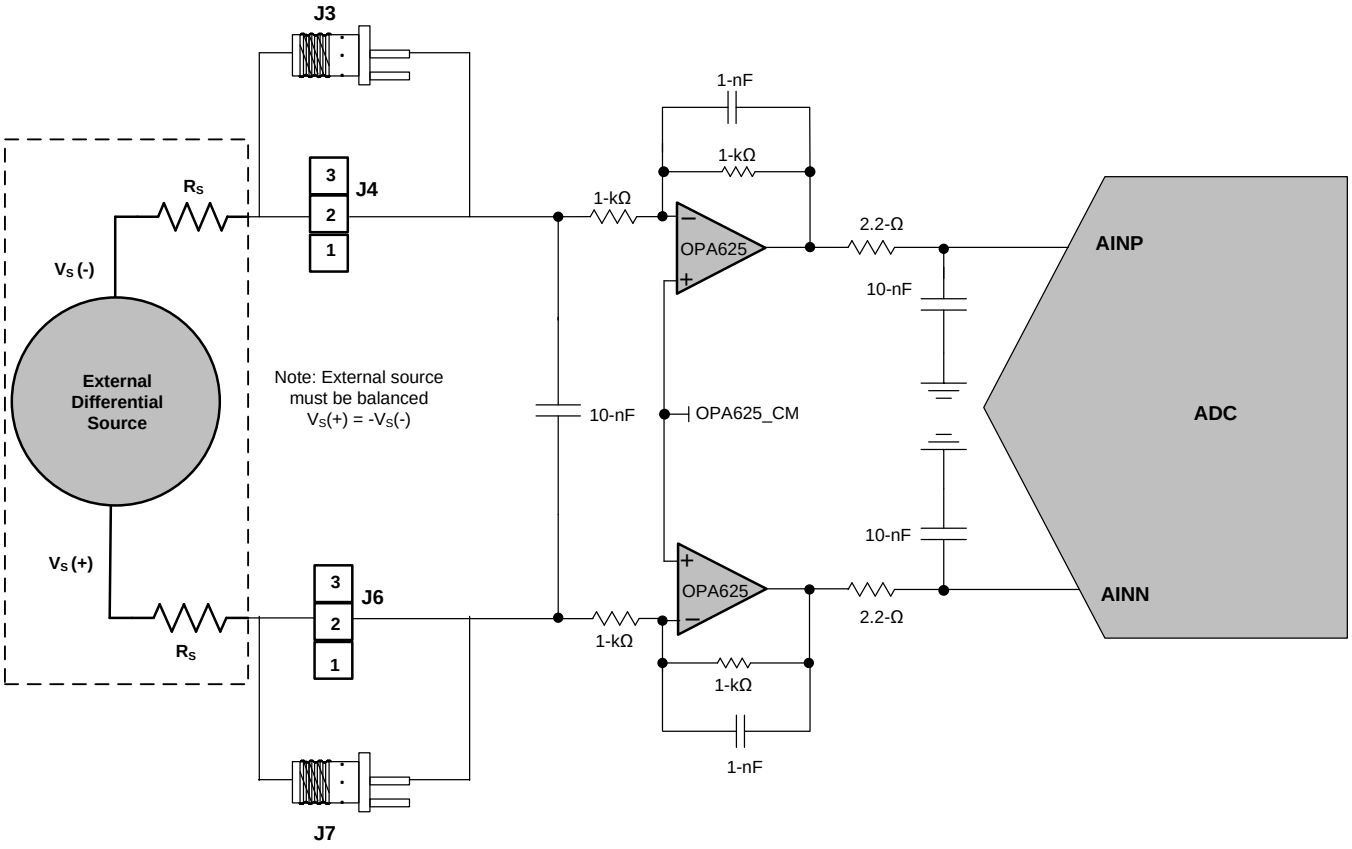

Figure 1. OPA625 Differential Input Driving Path

2.2.2 Input Common-Mode Jumper Configuration

The ADS9120EVM board accommodates three external source common-mode options: 0 V, 2.5 V, and floating with jumpers J1 and J2; see Figure 2 and Table 3.

J2 selects the OPA625 common-mode as 2.5 V (J2:OPEN) or 1.25 V (J2:CLOSED). J1 increases the OPA625 common-mode by almost 100 mV to avoid amplifier output saturation with full-scale external source signal amplitude. R1 is installed as 280 kΩ, allowing full-scale external source signals for external source impedance (R_S) between 0 Ω and 32 Ω, with 0-V common mode. R1 must be changed to compensate for larger external source impedance (R_S) values or for 2.5-V external source common-mode, as explained in Section 2.2.3.

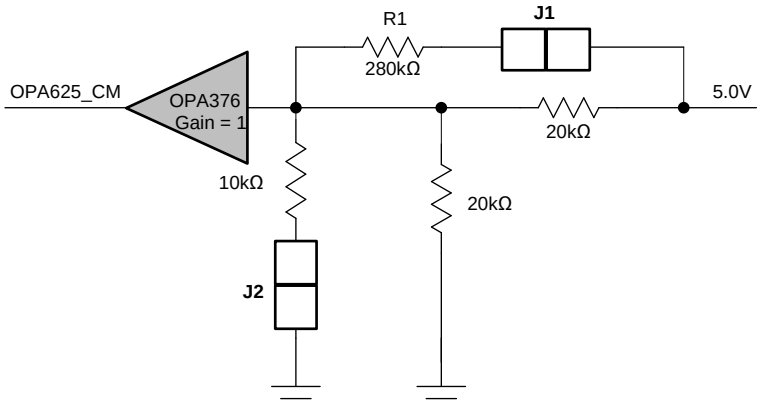

Figure 2. Common-Mode Selection Jumpers

Table 3. J1 and J2 Configuration per Input Common-Mode

J1 Setting (R1 Comp)	J2 Setting	External Signal Common-Mode	Differential Source Type
CLOSED	CLOSED	0 V	Bipolar: If R1 = 280 kΩ, R_S range is 0 Ω to 32 Ω
CLOSED	OPEN	2.5 V	Unipolar: must change R1 to match R_S
CLOSED	OPEN	Floating	AC-coupled bipolar: If R1 = 280 kΩ, no R_S restriction

2.2.3 R1 Setting vs Source Impedance

The external source impedance (R_S) adds up to the 1 kΩ of the input resistor, thereby moving the output common-mode of the OPA625 amplifiers. To compensate for this change in output common-mode, R1 can be modified according to the particular external source impedance value used with the evaluation board to allow full-scale input range without saturating the OPA625 amplifiers.

The board is shipped with R1 as 280 kΩ that allows an external source impedance (R_S) range between 0 Ω to 32 Ω for a 0-V common-mode configuration (J1:closed and J2:closed). For floating or ac-coupled signals, the input common-mode is set by the OPA625 amplifiers themselves and R1 must remain at 280 kΩ for any given source impedance. The ADC common-mode for 0-V input common-mode setting is calculated using Equation 1.

$$\mathrm{ADC\_V_{CM}} = \frac{5 \times (10\mathrm{k\Omega} // 20\mathrm{k\Omega})}{(10\mathrm{k\Omega} // 20\mathrm{k\Omega}) + (\mathrm{R_1} // 20\mathrm{k\Omega})} \times \left(1 + \frac{1\mathrm{k\Omega}}{1\mathrm{k\Omega} + \mathrm{R_S}}\right) \quad (1)$$

In the case of unipolar input signals with a 2.5-V common-mode, the ADC common-mode is calculated using Equation 2.

$$\mathrm{ADC\_V_{CM}} = \frac{5 \times 20\mathrm{k\Omega}}{20\mathrm{k\Omega} + (\mathrm{R_1} // 20\mathrm{k\Omega})} \times \left(1 + \frac{1\mathrm{k\Omega}}{1\mathrm{k\Omega} + \mathrm{R_S}}\right) - \left(\frac{2.5 \times 1\mathrm{k\Omega}}{1\mathrm{k\Omega} + \mathrm{R_S}}\right) \quad (2)$$

For Equation 1 and Equation 2 the value of R1 must be calculated to satisfy Equation 3:

$$2.5\ \mathrm{V} \le \mathrm{ADC\_V_{CM}} \le 2.6\ \mathrm{V} \quad (3)$$

2.3 Onboard ADC Reference

The EVM does not include a provision for driving the reference input of the ADS9120 from an external source. The reference input signal path is entirely self-contained on the ADS9120EVM and consists of the REF5050, a 5.0-V precision voltage reference. The output of the REF5050 is filtered and buffered by a reference driver formed from two amplifiers: the OPA625 and OPA378. This reference driver offers zero-offset, low-noise and is optimized for a 1-LSB voltage regulation under maximum loading conditions at full device throughput of 2.5-MSPS. The schematic for the reference driver circuit is shown in Figure 3.

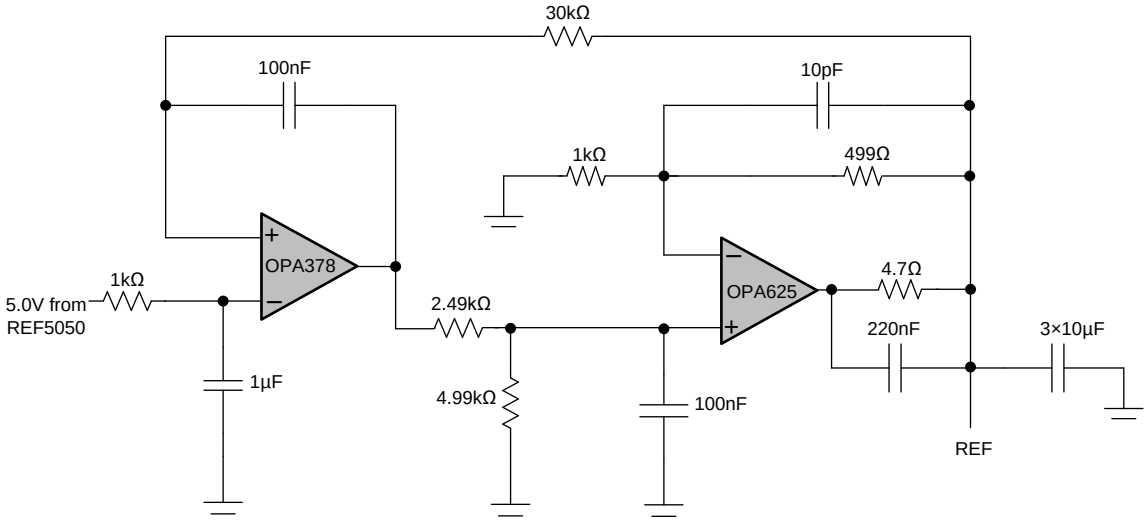

Figure 3. Onboard Reference Signal Path

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS9120 ADC (over SPI or multiSPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS9120EVM-PDK platform. Once the hardware is initialized, the EEPROM is no longer used.

3.1 multiSPI® for ADC Digital IO

The ADS9120EVM-PDK supports all the interface modes as detailed in the ADS9120 datasheet (SBAS710). In addition to the standard SPI modes, (with single-, dual- and quad-SDO lanes), the multiSPI modes support single- and dual-data output rates and the four possible clock source settings as well. The PHI is capable of operating at a 1.8-V logic level and is directly connected to the digital I/O lines of the ADC.

4 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the computer's USB supply.

The EEPROM on the ADS9120EVM use a 3.3-V power supply generated directly by the PHI. The ADC and analog input drive circuits are powered by the TPS7A4700 onboard the EVM, which is a low-noise linear regulator that uses the 5.5-V supply out of a switching regulator on the PHI to generate a much cleaner 5.2-V output. The 1.8-V supply to the digital section of the ADC is provided directly by an LDO on the PHI.

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas where possible between bypass capacitors and their loads to minimize inductance along the load current path.

5 ADS9120EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS9120EVM-PDK.

5.1 Default Jumper Settings

Jumper settings are determined by common mode and source impedance of the external source that provides a differential signal to the board. Remove shunts from J4 and J6 and set J2 and J1 according to the external source as described in Section 2.

5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS9120 and run the GUI installer to install the EVM GUI software on the user's computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message such as the one in Figure 4 may appear or the *installer.exe* file may be deleted.

Accept the license agreements and follow the on-screen instructions to complete the installation.

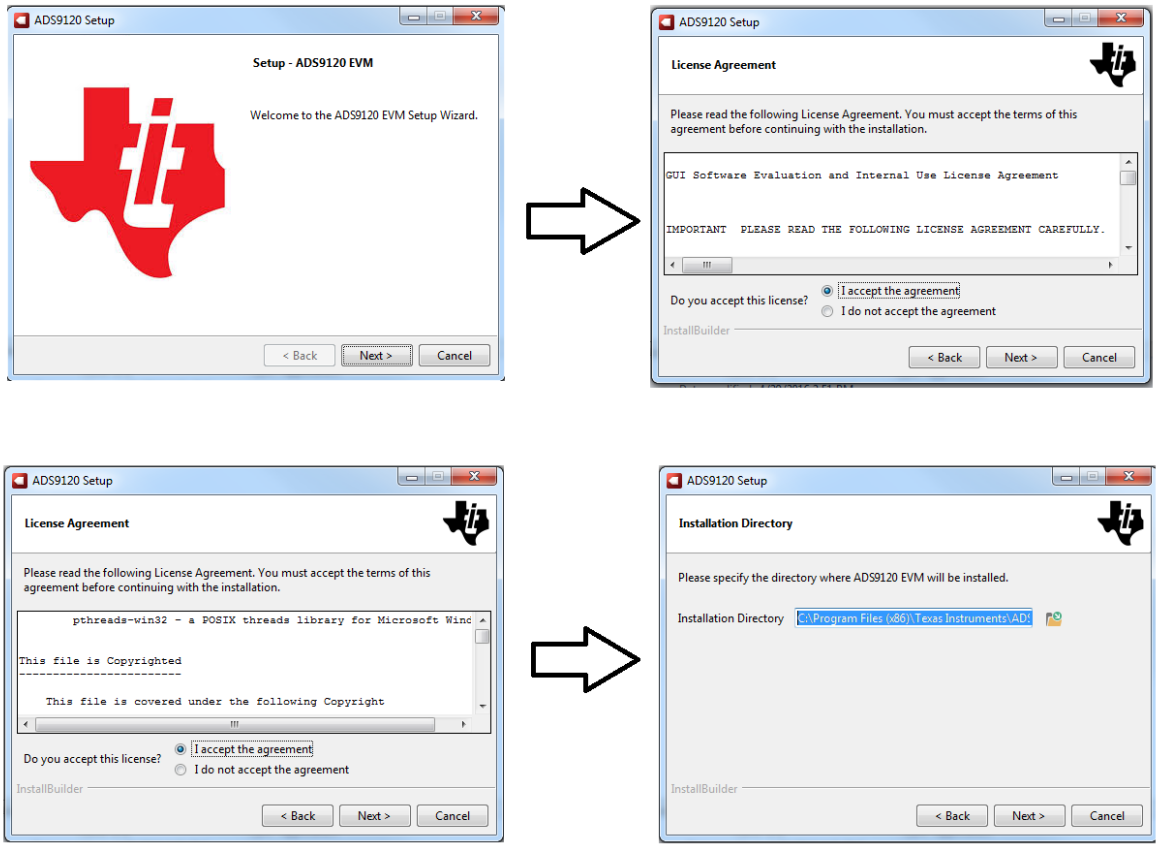

Figure 4. ADS9120 Software Installation Prompts

As a part of the ADS9120EVM GUI installation, a prompt with a *Device Driver Installation* will appear on the screen. Click *Next* to proceed.

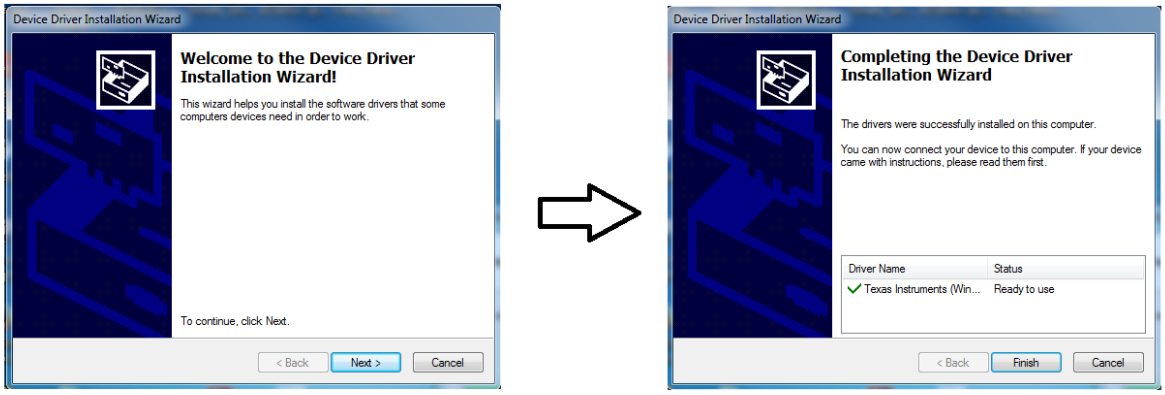

Figure 5. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS9120EVM-PDK requires LabVIEW™ Run-Time Engine may prompt for the installation of this software, if not already installed.

Figure 6. LabVIEW Run-Time Engine Installation

After these installations, verify that C:\Program Files (x86)\Texas Instruments\ADS9120EVM is as shown in Figure 7.

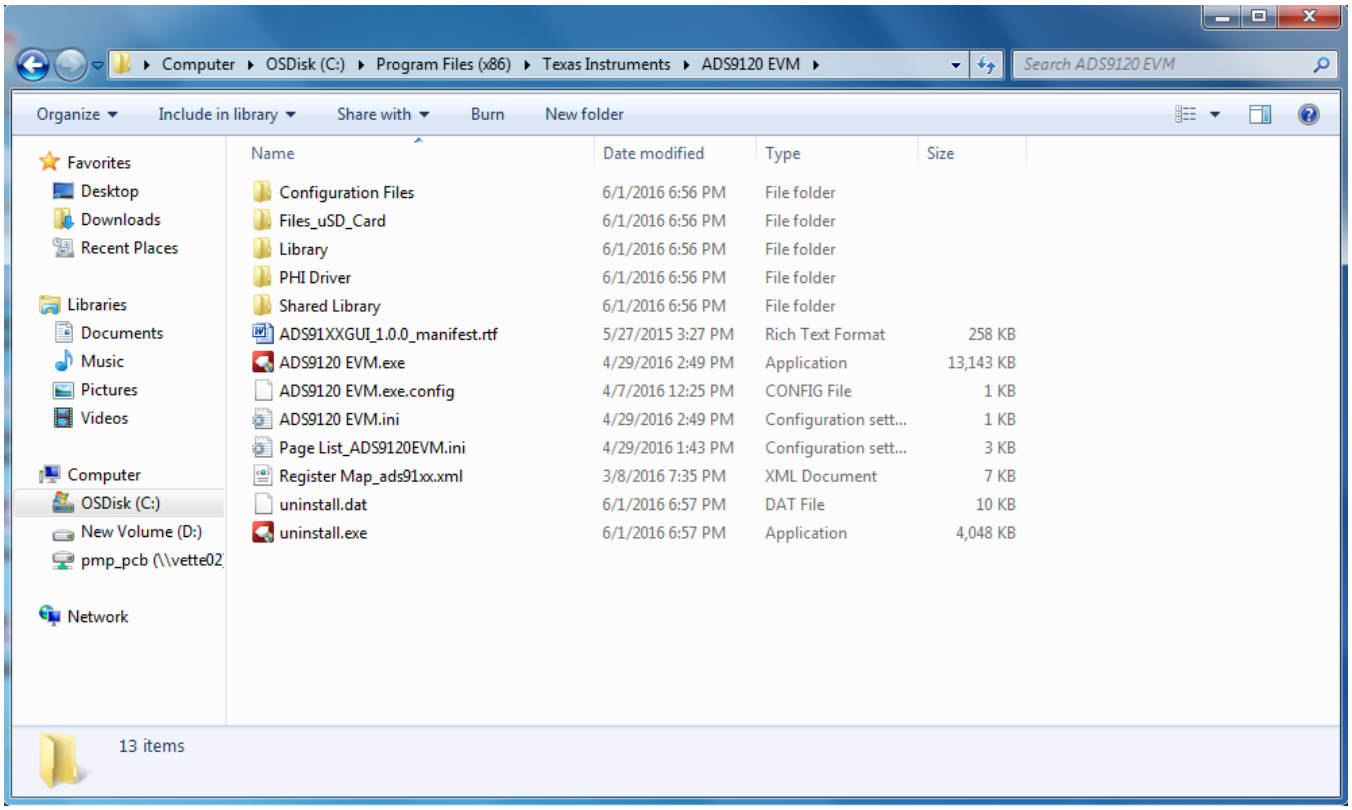

Figure 7. ADS9120EVM Folder Post-Installation

6 ADS9120EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the ADS9120EVM-PDK to the computer and evaluating the performance of the ADS9120:

1. Connect the ADS9120EVM to the PHI. Install the two screws as indicated in Figure 8.
2. Use the USB cable provided to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI starts blinking to indicate that the PHI is booted up and communicating with the PC. The resulting LED indicators are shown in Figure 8.

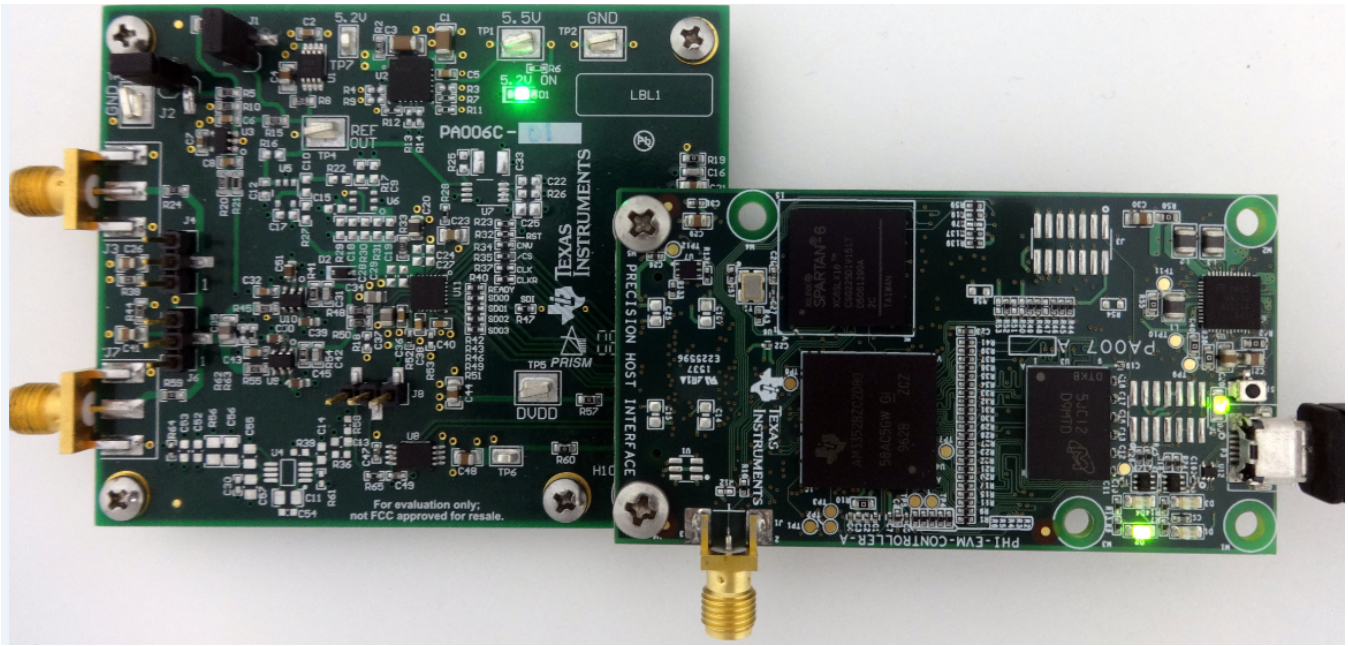

Figure 8. EVM-PDK Hardware Setup and LED Indicators

3. Launch the ADS9120EVM GUI software, as shown in Figure 9.

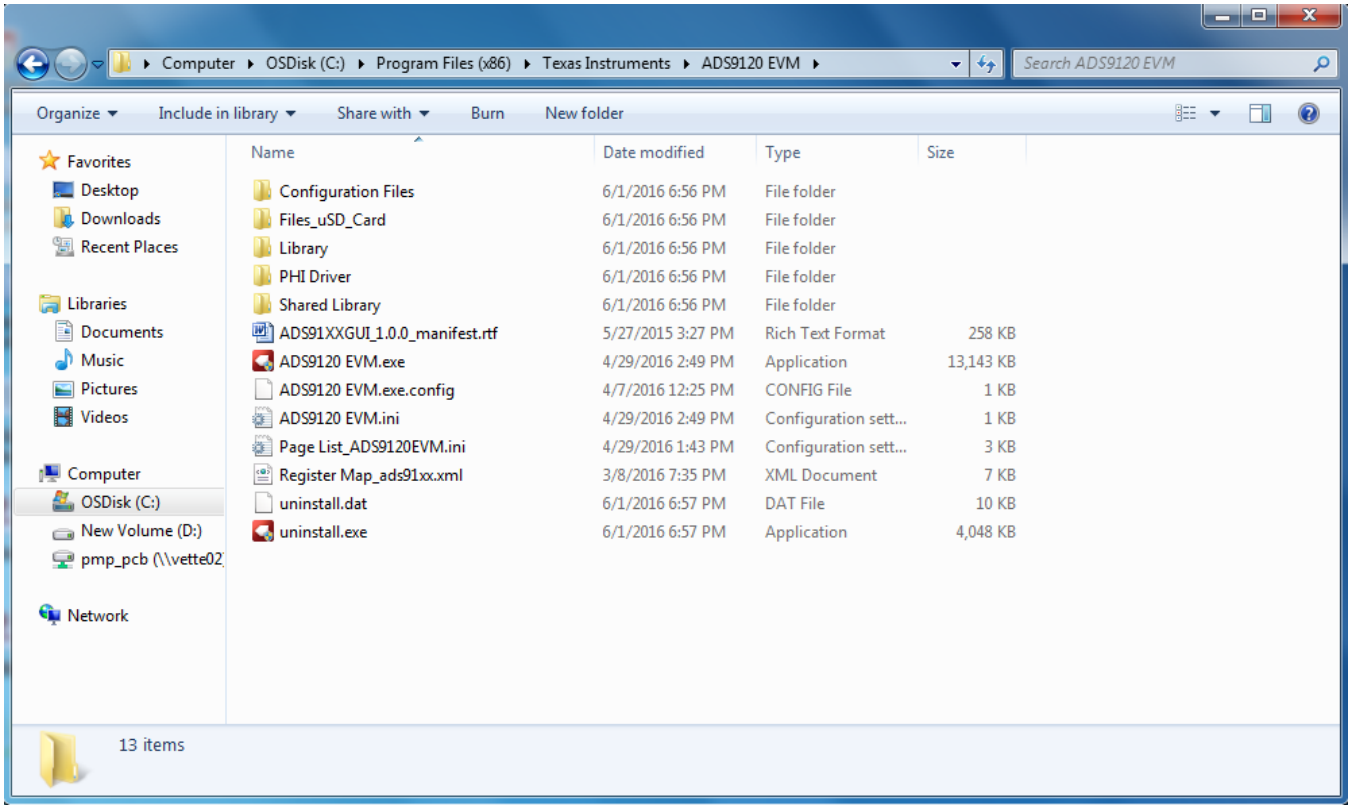

Figure 9. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over virtually all functions of the ADS9120 including interface modes, sampling rate, and number of samples to be captured.

Figure 10 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the ADS9120 can be exercised. These settings are global because they persist across the GUI tools listed in the top left pane (or from one page to another).

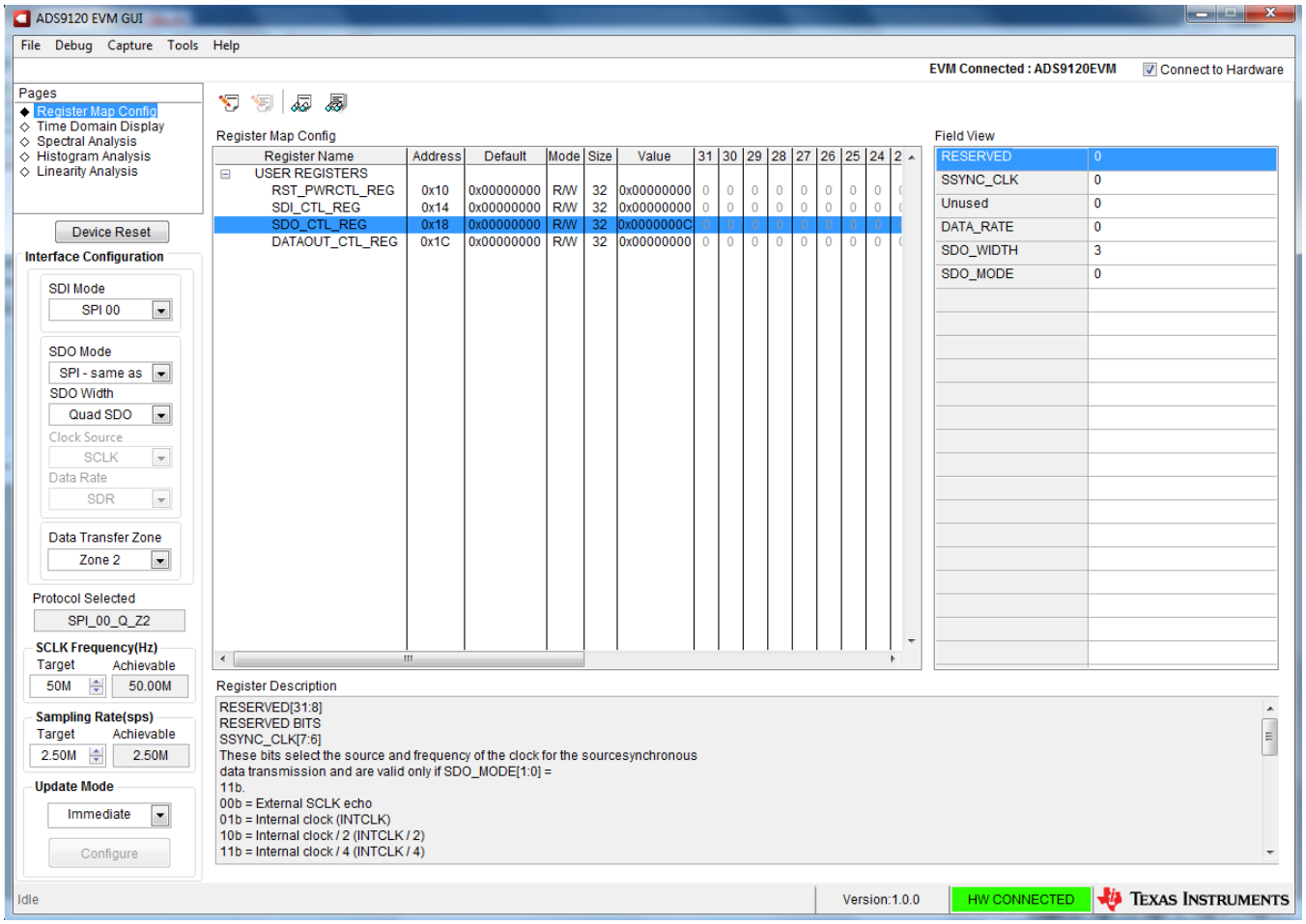

Figure 10. EVM GUI Global Input Parameters

The host configuration options in this pane allow the user to choose from various SPI and multiSPI host interface options available on the ADS9120. The host always communicates with the ADS9120 using the standard SPI protocol over the single SDI lane, irrespective of the mode selected for data capture.

The drop-down boxes under the Interface Configuration sub-menu allows the user to select the data capture protocol. The SDO Width drop-down allows selection between Single-, Dual- and Quad-SDO lanes; The SDO Mode drop-down allows selection between Standard SPI and multiSPI modes.

In SPI mode, the SDI Mode drop-down allows selection between the four SPI protocol combinations for CPOL and CPHA.

In multiSPI mode, the Clock Source drop-down allows selection between Source and System Synchronous modes; the Data Rate drop-down allows selection between SDR and DDR modes. Detailed descriptions of each of these modes is available in the ADS9120 datasheet (SBAS710). The selected data capture protocol is summarized in the Protocol Selected indicator box.

The user can select SCLK Frequency and Sampling Rate on this pane and is dependent of the Protocol selected. The GUI allows the user to enter the targeted values for these two parameters and the GUI computes the best values that can be achieved, considering the timing constraints of the selected Device Protocol.

The user can specify a target SCLK frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings and the achievable frequency that can differ from the target value displayed. Similarly, the sampling rate of the ADC can be adjusted by modifying the Target Sampling Rate argument (also in Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and selected Device Mode and the closest match achievable is displayed. This pane therefore allows the user to try various settings available on the ADS9120 in an iterative fashion until the user converges to the best settings for the corresponding test scenario.

The final option in this pane is the selection for the Update Mode. The default value is *Immediate*, indicating that the interface settings selection made by the user is applied to configure both the host and the ADS9120 instantly. *Manual* indicates that the selection made is made only when the user finalizes their choices and is ready to configure the device.

The Device Reset button functions as a Master RESET to both the ADS9120EVM and the GUI. When the button is pressed, the ADC RESETs to the RESET configuration explained in the datasheet (SBAS710). The GUI also updates the Interface Configuration settings and the Register Map to reflect the device RESET state.

6.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the ADS9120. This tool can be selected by clicking on the Register Map Config radio button at the Pages section of the left pane, as indicated in Figure 11. On power-up, the values on this page correspond to the Host Configuration Settings that enable ADC sampling at the maximum sampling rate specified for the ADC. The register values can be edited by double-clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately. The effect of changes in the register value reflect on the ADS9120 device on ADS9120EVM-PDK based on the Update Mode selection, as described in Section 6.1.

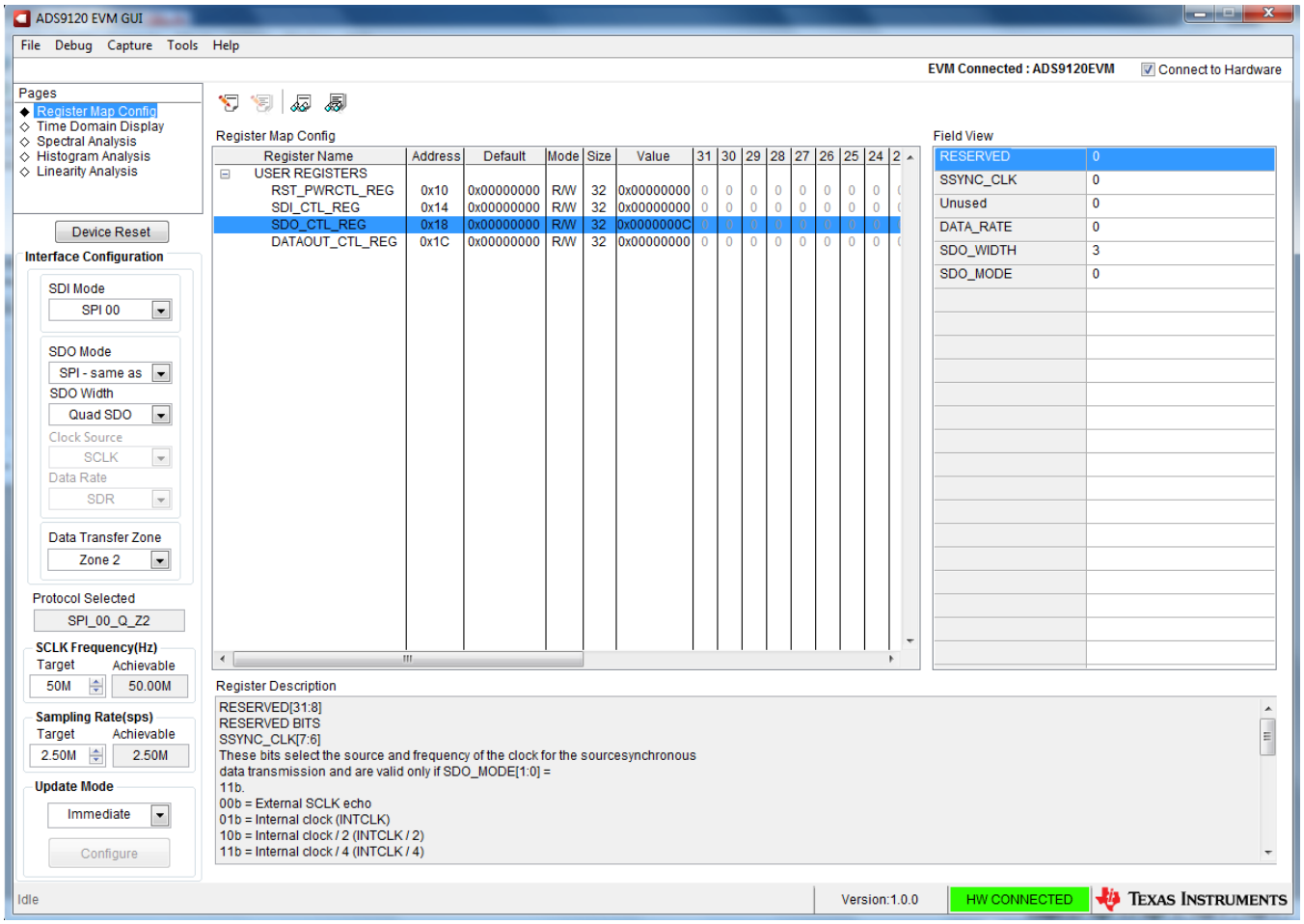

Figure 11. Register Map Configuration

Section 6.3 through Section 6.6 describe the data collection and analysis features of the ADS9120EVM-PDK GUI.

6.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS9120, as per the current interface mode settings using the capture button as indicated in Figure 12. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections, triggers calculations to be performed on the same set of data.

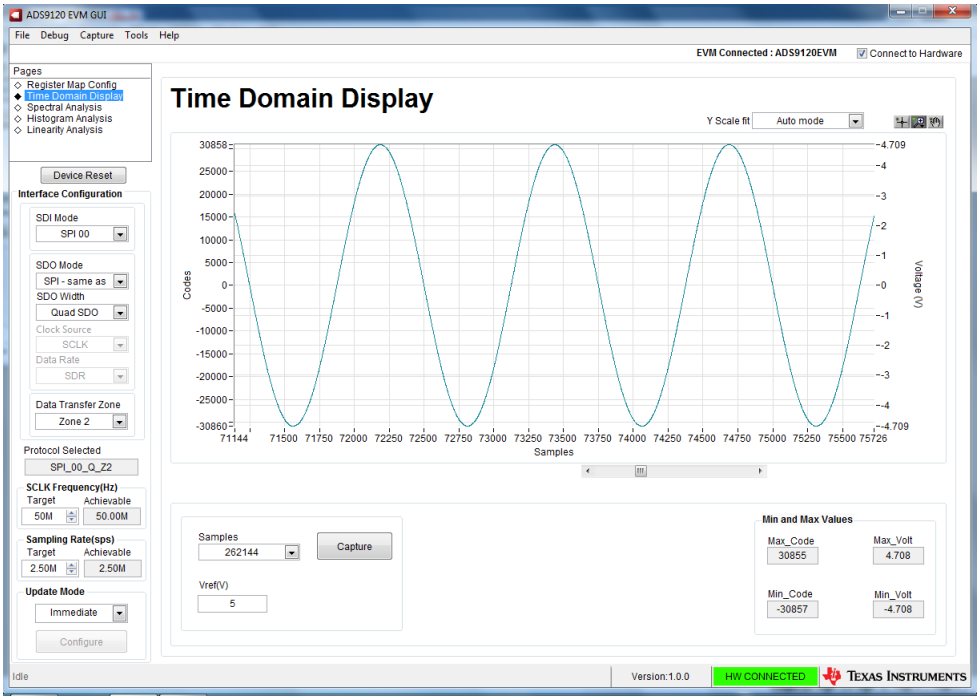

Figure 12. Time Domain Display Tool Options

6.4 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS9120 SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. Also, the window setting of *None* can be used to search for noise spurs over frequency in dc inputs.

For dynamic performance evaluation, the external differential source must have better specifications than the ADC itself to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 4.

Table 4. External Source Requirements for Evaluation of the ADS9120

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Balanced differential
External source common-mode	0 V or floating (see Section 2.2.2 for jumper settings)
External source impedance (R_S)	10 Ω–30 Ω
External source differential impedance ($R_{S\_DIFF} = 2 \times R_S$)	20 Ω–60 Ω
Source differential signal (V_{PP} Amplitude for –0.1 dBFS)	$(2 \times R_S \times 4.45 \times 10^{-3}) + 8.9$ V or $(R_{S\_DIFF} \times 4.45 \times 10^{-3}) + 8.9$ V
Maximum noise	10 μV_{RMS}
Maximum SNR	110 dB
Maximum THD	–130 dB

For 2-kHz SNR and ENOB evaluation at a maximum throughput of 2.5 MSPS, the number of samples must be 32768 or 65536. More samples brings the noise floor so low that the external source phase noise can dominate the SNR and ENOB calculations. On the contrary, for THD and SFDR evaluation, a much large number of samples must be used to reduce the noise floor below –140 dBc to analyze noise-free harmonics and spurs in the order of –120 dBc. Such analysis requires at least 262144 samples.

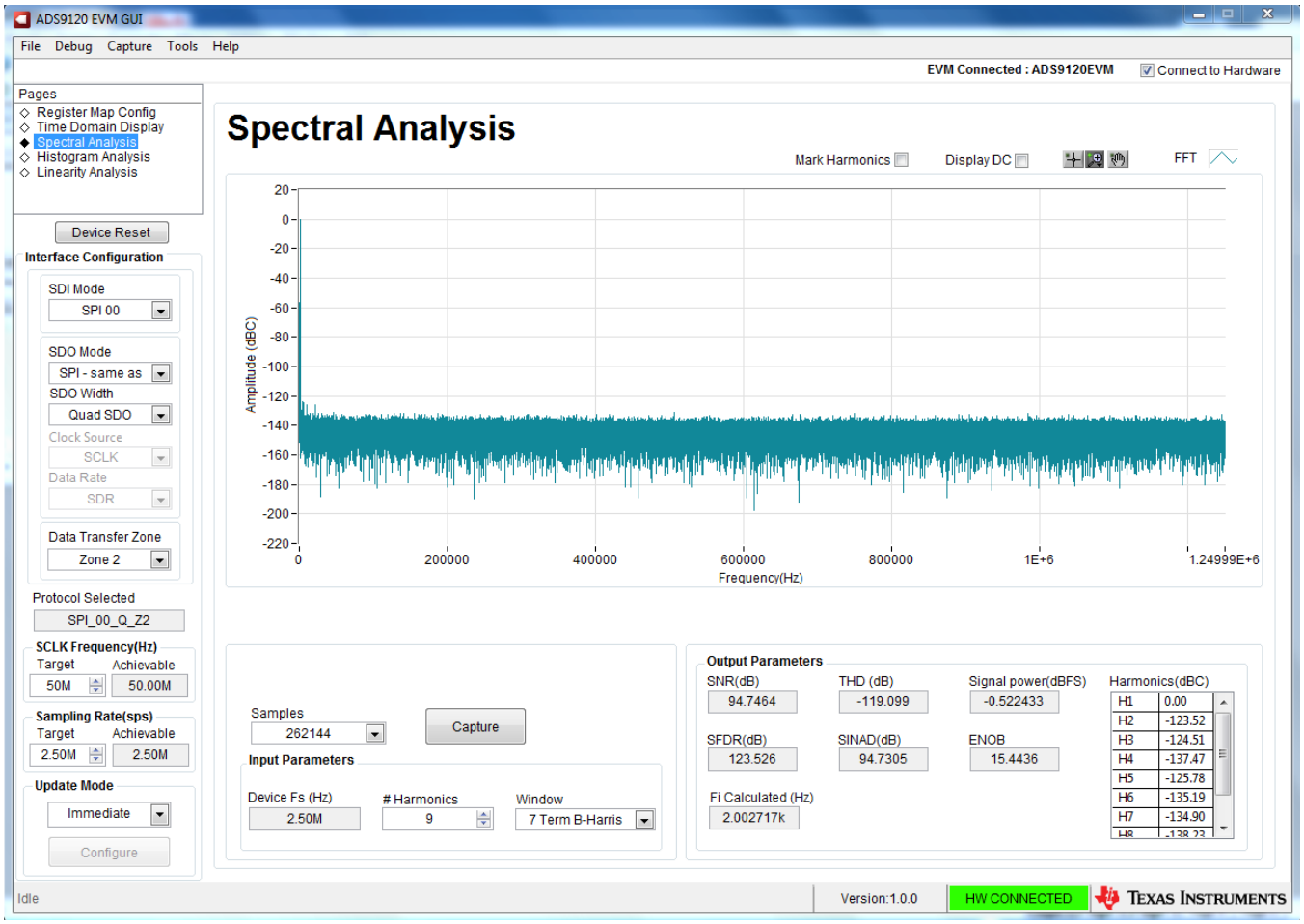

Figure 13. Spectral Analysis Tool

Finally, the FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. Note that the *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

6.5 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking on the **Capture** button, as shown in Figure 14:

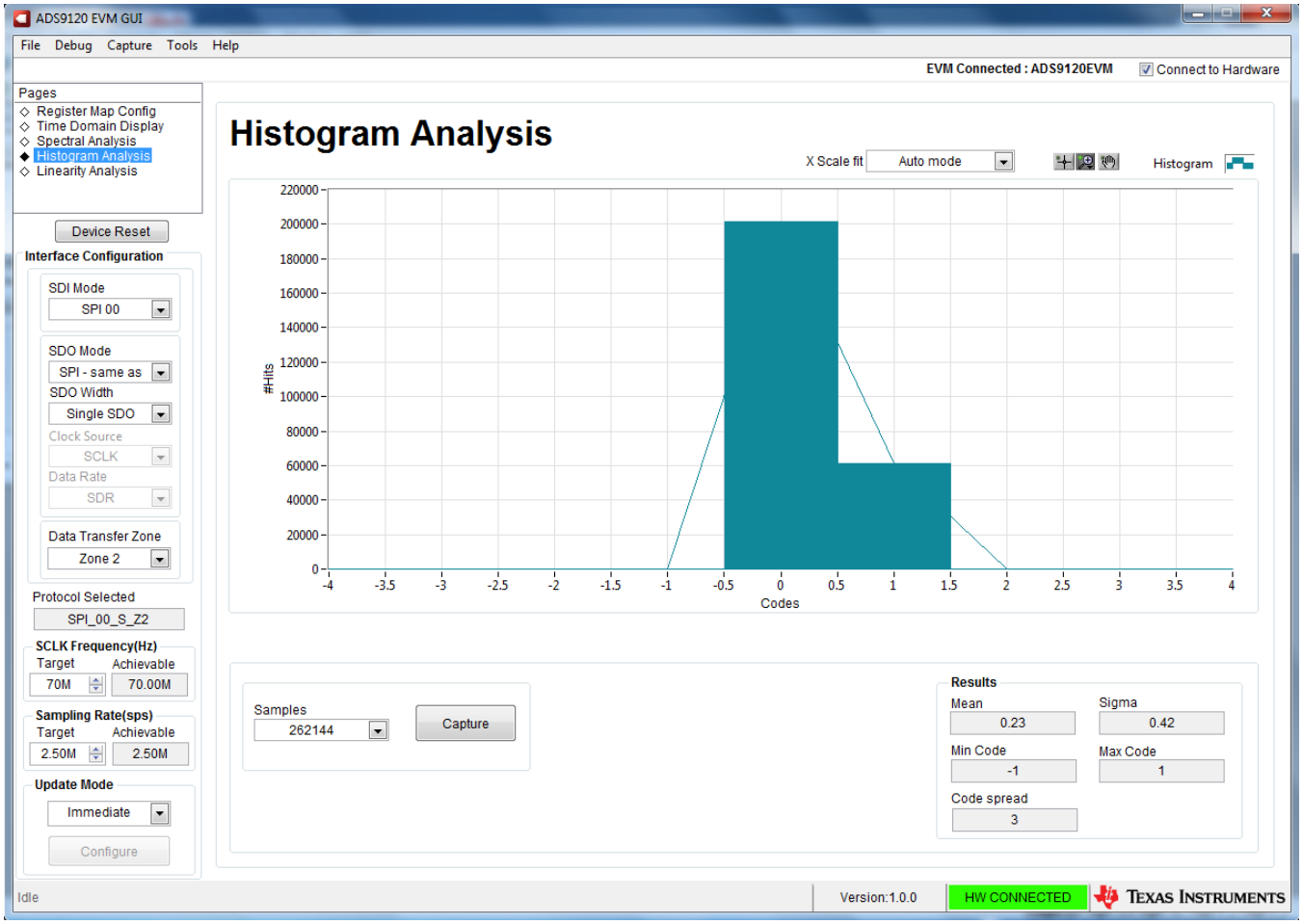

Figure 14. Histogram Analysis Tool

6.6 Linearity Analysis Tool

The linearity analysis tool measures and generates the DNL and INL plots over code for the specific ADS9120 installed in the evaluation board. A 2-kHz sinusoidal input signal is required, which is slightly saturated (35 mV outside the full-scale range at each input or 0.13 dBFS) with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Table 5.

Table 5. External Source Requirements for ADS9120 Evaluation

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Balanced differential
External source common mode	0 V or floating (see Section 2.2.2 for jumper settings)
External source impedance (R_S)	10 Ω–30 Ω
External source differential impedance ($R_{S\_DIFF} = 2 \times R_S$)	20 Ω–60 Ω
Source differential signal (V_{PP} amplitude for –0.1 dBFS)	$(2 \times R_S \times 4.57 \times 10^{-3}) + 9.14$ V or $(R_{S\_DIFF} \times 4.57 \times 10^{-3}) + 9.14$ V
Maximum noise	30 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–130 dB

The number-of-hits setting depends on the external noise source. For a 110-dB SNR external source with approximately 10 µVrms of noise, total number of hits must be 512. For a source with 100-dB SNR, the recommended number of hits is 1024.

NOTE: This analysis can take a couple of minutes to run and the evaluation board must remain undisturbed during the complete duration of the analysis.

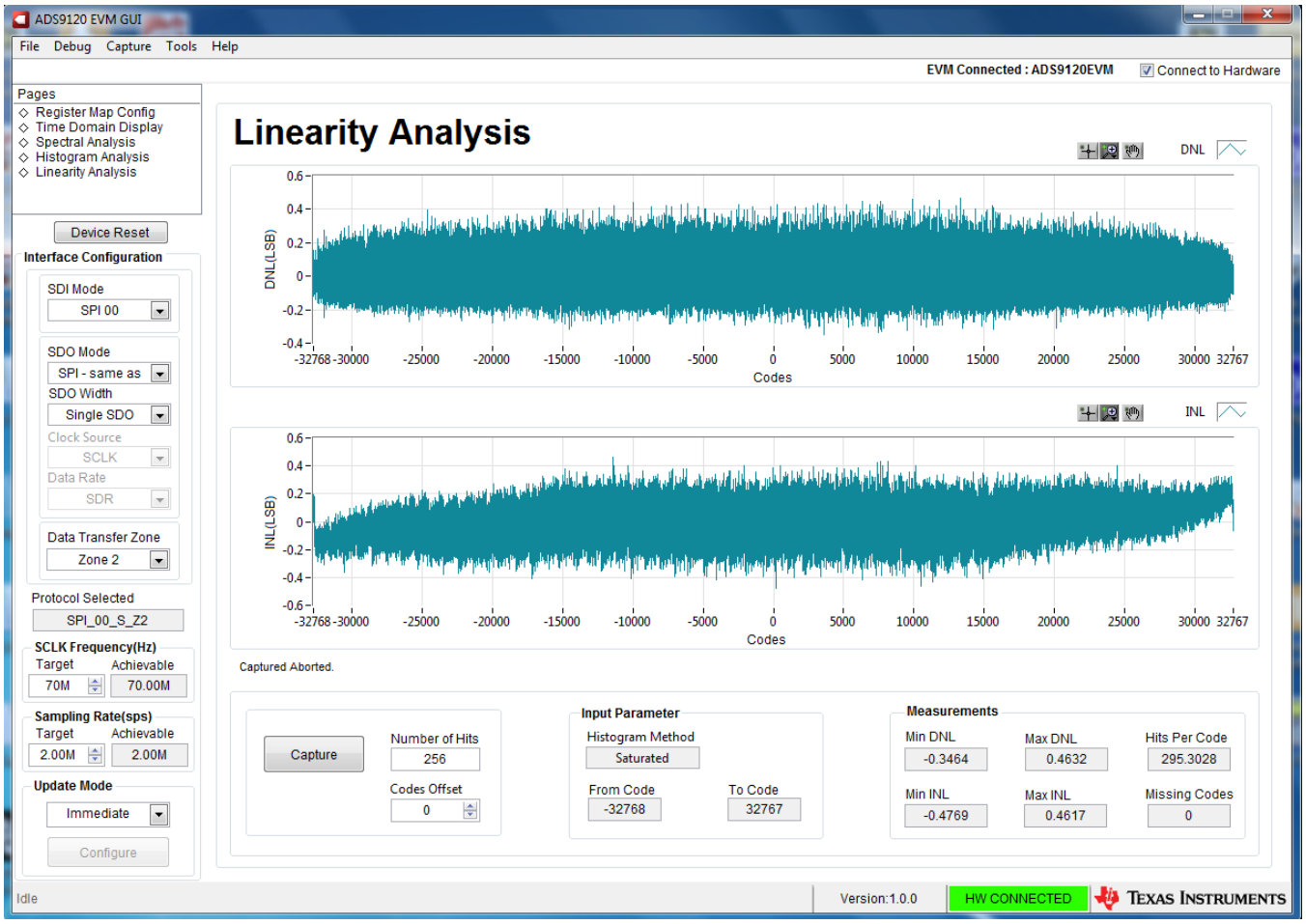

Figure 15. Linearity Analysis Tool

7 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS9120EVM bill of materials, PCB layout, and the EVM schematics.

7.1 Bill of Materials

Table 6 lists the ADS9120EVM BOM.

Table 6. ADS9120EVM Bill of Materials

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
PA006	1	!PCB	Any	Printed Circuit Board for Evaluation of ADS9120
PHI-EVM-CONTROLLER (Edge# 6591636 rev. B)	1	!PCB2	Texas Instruments	USB Controller Board for ADC EVMs (Kit Item)
C3216X5R1E476M160AC	2	C1, C3	TDK	CAP, CERM, 47 µF, 25 V, +/- 20%, X5R, 1206
GRM188R71E105KA12D	9	C2, C5, C6, C8, C12, C32, C38, C40, C43	MuRata	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603
GRM21BR71A106KE51L	6	C4, C21, C26, C41, C44, C48	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805
C0603C104J3RACTU	4	C7, C9, C10, C17	Kemet	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603
ZRB18AD71A106KE01L	9	C13, C15, C27, C28, C29, C39, C45, C50, C51	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7T, 0603
GRM1885C1H102FA01J	3	C16, C31, C42	MuRata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603
C0603C100F5GAC7867	1	C18	Kemet	CAP, CERM, 10 pF, 50 V, +/- 1%, C0G/NP0, 0603
C0603C224J3RAC7867	1	C19	Kemet	CAP, CERM, 0.22 µF, 25 V, +/- 5%, X7R, 0603
C0805C103F1GACTU	3	C34, C35, C37	Kemet	CAP, CERM, 0.01 µF, 100 V, +/- 1%, C0G/NP0, 0805
GRM155R71C104KA88D	2	C47, C49	MuRata	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402
APT2012LZGCK	1	D1	Kingbright	LED, Green, SMD
CUS05S40,H3F	1	D2	Toshiba	Diode, Schottky, 40 V, 0.5 A, SOD-323
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
1891	4	H5, H6, H7, H8	Keystone	3/16 Hex Female Standoff
9774050360R	2	H9, H10	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
RM3X4MM 2701	2	H14, H15	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
87898-0204	2	J1, J2	Molex	Header, 2.54 mm, 2x1, Gold, R/A, SMT
142-0701-801	2	J3, J7	Johnson	Connector, End launch SMA, 50 ohm, SMT
TSM-103-01-L-SV	3	J4, J6, J8	Samtec	Header, 100mil, 3x1, Gold, SMT
QTH-030-01-L-D-A	1	J5	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
THT-14-423-10	1	LBL1	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
RG2012P-2803-B-T5	1	R1	Susumu Co Ltd	RES, 280 k, 0.1%, 0.125 W, 0805

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
ERJ-3RSFR10V	1	R2	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
RG1608P-103-B-T5	1	R5	Susumu Co Ltd	RES, 10.0 k, 0.1%, 0.1 W, 0603
ERJ-2RKF1002X	3	R6, R23, R65	Panasonic	RES, 10.0 k, 1%, 0.1 W, 0402
ERJ-2GE0R00X	17	R7, R11, R12, R32, R34, R35, R37, R40, R42, R43, R46, R47, R49, R51, R53, R63, R64	Panasonic	RES, 0, 5%, 0.063 W, 0402
ERJ-3RQFR22V	2	R8, R58	Panasonic	RES, 0.22, 1%, 0.1 W, 0603
RG1608P-203-B-T5	3	R10, R15, R20	Susumu Co Ltd	RES, 20.0 k, 0.1%, 0.1 W, 0603
RG1608P-102-B-T5	6	R16, R29, R41, R45, R54, R55	Susumu Co Ltd	RES, 1.00 k, 0.1%, 0.1 W, 0603
RG1608P-4991-B-T5	1	R17	Susumu Co Ltd	RES, 4.99 k, 0.1%, 0.1 W, 0603
ERJ-3GEY0R00V	5	R19, R24, R57, R59, R60	Panasonic	RES, 0, 5%, 0.1 W, 0603
RG1608P-4990-B-T5	2	R21, R30	Susumu Co Ltd	RES, 499, 0.1%, 0.1 W, 0603
RG1608P-2491-B-T5	1	R22	Susumu Co Ltd	RES, 2.49 k, 0.1%, 0.1 W, 0603
RG1608P-303-B-T5	1	R27	Susumu Co Ltd	RES, 30.0 k, 0.1%, 0.1 W, 0603
CRCW06034R75FKEA	1	R31	Vishay-Dale	RES, 4.75, 1%, 0.1 W, 0603
RG1608P-101-B-T5	2	R38, R44	Susumu Co Ltd	RES, 100, 0.1%, 0.1 W, 0603
CRCW06032R21FKEA	2	R48, R50	Vishay-Dale	RES, 2.21, 1%, 0.1 W, 0603
881545-2	3	SH-J1, SH-J2, SH-J3	TE Connectivity	Shunt, 100mil, Gold plated, Black
5016	5	TP1, TP2, TP3, TP4, TP5	Keystone	Test Point, Compact, SMT
5015	2	TP6, TP7	Keystone	Test Point, Miniature, SMT
REF5050AIDGKT	1	U1	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin VSSOP (DGK), Green (RoHS & no Sb/Br)
TPS7A4700RGW	1	U2	Texas Instruments	36-V, 1-A, 4.17-µVRMS, RF LDO Voltage Regulator, RGW0020A
OPA376AIDBVR	1	U3	Texas Instruments	Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim Series, DBV0005A
OPA378AIDBVT	1	U5	Texas Instruments	Low-Noise, 900 kHz, RRIO, Precision Operational Amplifier, Zerø-Drift Series, 2.2 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS & no Sb/Br)
OPA625IDBVR	3	U6, U9, U10	Texas Instruments	High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers, DBV0006A
BR24G32FVT-3AGE2	1	U8	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
ADS9120IRGER	1	U11	Texas Instruments	16-Bit, 2.5-MSPS, 20-mW, SAR ADC with Enhanced Serial Interface, RGE0024H
EMK212BJ475KG-T	0	C11	Taiyo Yuden	CAP, CERM, 4.7 µF, 16 V, +/- 10%, X5R, 0805
ZRB18AD71A106KE01L	0	C14, C24, C52, C53	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7T, 0603
C2012X7S1A226M125AC	0	C20, C55, C57	TDK	CAP, CERM, 22 µF, 10 V, +/- 20%, X7S, 0805
GRM188R71A105KA61D	0	C22	MuRata	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603
GRM21BR71A106KE51L	0	C23	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
GRM21BR71A106KE51L	0	C25	MuRata	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805
GRM155R71C104KA88D	0	C30	MuRata	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402
GRM32ER71A476KE15L	0	C33	MuRata	CAP, CERM, 47 µF, 10 V, +/- 10%, X7R, 1210
GRM188R71E105KA12D	0	C36	MuRata	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603
C0603C224J3RAC7867	0	C54	Kemet	CAP, CERM, 0.22 µF, 25 V, +/- 5%, X7R, 0603
GMK212BJ474KG-T	0	C56	Taiyo Yuden	CAP, CERM, 0.47 µF, 35 V, +/- 10%, X5R, 0805
N/A	0	FID1, FID2, FID3, FID4, FID5, FID6	N/A	Fiducial mark. There is nothing to buy or mount.
102-1092-BL-00100	0	H12	CNC Tech	CABLE USB A MALE-B MICRO MALE 1M (Kit Item)
ERJ-2GE0R00X	0	R3, R4, R9, R13, R14, R18, R52, R61, R62	Panasonic	RES, 0, 5%, 0.063 W, 0402
ERJ-3RQFR22V	0	R25, R26	Panasonic	RES, 0.22 ohm, 1%, 0.1W, 0603
ERJ-2RKF1002X	0	R28	Panasonic	RES, 10.0 k, 1%, 0.1 W, 0402
RC0603FR-071RL	0	R33	Yageo America	RES, 1.00, 1%, 0.1 W, 0603
ERJ-3RQFR22V	0	R36, R39	Panasonic	RES, 0.22, 1%, 0.1 W, 0603
ERJ-6GEYJ4R7V	0	R56	Panasonic	RES, 4.7, 5%, 0.125 W, 0805
LM7705MM/NOPB	0	U4	Texas Instruments	Low Noise Negative Bias Generator, 8-pin Mini SOIC, Pb-Free
REF6025AIDGK	0	U7	Texas Instruments	High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A

7.2 PCB Layout

Figure 16 through Figure 19 illustrate the EVM PCB layout.

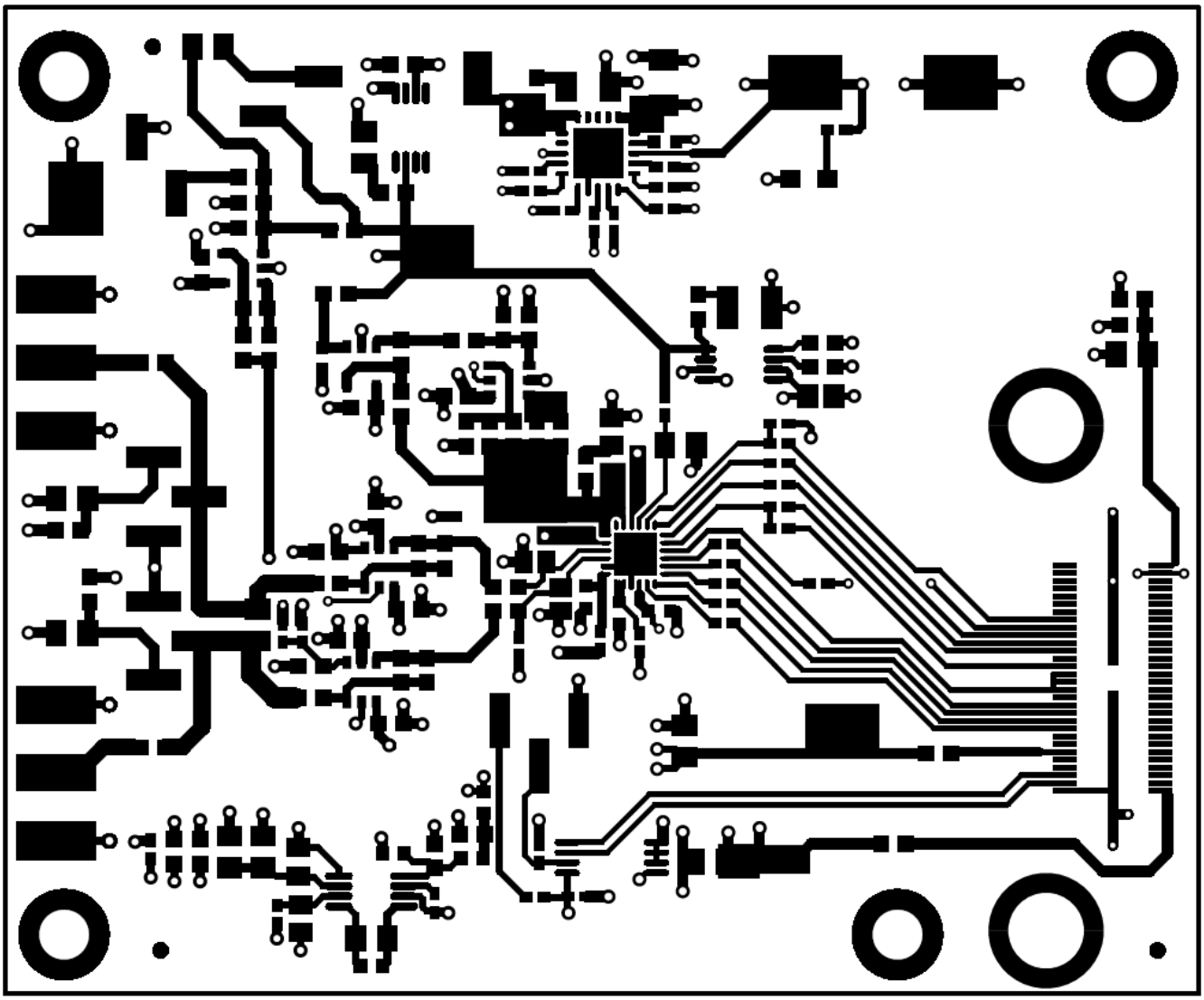

Figure 16. ADS9120EVM PCB Layer 1: Top Layer

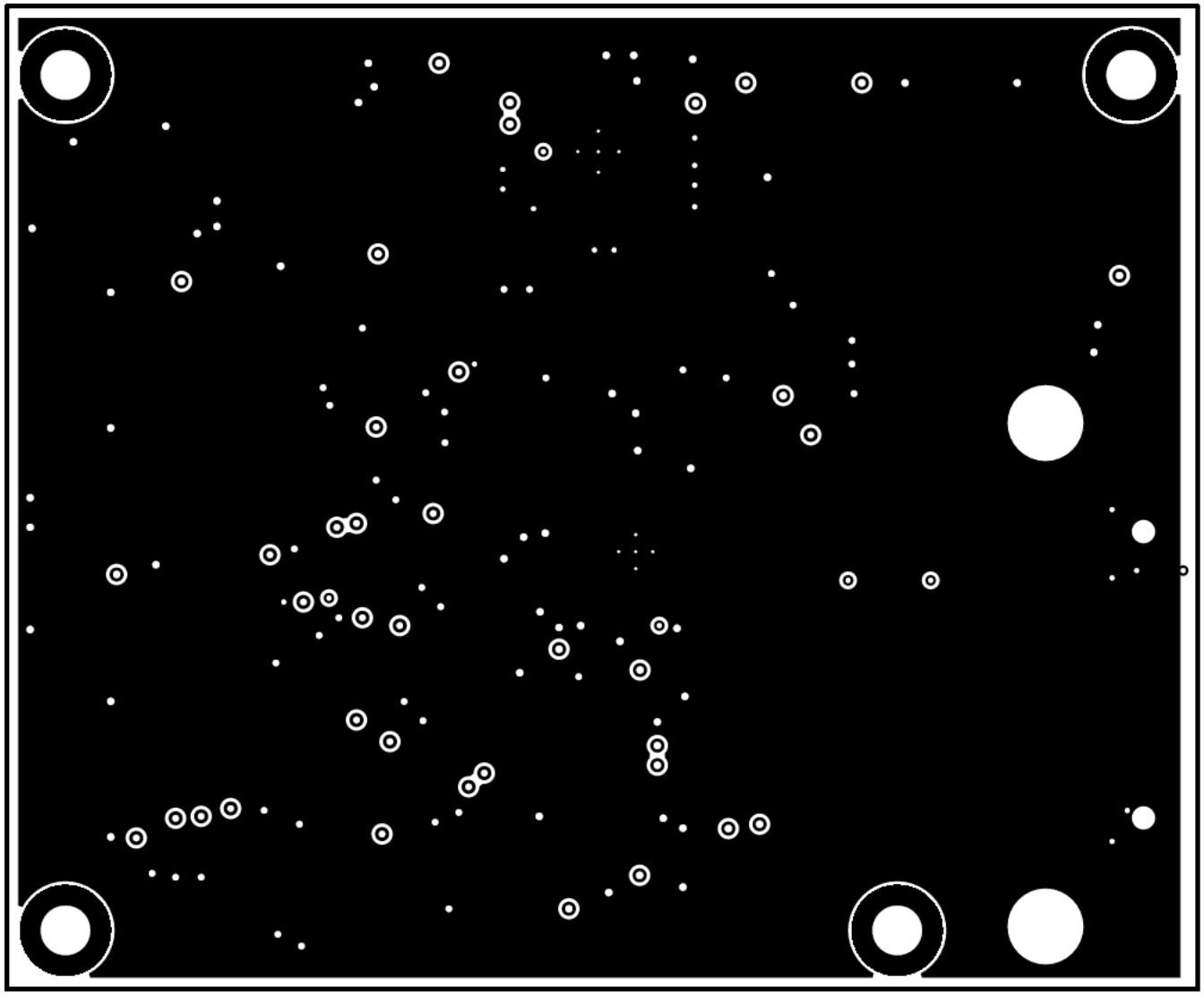

Figure 17. ADS9120EVM PCB Layer 2: GND Plane

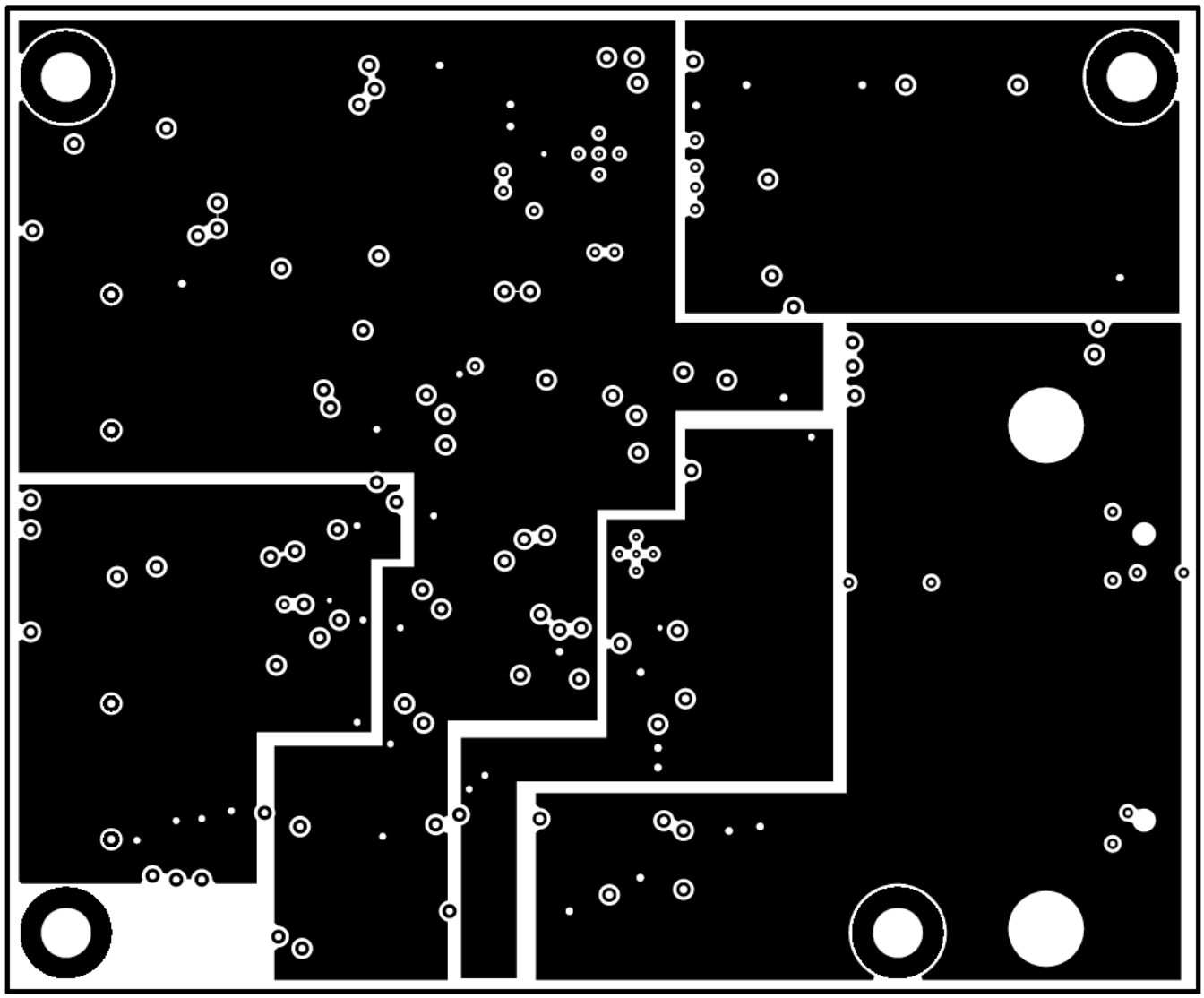

Figure 18. ADS9120EVM PCB Layer 3: Power Planes

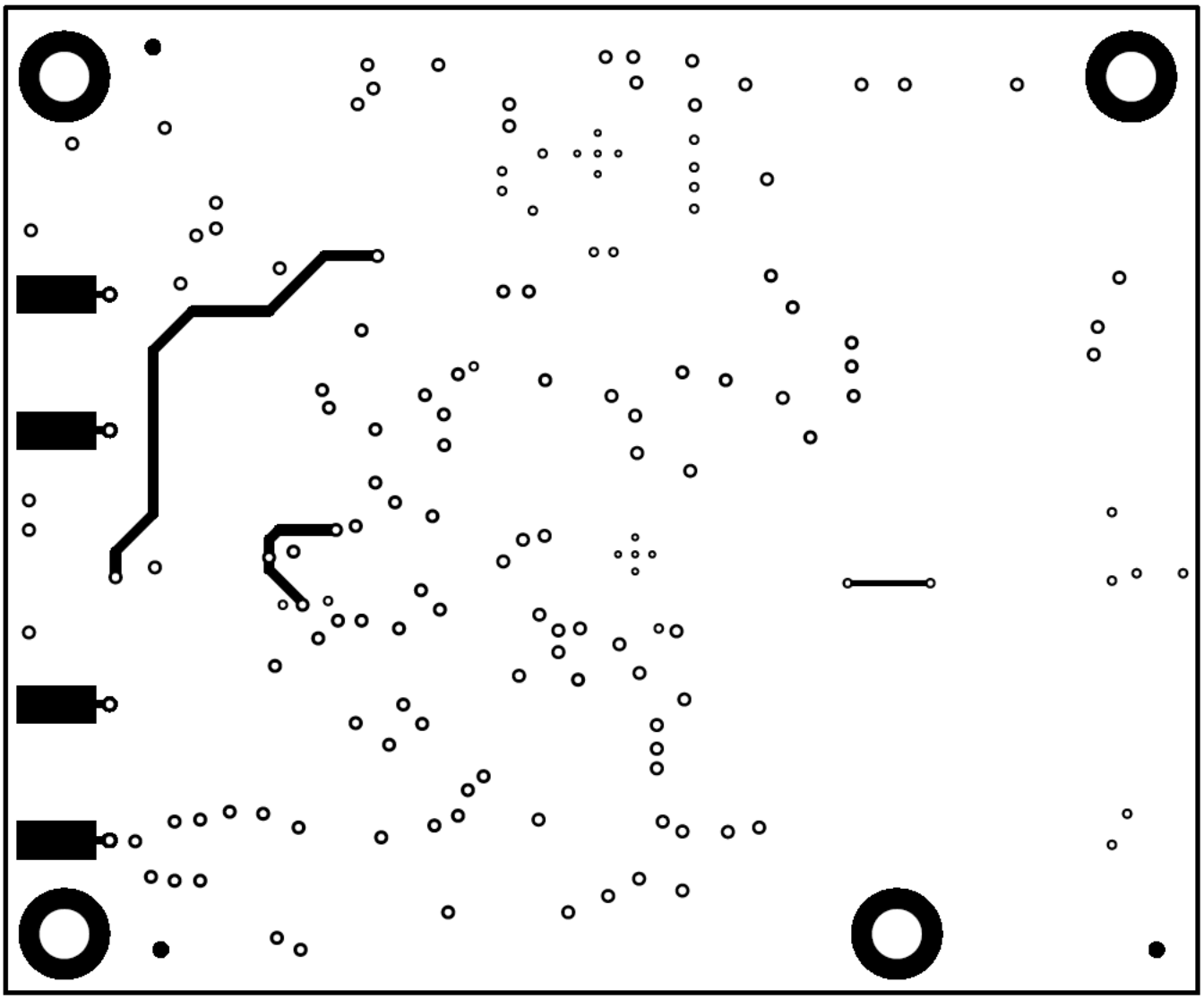

Figure 19. ADS9120EVM PCB Layer 4: Bottom Layer

7.3 Schematics

Figure 20 through Figure 22 illustrate the EVM schematics.

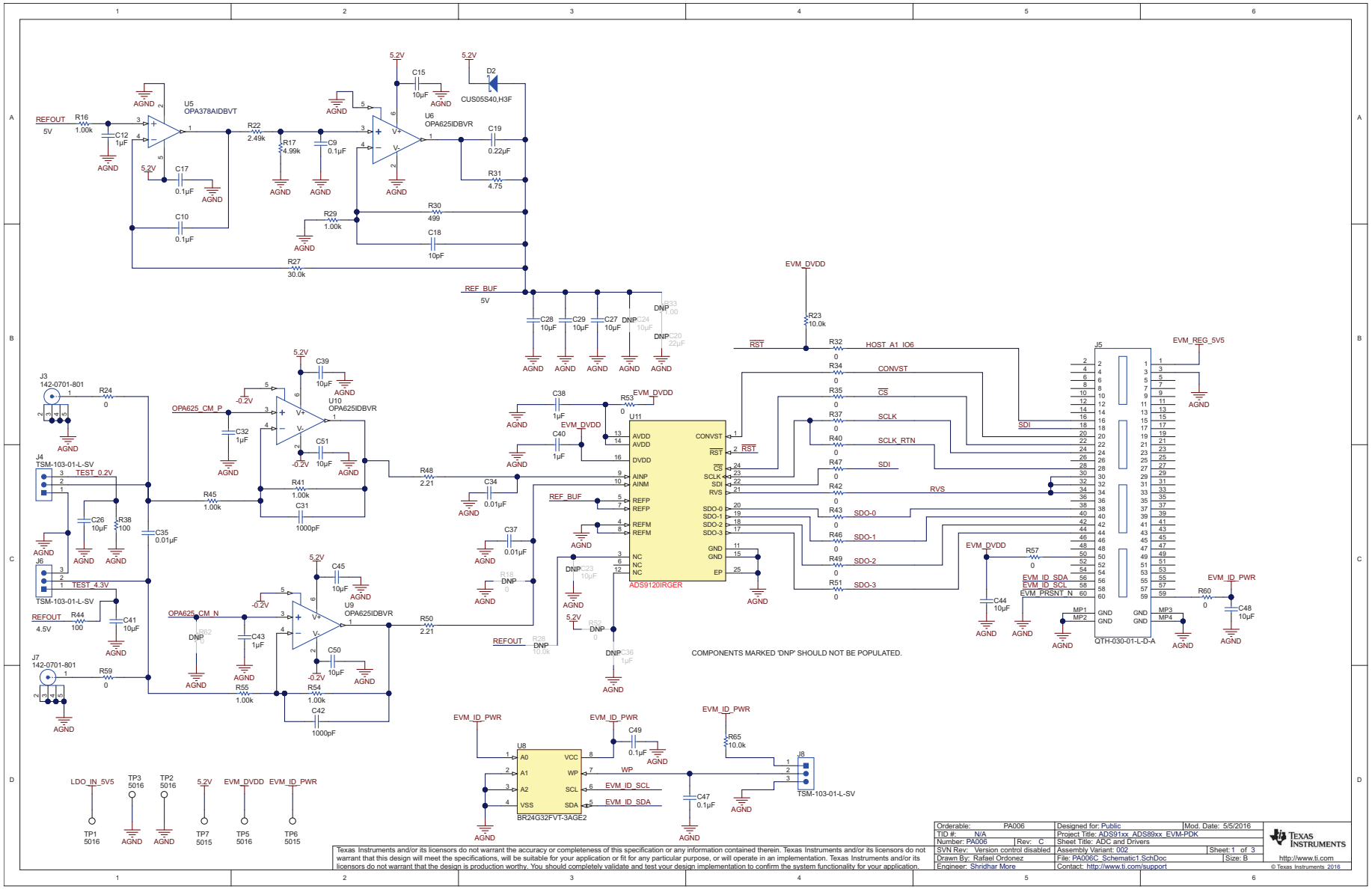

Figure 20. Schematic Diagram (Page 1) of the ADS9120EVM PCB

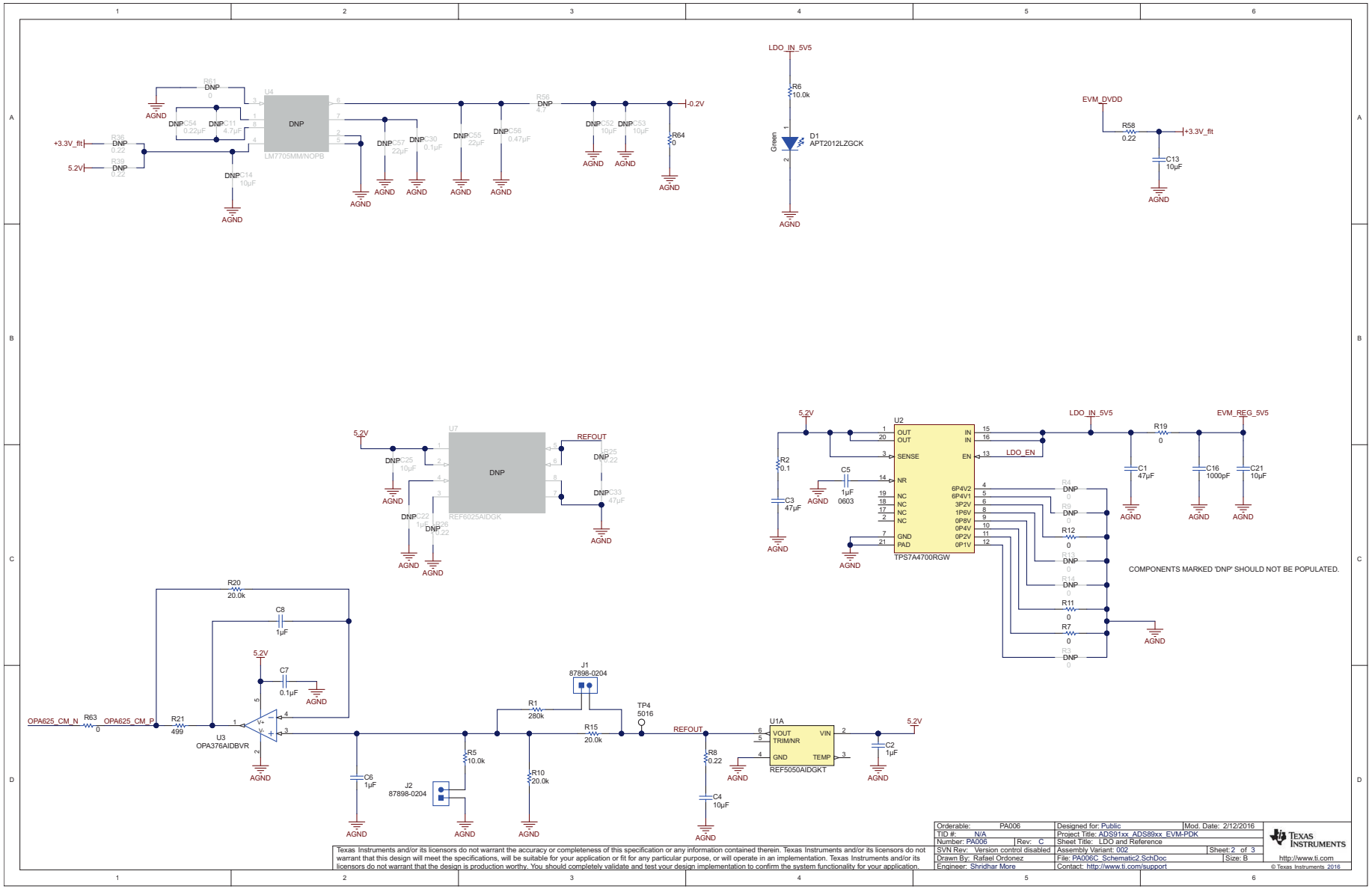

Figure 21. Schematic Diagram (Page 2) of the ADS9120EVM PCB

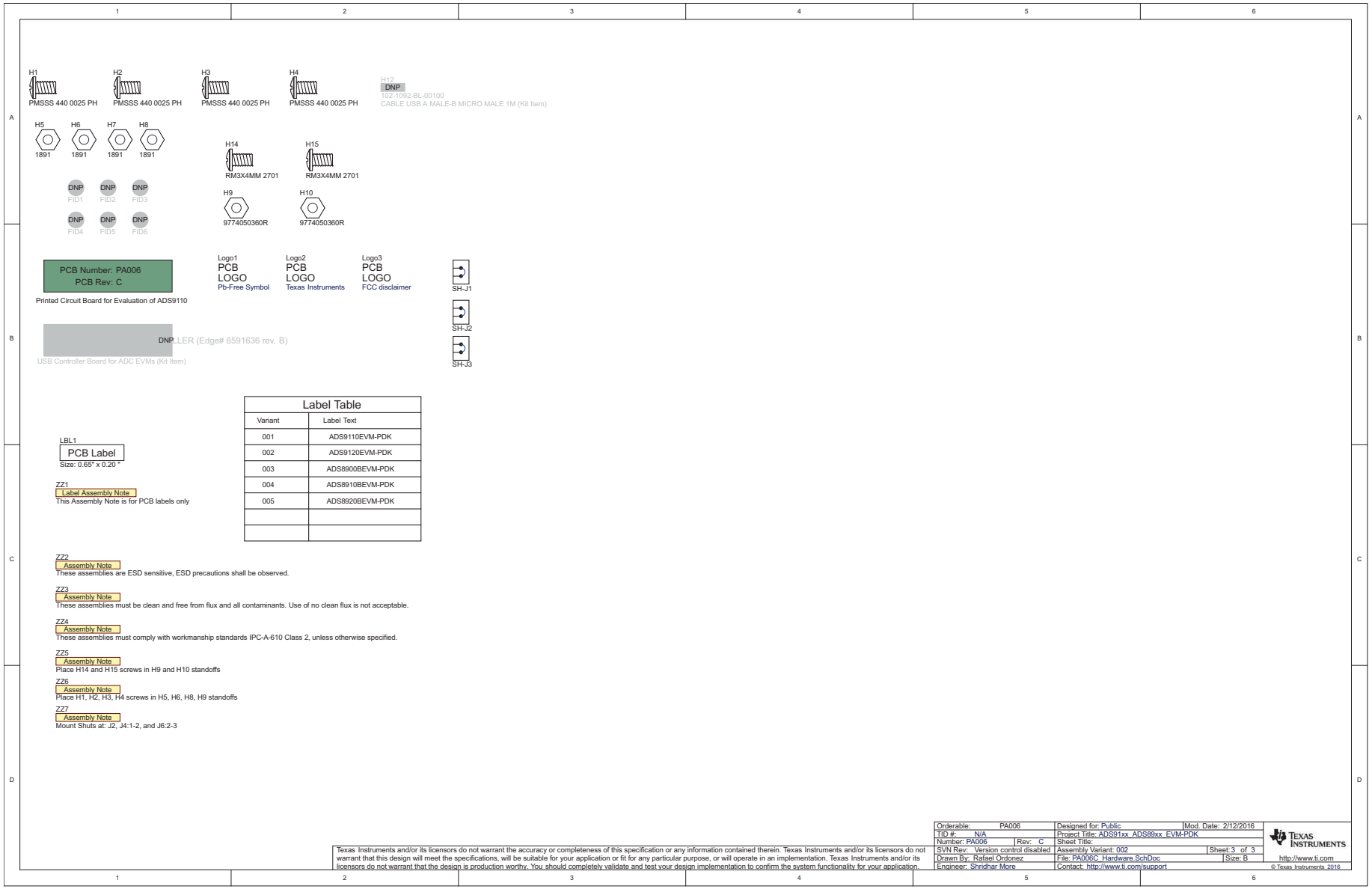

Figure 22. Schematic Diagram (Page 3) of the ADS9120EVM PCB

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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