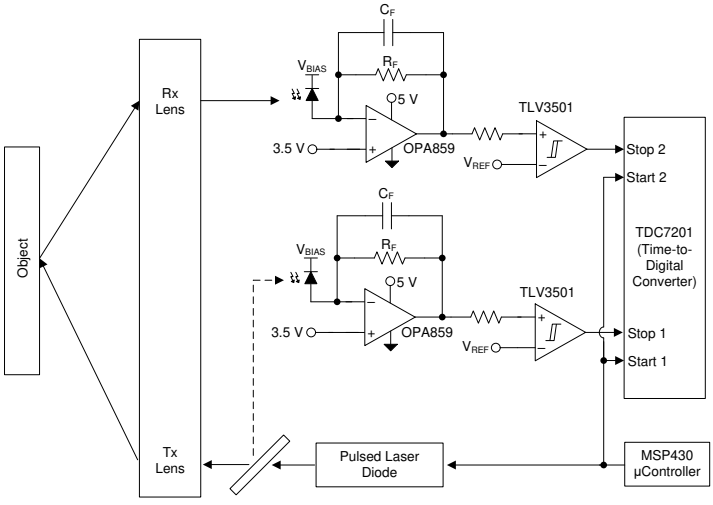
OPA859 1.8GHz Unity-Gain Bandwidth, 3.3nV/√Hz, FET Input Amplifier

1 Features

- High unity-gain bandwidth: 1.8GHz
- Gain bandwidth product: 900MHz
- Ultra-low bias current MOSFET inputs: 10pA
- Low input voltage noise: 3.3nV/√Hz
- Slew rate: 1150V/µs
- Low Input capacitance:
  - Common-mode: 0.6pF
  - Differential: 0.2pF
- Wide input common-mode range:
  - 1.4V from positive supply
  - Includes negative supply
- $2.5V_{PP}$ output swing in TIA configuration
- Supply voltage range: 3.3V to 5.25V
- Quiescent current: 20.5mA
- Package: 8-pin WSON
- Temperature range: –40°C to +125°C

2 Applications

- Optical time domain reflectometry (OTDR)
- 3D scanner
- Laser distance measurement
- Solid-state scanning LIDAR
- Optical ToF position sensor
- Drone vision
- Industrial robot LIDAR
- Vacuum robot LIDAR
- Silicon photomultiplier (SiPM) buffer amplifier
- Photomultiplier tube post amplifier



High-Speed Time-of-Flight Receiver

3 Description

The OPA859 is a wideband, low-noise operational amplifier with CMOS inputs for wideband transimpedance and voltage amplifier applications. When the device is configured as a transimpedance amplifier (TIA), the 0.9GHz gain bandwidth product (GBWP) enables high closed-loop bandwidths in low-capacitance photodiode applications.

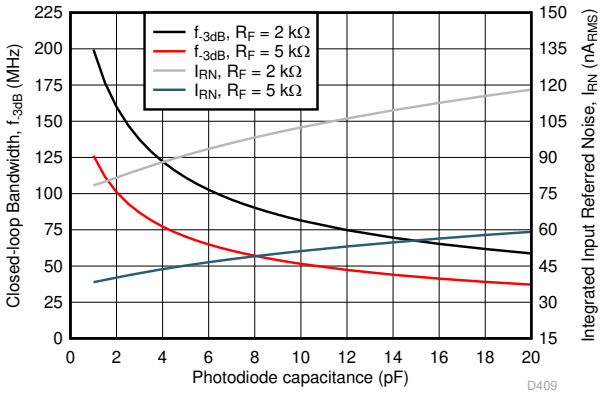
The following graph shows the bandwidth and noise performance of the OPA859 as a function of the photodiode capacitance when the amplifier is configured as a TIA. The total noise is calculated along a bandwidth range extending from dc to the calculated frequency (*f*) on the left scale. The OPA859 package has a feedback pin (FB) that simplifies the feedback network connection between the input and the output.

The OPA859 is optimized to operate in optical time-of-flight (ToF) systems where the OPA859 is used with time-to-digital converters, such as the TDC7201. Use the OPA859 to drive a high-speed analog-to-digital converter (ADC) in high-resolution LIDAR systems with a differential output amplifier, such as the THS4541 or LMH5401 devices.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA859	DSG (WSON, 8)	2mm × 2mm
	Bare die	0.751mm × 0.705mm

(1) See the *Device Comparison Table*.
(2) For more information, see Section 12.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Photodiode Capacitance vs Bandwidth and Noise

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4 Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN	VOLTAGE NOISE (nV/√Hz)	INPUT CAPACITANCE (pF)	GAIN BANDWIDTH (GHz)
OPA859	CMOS	1V/V	3.3	0.8	0.9
OPA858	CMOS	7V/V	2.5	0.8	5.5
OPA855	Bipolar	7V/V	0.98	0.8	8
LMH6629	Bipolar	10V/V	0.69	5.7	4

5 Pin Configuration and Functions

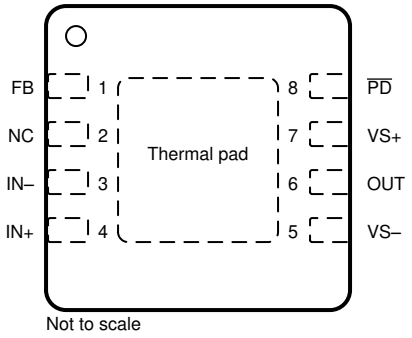


**Figure 5-1. DSG Package,
8-Pin WSON With Exposed Thermal Pad
(Top View)**

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
FB	1	Input	Feedback connection to output of amplifier
IN–	3	Input	Inverting input
IN+	4	Input	Noninverting input
NC	2	—	Do not connect
OUT	6	Output	Amplifier output
$\overline{PD}$	8	Input	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to VS–

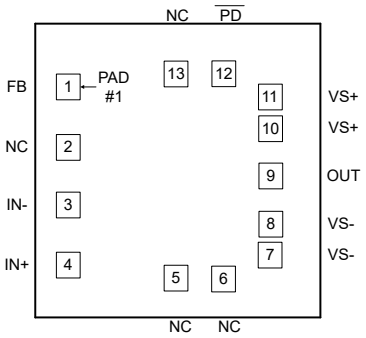


Figure 5-2. Bare Die Package

Table 5-2. Bond Pad Functions

PAD		TYPE	DESCRIPTION
NAME	NO.		
FB	1	Input	Feedback connection to output of amplifier
IN–	3	Input	Inverting input
IN+	4	Input	Noninverting input
NC	2,5,6, 13	—	Do not connect
OUT	9	Output	Amplifier output
$\overline{PD}$	12	Input	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	7,8	—	Negative voltage supply
VS+	10,11	—	Positive voltage supply
Backside		—	Connect to VS–

Table 5-3. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION
381 µm	Silicon with backgrind	Wafer backside is electrically connected to VS–	AlCu

Table 5-4. Bond Pad Coordinates of Bare Die Version in Microns

PAD NUMBER	PAD NAME	X-MIN	Y-MIN	X-MAX	Y-MAX
1	FB	14.5	537.4	79.5	602.4
2	NC	14.5	379	79.5	444
3	IN–	14.5	227	79.5	292
4	IN+	14.5	68.6	79.5	133.6
5	NC	296.725	34.825	361.725	99.825
6	NC	421.725	34.825	486.725	99.825
7	VS–	545.5	93.8	610.5	158.8
8	VS–	545.5	178.8	610.5	243.8
9	OUT	545.5	303	610.5	368
10	VS+	545.5	427.2	610.5	492.2
11	VS+	545.5	512.2	610.5	577.2
12	$\overline{PD}$	421.325	571.175	486.325	636.175
13	NC	297.125	571.175	362.125	636.175

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)		5.5	V
V_{IN+}, $V_{IN–}$	Input voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
V_{ID}	Differential input voltage		1	V
V_{OUT}	Output voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current(2)		±100	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)	3.3	5	5.25	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA859 DSG (WSON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	45	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	6.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	45.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{S+} = 5 V, V_{S-} = 0 V, input common-mode biased at midsupply, unity gain configuration, R_L = 200 Ω, output load is referenced to midsupply, and T_A ≈ +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		1.8		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		400		MHz
GBWP	Gain-bandwidth product			900		MHz
	Bandwidth for 0.1dB flatness			140		MHz
SR	Slew rate (10%–90%)	V_{OUT} = 2-V step		1150		V/µs
t_r	Rise time	V_{OUT} = 100-mV step		0.3		ns
t_f	Fall time	V_{OUT} = 100-mV step		0.3		ns
	Settling time to 0.1%	V_{OUT} = 2-V step		8		ns
	Settling time to 0.001%	V_{OUT} = 2-V step		3000		ns
	Overshoot/undershoot	V_{OUT} = 2-V step		7%		
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		90		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		60		
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		86		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		64		dBc
e_n	Input-referred voltage noise	f = 1 MHz		3.3		nV/√Hz
Z_{OUT}	Closed-loop output impedance	f = 1 MHz		0.15		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain(1)		60	65		dB
V_{OS}	Input offset voltage(1)	T_A = 25°C	–5	±0.9	5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to +125°C		–2		µV/°C
I_{BN}, I_{BI}	Input bias current(1)	T_A = 25°C	–5	±0.5	5	pA
I_{BOS}	Input offset current(1)	T_A = 25°C	–5	±0.1	5	pA
CMRR	Common-mode rejection ratio(1)	V_{CM} = ±0.5 V	70	84		dB
INPUT						
	Common-mode input resistance			1		GΩ
C_{CM}	Common-mode input capacitance			0.62		pF
	Differential input resistance			1		GΩ
C_{DIFF}	Differential input capacitance			0.2		pF
V_{IH}	Common-mode input voltage (high)(1)	V_{S+} = 3.3 V, CMRR > 66 dB	1.7	1.9		V
V_{IL}	Common-mode input voltage (low)(1)	V_{S+} = 3.3 V, CMRR > 66 dB		0	0.4	V
V_{IH}	Common-mode input voltage (high)(1)	CMRR > 66 dB	3.4	3.6		V
		T_A = –40°C to +125°C, CMRR > 66 dB		3.4		
V_{IL}	Common-mode input voltage (low)(1)	CMRR > 66 dB		0	0.4	V
		T_A = –40°C to +125°C, CMRR > 66 dB		0.35	0.45	

6.5 Electrical Characteristics (continued)

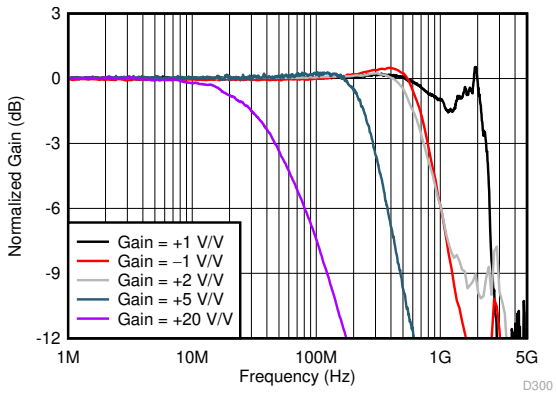
V_{S+} = 5 V, V_{S-} = 0 V, input common-mode biased at midsupply, unity gain configuration, R_L = 200 Ω, output load is referenced to midsupply, and T_A ≈ +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OH}	Output voltage (high)	V_{S+} = 3.3 V, T_A = 25°C	2.3	2.4		V
		TA = 25°C	3.95	4.1		
		T_A = –40°C to +125°C		3.9		
V_{OL}	Output voltage (low)	V_{S+} = 3.3 V, T_A = 25°C		1.05	1.15	V
		T_A = 25°C		1.1	1.15	
		T_A = –40°C to +125°C		1.2		
I_{O_LIN}	Linear output drive (sink and source)(1)	R_L = 10 Ω, A_{OL} > 52 dB	65	76		mA
		T_A = –40°C to +125°C, R_L = 10 Ω, A_{OL} > 52 dB		64		
I_{SC}	Output short-circuit current(1)		85	105		mA
POWER SUPPLY						
I_Q	Quiescent current	V_{S+} = 5 V	18	20.5	24	mA
		V_{S+} = 3.3 V	17.5	20	23.5	
		V_{S+} = 5.25 V	18	21	24	
		T_A = 125°C		24.5		
		T_A = –40°C		18.5		
PSRR+	Positive power-supply rejection ratio(1)		66	74		dB
PSRR–	Negative power-supply rejection ratio(1)		64	72		
POWER DOWN						
	Disable voltage threshold	Amplifier off when < this voltage	0.65	1		V
	Enable voltage threshold	Amplifier on when > this voltage		1.5	1.8	V
	Power-down quiescent current			70	140	µA
	$\overline{PD}$ bias current			70	200	µA
	Turn-on time delay	Time to V_{OUT} = 90% of final value		25		ns
	Turn-off time delay			120		ns

(1) MIN and MAX limits do not apply for bare die.

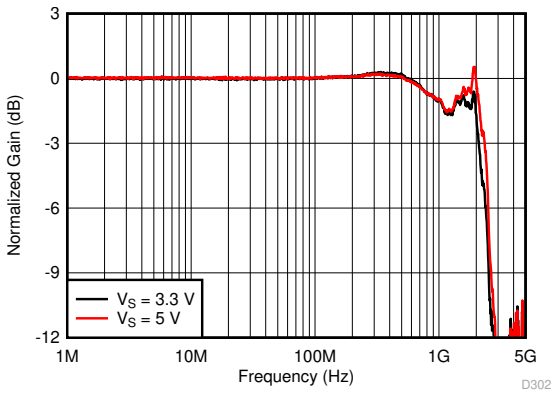
6.6 Typical Characteristics

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



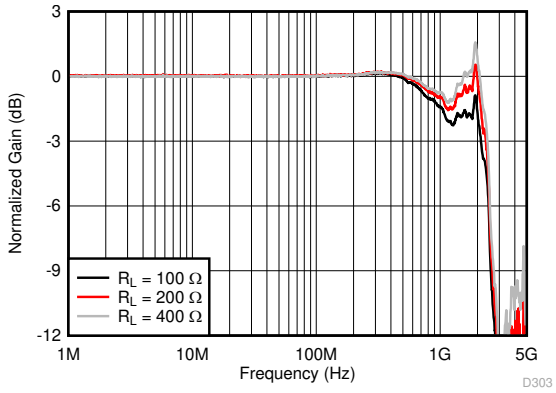
V_{OUT} = 100 mV_{PP}; see Section 7 for circuit configuration

Figure 6-1. Small-Signal Frequency Response vs Gain



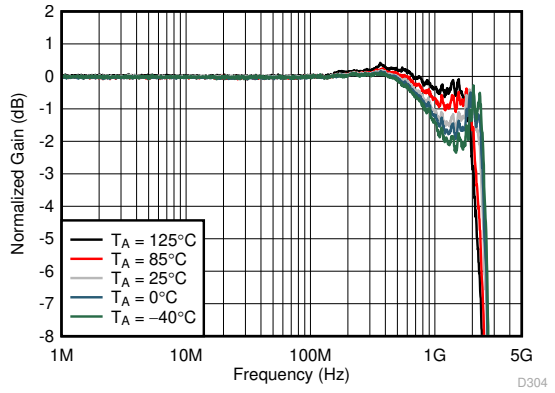
V_{OUT} = 100 mV_{PP}

Figure 6-2. Small-Signal Frequency Response vs Supply Voltage



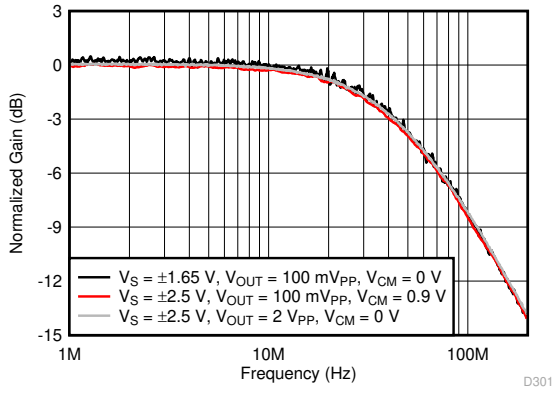
V_{OUT} = 100 mV_{PP}

Figure 6-3. Small-Signal Frequency Response vs Output Load



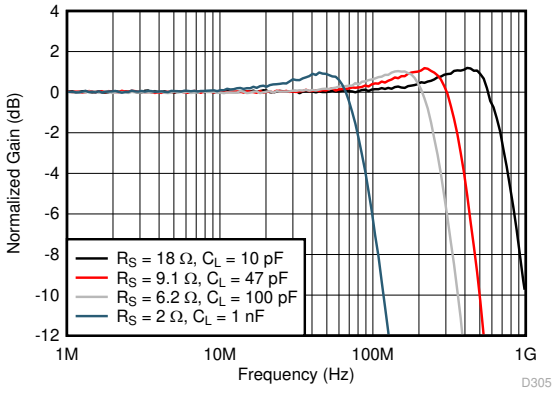
V_{OUT} = 100 mV_{PP}

Figure 6-4. Small-Signal Frequency Response vs Ambient Temperature



Gain = 20 V/V R_F = 453 Ω

Figure 6-5. Frequency Response at Gain = 20 V/V

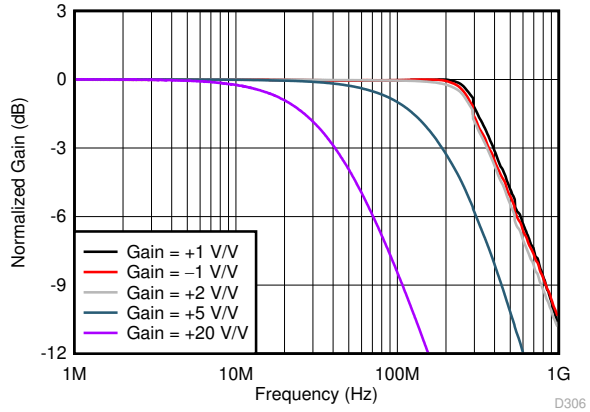


V_{OUT} = 100 mV_{PP}, See Figure 7-4 for circuit configuration

Figure 6-6. Small-Signal Frequency Response vs Capacitive Load

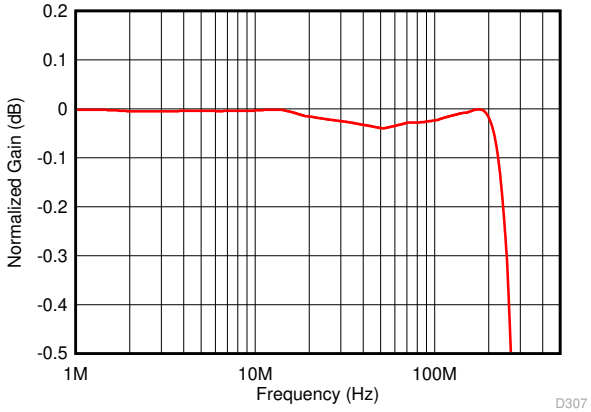
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



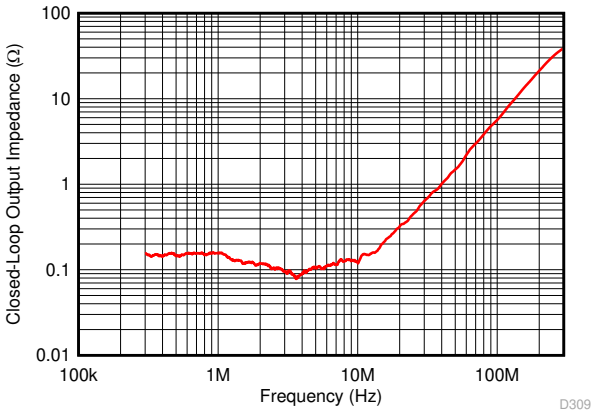
V_{OUT} = 2 V_{PP}

Figure 6-7. Large-Signal Frequency Response vs Gain



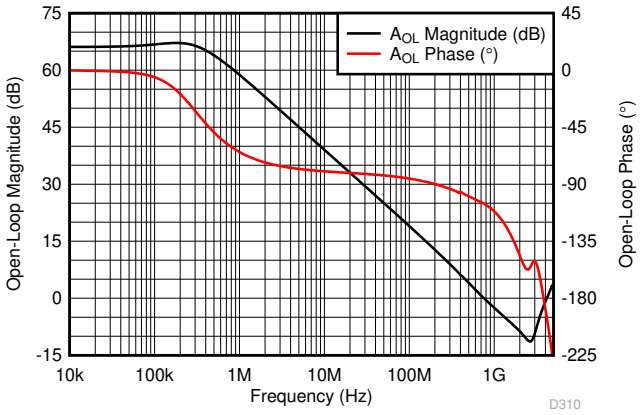
V_{OUT} = 2 V_{PP}

Figure 6-8. Large-Signal Response for 0.1-dB Gain Flatness



Small-signal response

Figure 6-9. Closed-Loop Output Impedance vs Frequency



Small-signal response

Figure 6-10. Open-Loop Magnitude and Phase vs Frequency

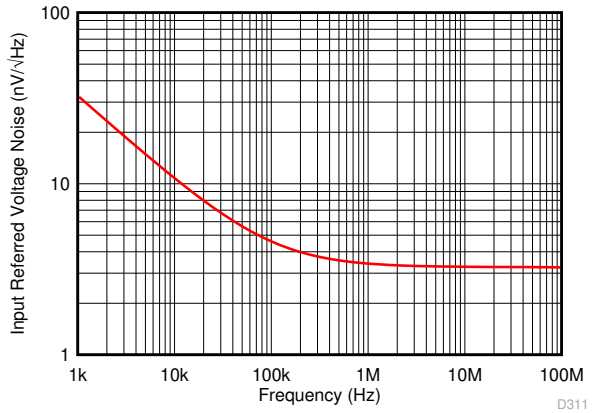
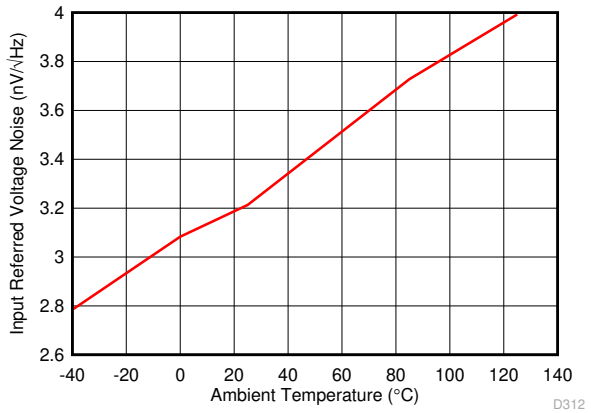


Figure 6-11. Voltage Noise Density vs Frequency



Frequency 10 MHz

Figure 6-12. Voltage Noise Density vs Ambient Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)

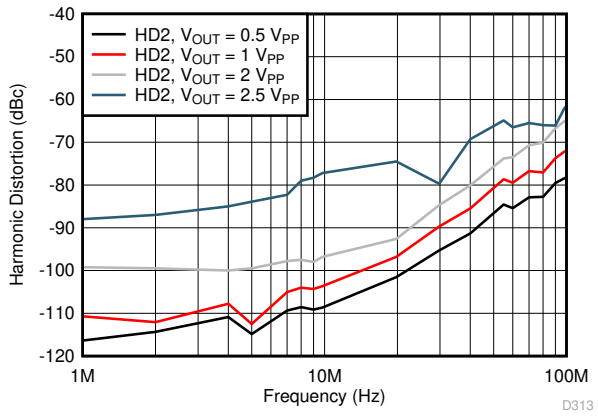


Figure 6-13. Harmonic Distortion (HD2) vs Output Swing

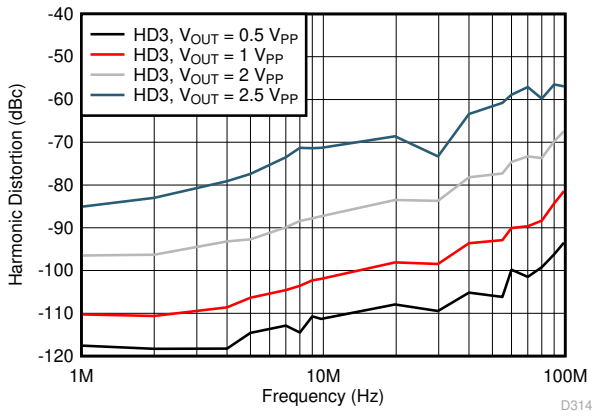


Figure 6-14. Harmonic Distortion (HD3) vs Output Swing

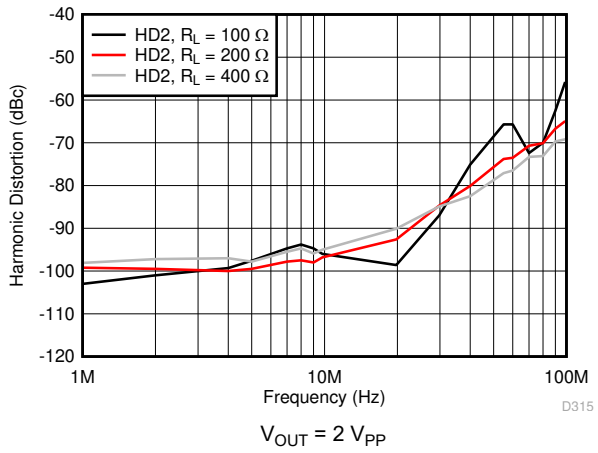


Figure 6-15. Harmonic Distortion (HD2) vs Output Load

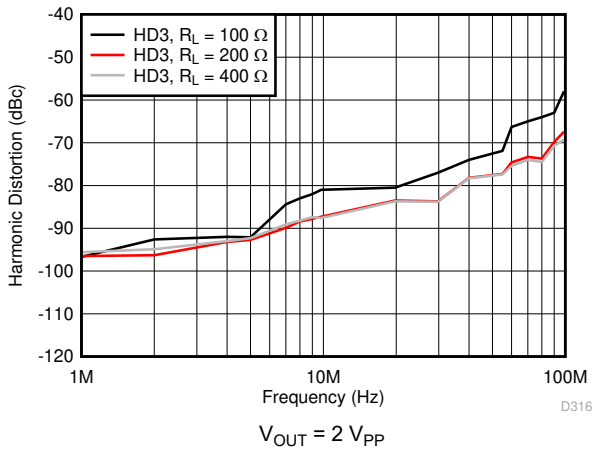


Figure 6-16. Harmonic Distortion (HD3) vs Output Load

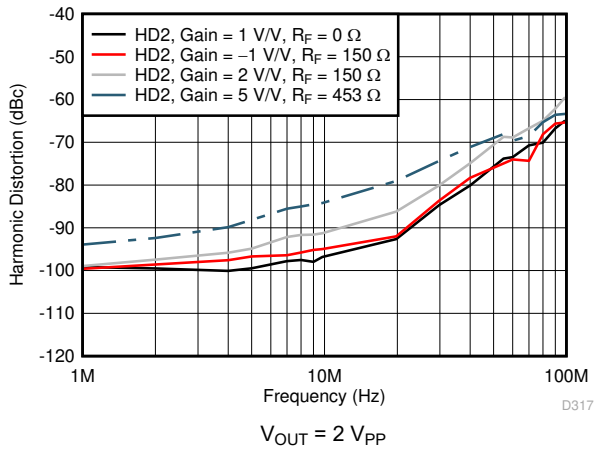


Figure 6-17. Harmonic Distortion (HD2) vs Gain

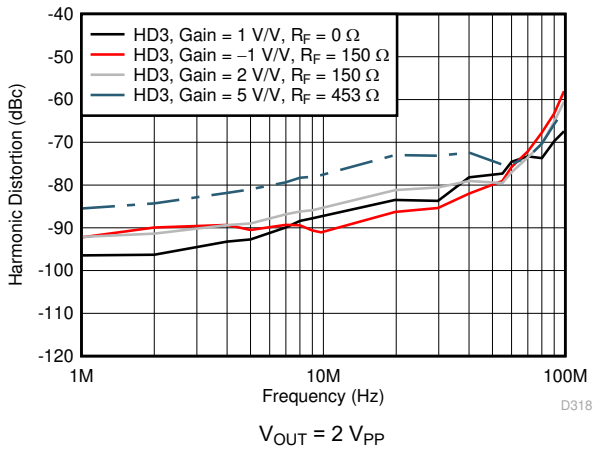
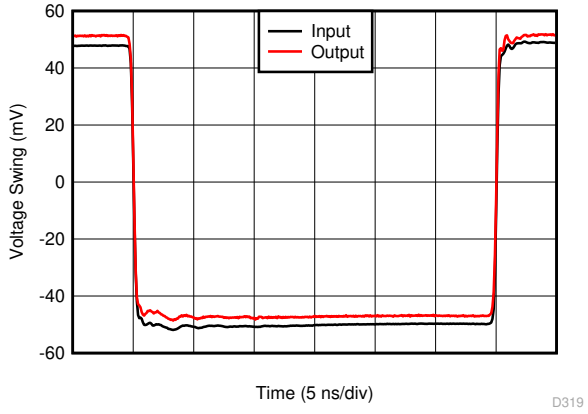


Figure 6-18. Harmonic Distortion (HD3) vs Gain

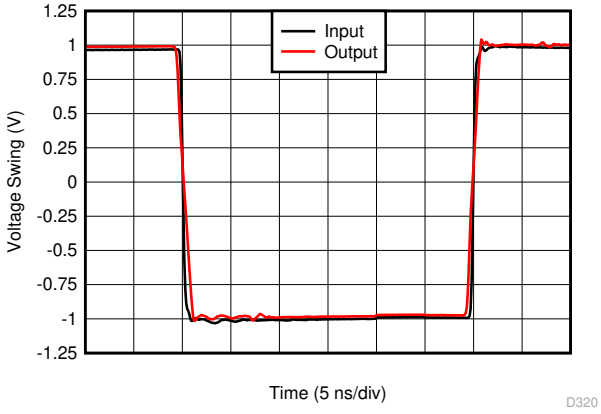
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



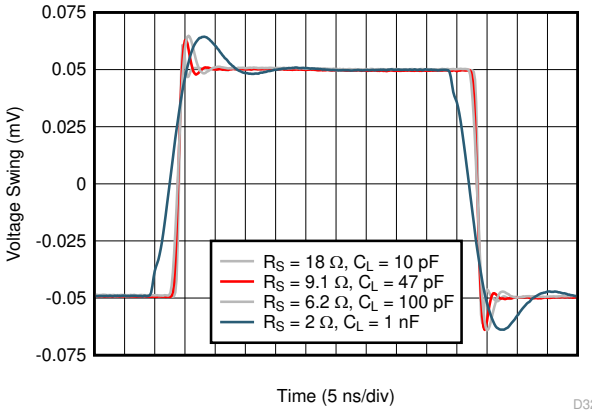
Average rise-and-fall time (10%–90%) = 450 ps

Figure 6-19. Small-Signal Transient Response



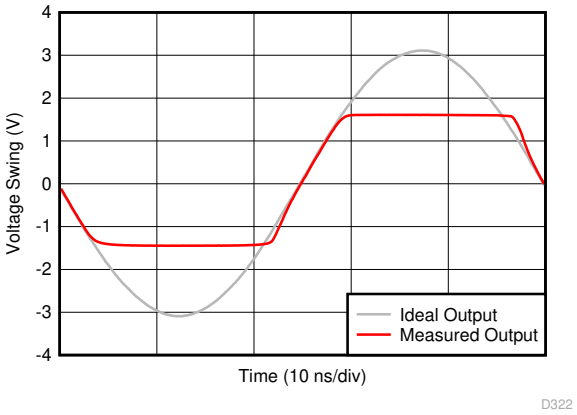
Slew rate: falling = 1160 V/µs, rising = 1400 V/µs

Figure 6-20. Large-Signal Transient Response



See Figure 7-4 for circuit configuration

Figure 6-21. Small-Signal Transient Response vs Capacitive Load



Gain = 5 V/V, R_F = 453 Ω, 2 × output overdrive

Figure 6-22. Output Overload Response

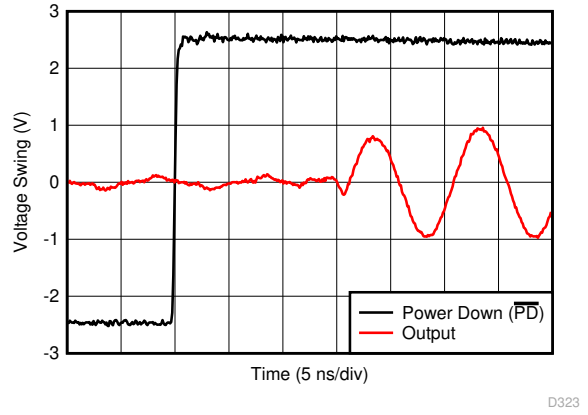


Figure 6-23. Turnon Transient Response

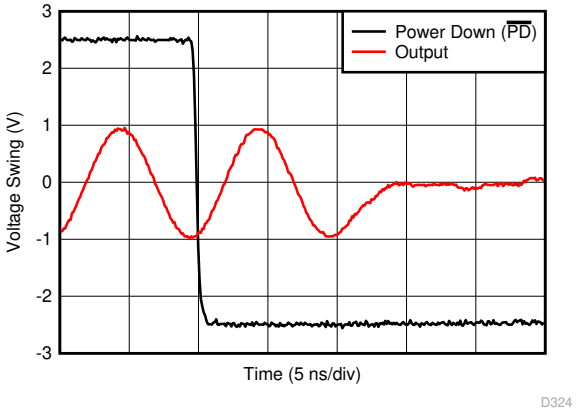
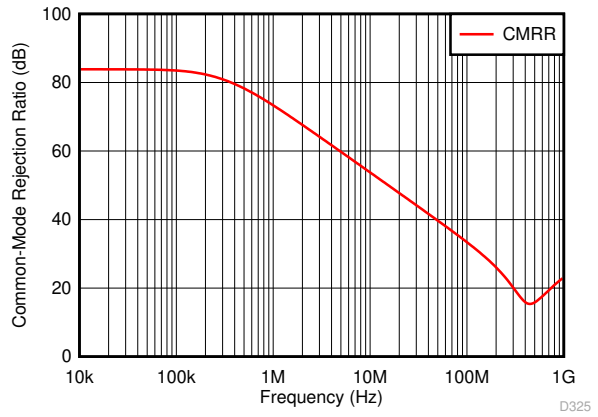


Figure 6-24. Turnoff Transient Response

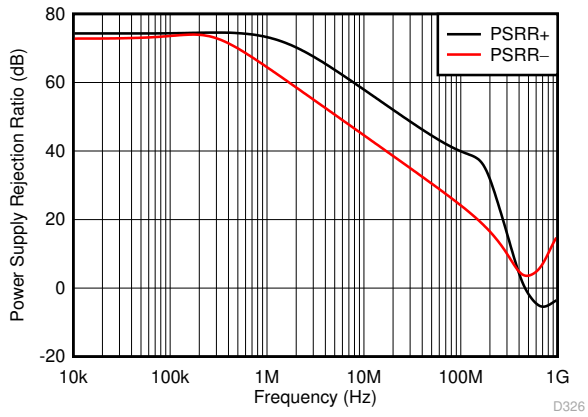
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



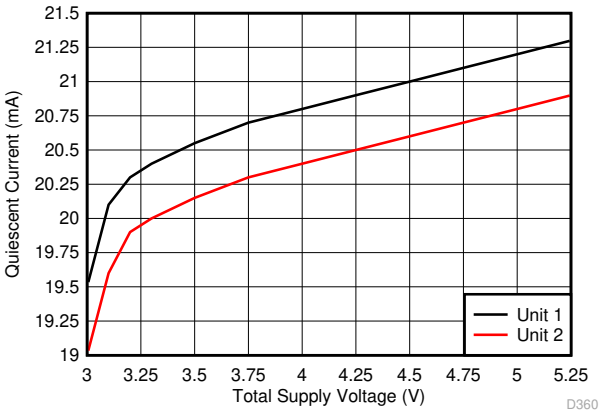
Small-signal response

Figure 6-25. Common-Mode Rejection Ratio vs Frequency



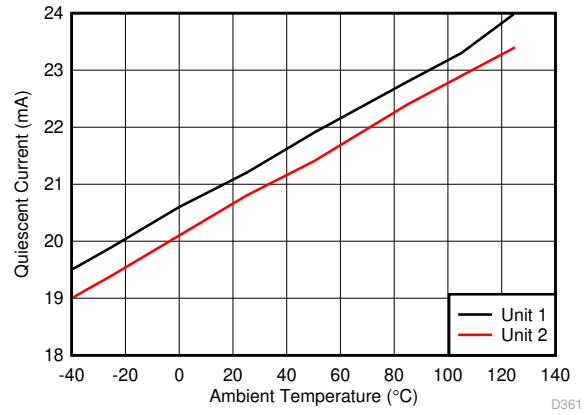
Small-signal response

Figure 6-26. Power Supply Rejection Ratio vs Frequency



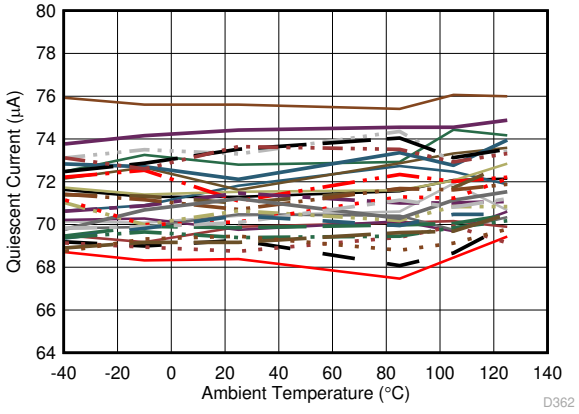
2 typical units

Figure 6-27. Quiescent Current vs Supply Voltage



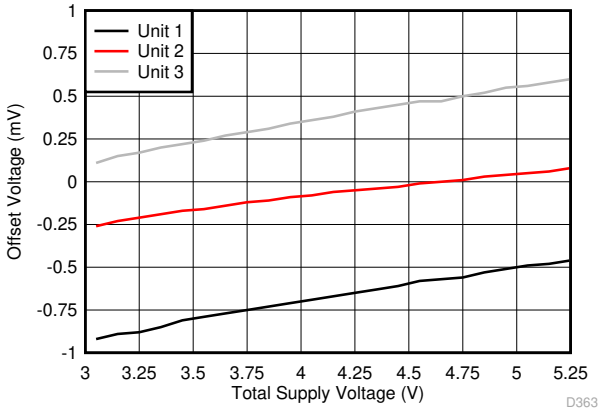
V_S = 5 V 2 typical units

Figure 6-28. Quiescent Current vs Ambient Temperature



32 units tested

Figure 6-29. Quiescent Current (Amplifier Disabled) vs Ambient Temperature



3 typical units

Figure 6-30. Offset Voltage vs Supply Voltage

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)

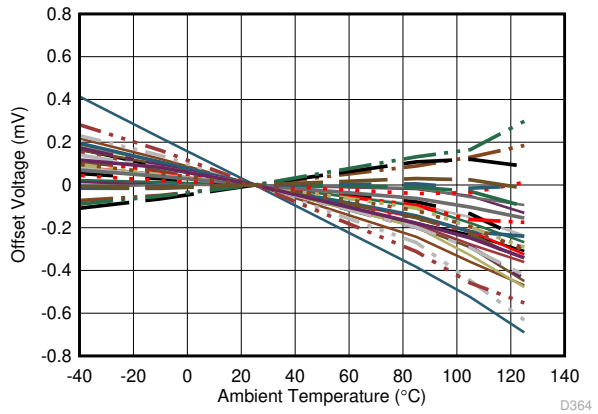


Figure 6-31. Offset Voltage vs Ambient Temperature

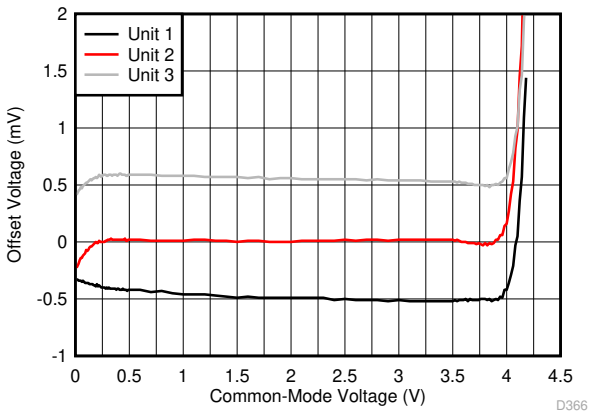


Figure 6-32. Offset Voltage vs Input Common-Mode Voltage

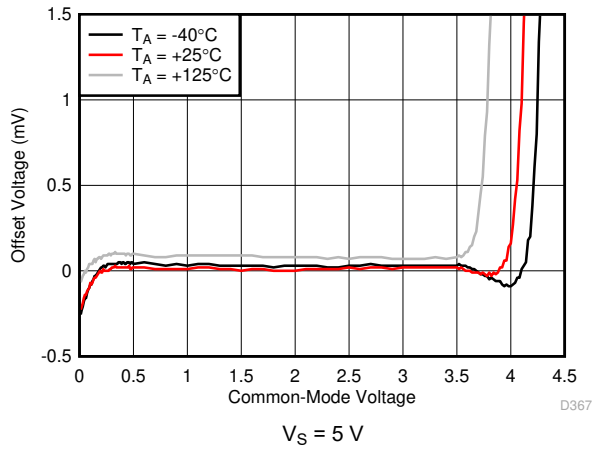


Figure 6-33. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature

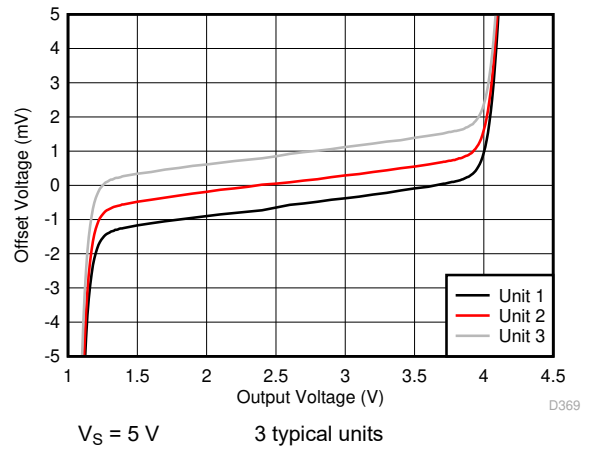


Figure 6-34. Offset Voltage vs Output Swing

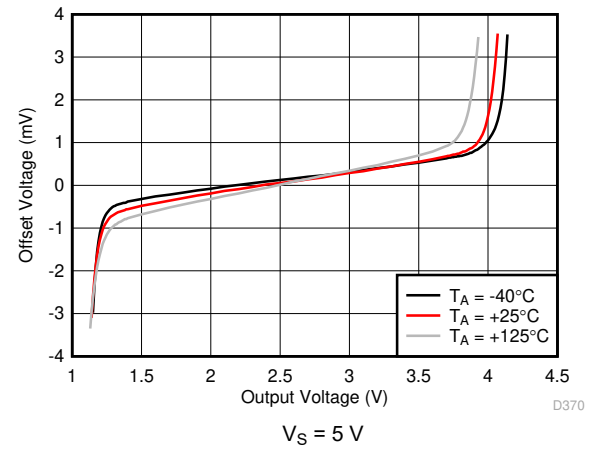


Figure 6-35. Offset Voltage vs Output Swing vs Ambient Temperature

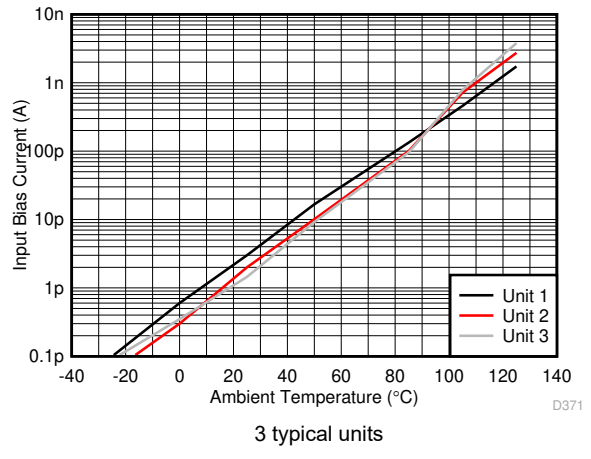
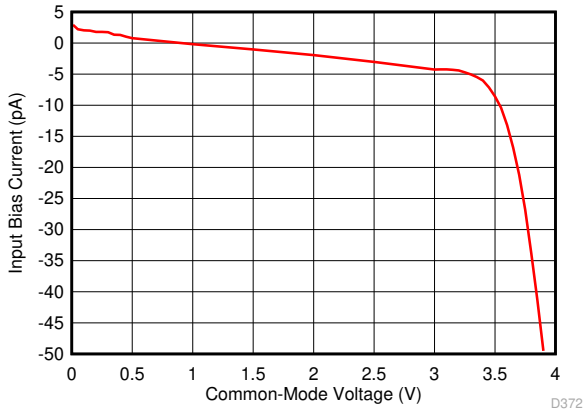


Figure 6-36. Input Bias Current vs Ambient Temperature

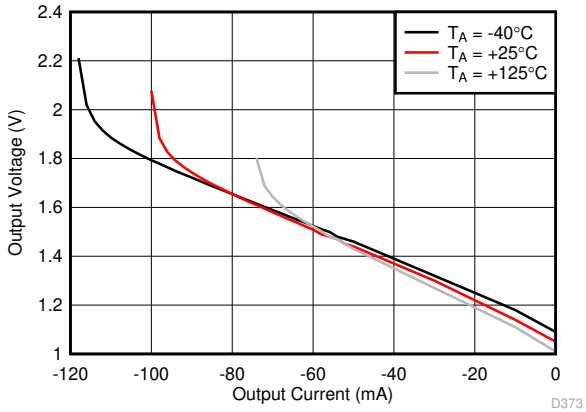
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



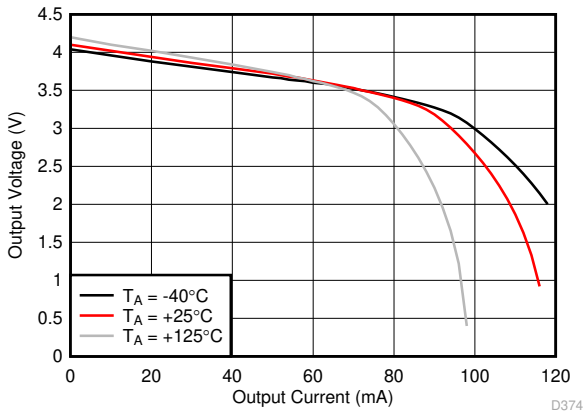
V_S = 5 V

Figure 6-37. Input Bias Current vs Input Common-Mode Voltage



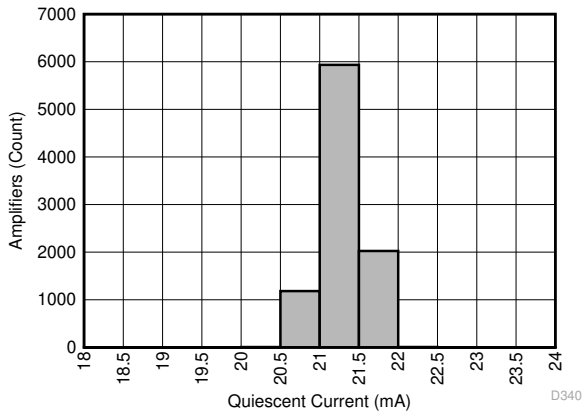
V_S = 5 V

Figure 6-38. Output Swing vs Sinking Current



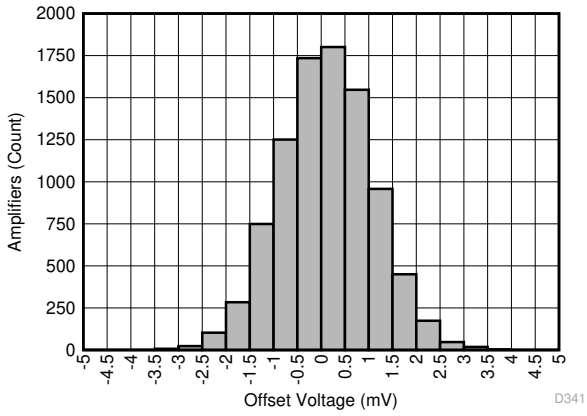
V_S = 5 V

Figure 6-39. Output Swing vs Sourcing Current



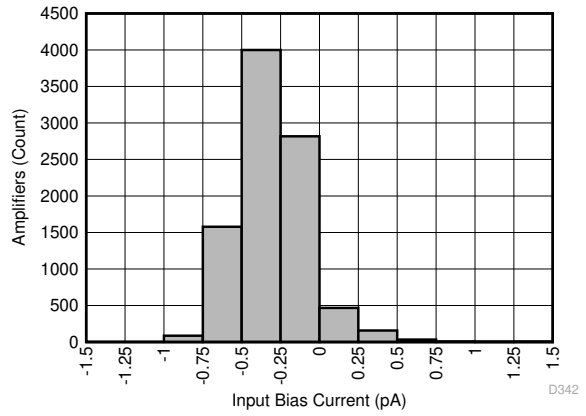
μ = 20.8 mA σ = 0.25 mA 9150 units tested

Figure 6-40. Quiescent Current Distribution



μ = –0.38 mV σ = 0.97 mV 9150 units tested

Figure 6-41. Offset Voltage Distribution



μ = –0.55 pA σ = 0.23 pA 9150 units tested

Figure 6-42. Input Bias Current Distribution

7 Parameter Measurement Information

The various test setup configurations for the OPA859 are shown in the following figures. When configuring the OPA859 as a noninverting amplifier in gains less than 3 V/V, set R_F = 150 Ω. When configuring the OPA859 as a noninverting amplifier in gains of 4 V/V and greater, set R_F = 453 Ω.

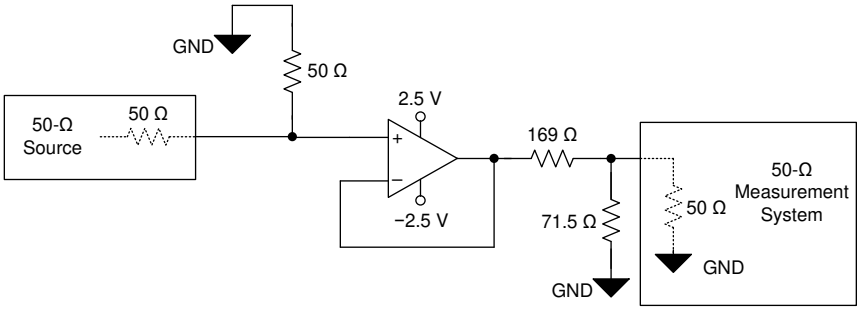
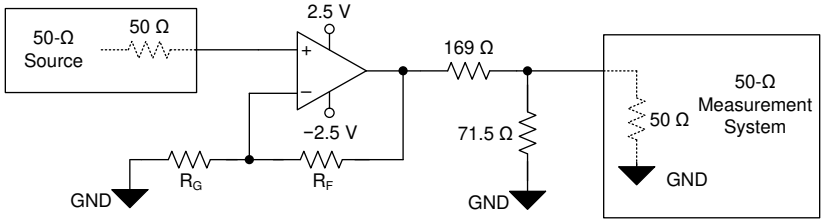


Figure 7-1. Unity-Gain Buffer Configuration



R_G values depend on gain configuration

Figure 7-2. Noninverting Configuration

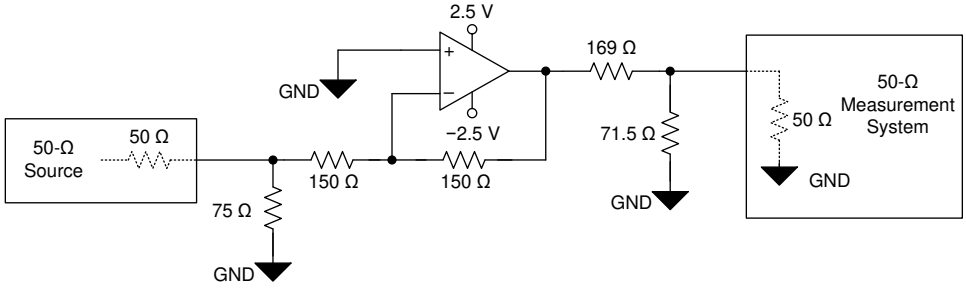


Figure 7-3. Inverting Configuration (Gain = –1 V/V)

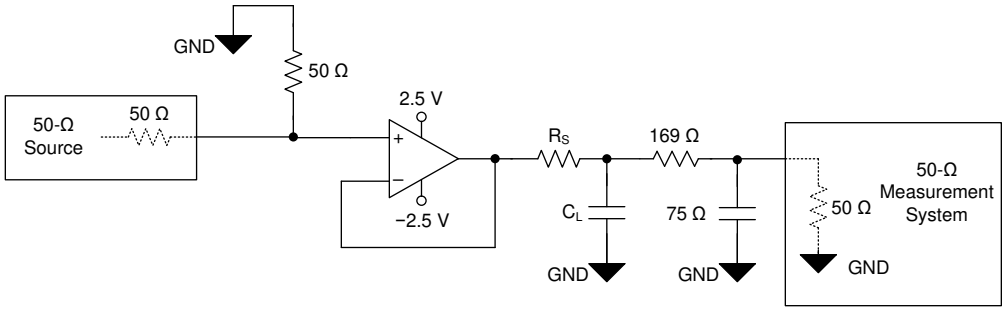


Figure 7-4. Capacitive Load Driver Configuration

8 Detailed Description

8.1 Overview

The ultra-wide, 900-MHz gain bandwidth product (GBWP) of the OPA859, combined with the broadband voltage noise of 3.3 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA859 combines multiple features to optimize dynamic performance. In addition to the wide small-signal bandwidth, the OPA859 has 400 MHz of large-signal bandwidth (V_{OUT} = 2 V_{PP}), and a slew rate of 1150 V/µs.

8.2 Functional Block Diagram

The OPA859 is a classic voltage-feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, such as the two basic options in Figure 8-1 and Figure 8-2. The dc operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

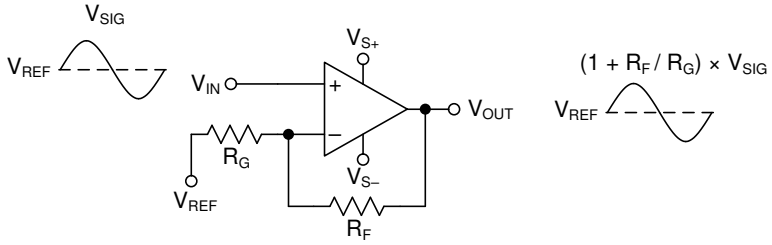


Figure 8-1. Noninverting Amplifier

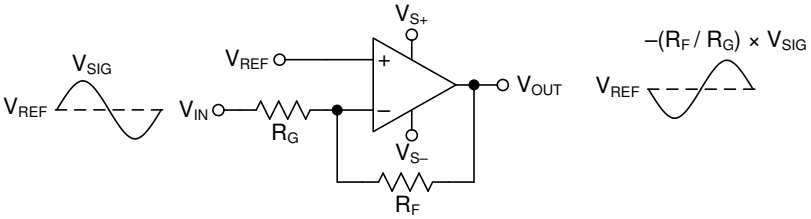


Figure 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA859 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as Figure 8-3 shows. There are two anti-parallel diodes between the inputs of the amplifier that clamp the inputs during an over-range or fault condition.

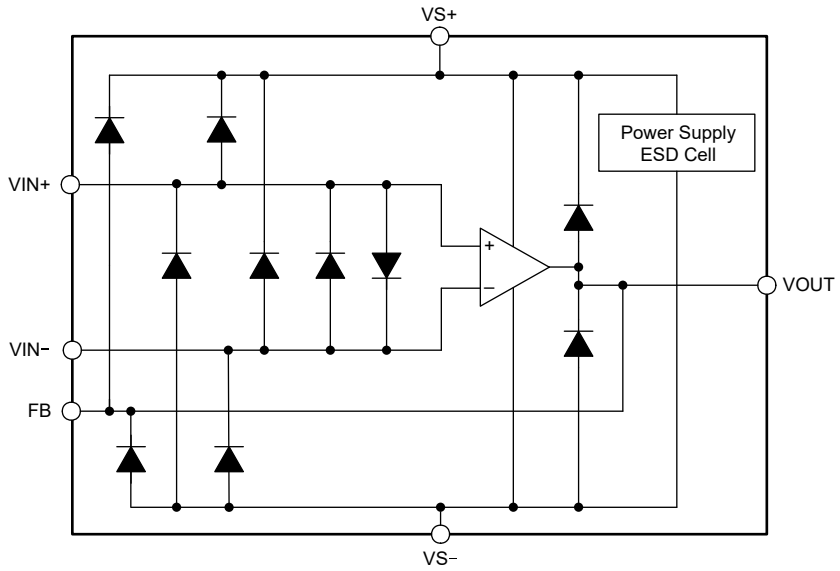


Figure 8-3. Internal ESD Structure

8.3.2 Feedback Pin

The OPA859 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see Figure 8-4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

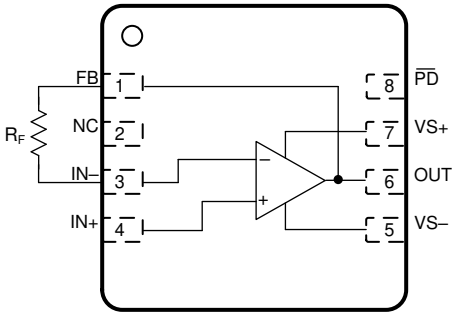


Figure 8-4. R_F Connection Between FB and IN– Pins

8.3.3 Wide Gain-Bandwidth Product

Figure 6-10 shows the open-loop magnitude and phase response of the OPA859. Calculate the gain bandwidth product of any op amp by determining the frequency at which the A_{OL} is 40 dB and multiplying that frequency by a factor of 100. The open-loop response shows the OPA859 to have approximately 63° of phase-margin when configured as a unity-gain buffer.

Figure 8-5 shows the open-loop magnitude (A_{OL}) of the OPA859 as a function of temperature. The results show approximately 5° of phase-margin variation over the entire temperature range. Semiconductor process variation is the naturally occurring variation in the attributes of a transistor (Early-voltage, β, channel-length, and width) and other passive elements (resistors and capacitors) when fabricated into an integrated circuit. The process variation can occur across devices on a single wafer or across devices over multiple wafer lots over time. Typically the variation across a single wafer is tightly controlled. Figure 8-6 shows the A_{OL} magnitude of the OPA859 as a function of process variation over time. The results show the A_{OL} curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results show less than 2° of phase-margin difference within a standard deviation of process variation when the amplifier is configured as a unity-gain buffer.

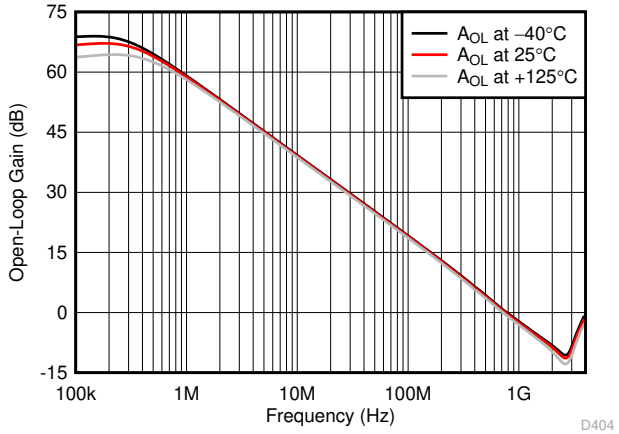


Figure 8-5. Open-Loop Gain vs Temperature

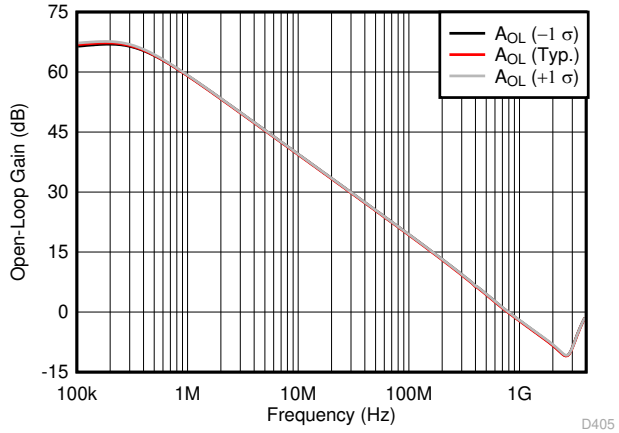


Figure 8-6. Open-Loop Gain vs Process Variation

8.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA859 features a high slew rate of 1150 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub-10-ns pulses, such as optical time-domain reflectometry (OTDR) and LIDAR. The high slew rate of the OPA859 implies that the device accurately reproduces a 2-V, sub-ns pulse edge; see also Figure 6-20. The wide bandwidth and slew rate make the OPA859 an excellent amplifier for high-speed signal-chain front ends.

Figure 8-7 shows the open-loop output impedance of the OPA859 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA859 is limited to approximately 3 V. The OPA859 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA859 output swing range coupled with the class-leading voltage noise specification for a CMOS amplifier maximizes the overall dynamic range of the signal chain.

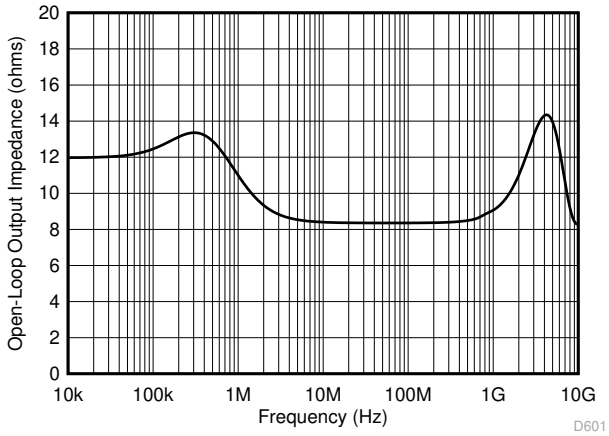


Figure 8-7. Open-Loop Output Impedance (Z_{OL}) vs Frequency

8.3.5 Current Noise

The input impedance of CMOS and JFET input amplifiers at low frequencies exceed several GΩs. However, at higher frequencies, the transistors parasitic capacitance to the drain, source, and substrate reduces the impedance. The high impedance at low frequencies eliminates any bias current and the associated shot noise. At higher frequencies, the input current noise increases (see Figure 8-8) as a result of capacitive coupling between the CMOS gate oxide and the underlying transistor channel. This phenomenon is a natural artifact of the construction of the transistor and is unavoidable.

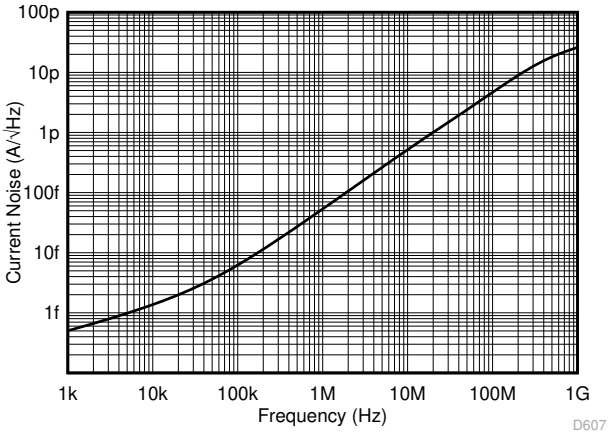


Figure 8-8. Input Current Noise (I_{BN} and I_{BI}) vs Frequency

8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA859 can be configured with single-sided supplies or split supplies; see also Figure 9-4 . Split-supply operation using balanced supplies with the input common-mode set to ground can help ease lab testing (because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground). In split-supply operation, connect the thermal pad to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA859 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the dc input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at midsupply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, connect the thermal pad to ground.

8.4.2 Power-Down Mode

The OPA859 features a power-down mode to reduce the quiescent current to conserve power. and show the OPA859 transient response as the $\overline{PD}$ pin toggles between the disabled and enabled states.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable threshold voltage is 0.65 V and the enable threshold voltage is 1.8 V. If the amplifier is configured with ±1.65-V supplies, then the disable threshold voltage is –1 V and the enable threshold voltage is 0.15 V. If the amplifier is configured with ±2.5-V supplies, then the disable threshold voltage is –1.85 V and the enable threshold voltage is –0.7 V.

Figure 8-9 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept down from the enabled to the disabled state. Similarly, Figure 8-10 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept up from the disabled to the enabled state. The small difference in the switching thresholds between the down sweep and up sweep is due to the hysteresis designed into the amplifier to increase noise immunity on $\overline{PD}$.

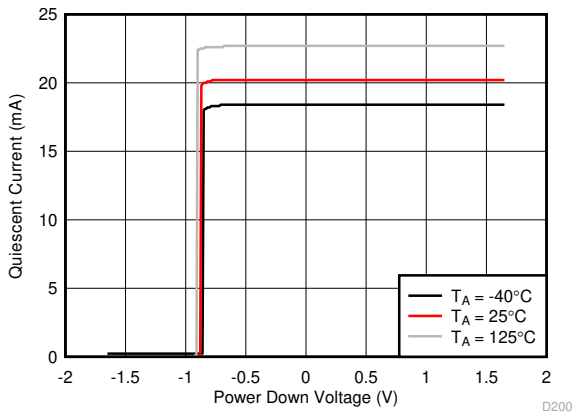


Figure 8-9. Switching Threshold ($\overline{PD}$ Pin Swept From High to Low)

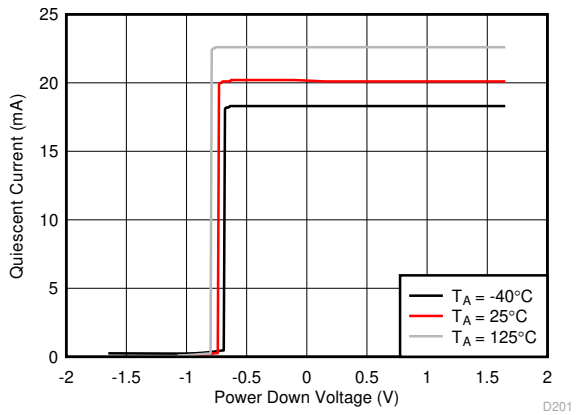


Figure 8-10. Switching Threshold ($\overline{PD}$ Pin Swept From Low to High)

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA859 uses internal, back-to-back protection diodes between the inverting and noninverting input pins; see also Figure 8-3. In the power-down state, if the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the noninverting input pin and the output pin.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPA859 offers high input impedance, very high-bandwidth, high slew-rate, low noise, and better than –60 dBc of distortion performance at frequencies up to 100 MHz. These features make this device an excellent front-end buffer in high-speed data acquisition systems. The wide bandwidth also makes this amplifier an excellent choice for high-gain active filter systems.

9.2 Typical Applications

9.2.1 TIA in an Optical Front-End System

Figure 9-1 shows the OPA859 configured as a transimpedance amplifier (U1) in a wide-bandwidth, optical front-end system. A second OPA859 configured as a unity-gain buffer (U2) sets a dc offset voltage to the THS4520. The THS4520 is used to convert the single-ended transimpedance output of the OPA859 into a differential output signal. The THS4520 drives the input of the ADS54J64, 14-bit, 1-GSPS analog-to-digital converter (ADC) that digitizes the analog signal.

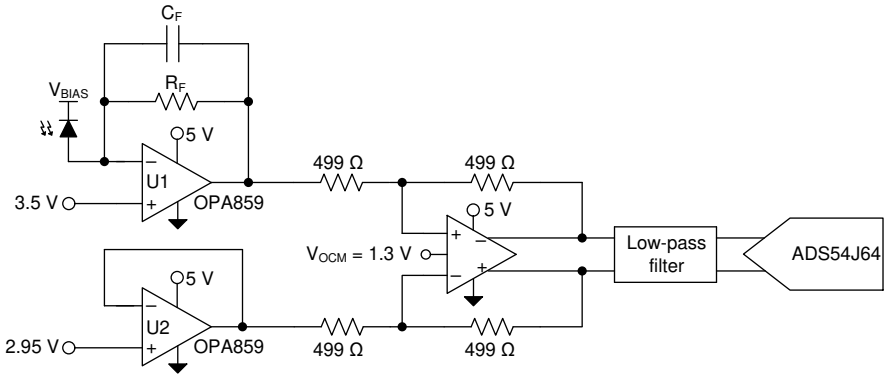


Figure 9-1. OPA859 as Both a TIA and a Buffer in an Optical Front-End System

9.2.1.1 Design Requirements

The objective is to design a low noise, wideband optical front-end system using the OPA859 as a transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: 5 V
- TIA common-mode voltage: 3.5 V
- THS4520 gain: 1 V/V
- ADC input common-mode voltage: 1.1 V_{PP}
- ADC analog differential input range: 1.1 V_{PP}

9.2.1.2 Detailed Design Procedure

The OPA859 meets the growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance (C_{IN}). This total includes the photodiode capacitance, the input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP).
3. The transimpedance gain (R_F).

Figure 9-1 shows the OPA859 configured as a transimpedance amplifier (TIA), with the avalanche photodiode (APD) reverse biased so that the APD cathode is tied to a large positive bias voltage. In this configuration, the APD sources current into the op-amp feedback loop so that the output swings in a negative direction relative to the input common-mode voltage. To maximize the output swing in the negative direction, the common-mode voltage of the OPA859 is set close to the positive limit; only 1.5 V from the positive supply rail. The feedback resistance (R_F) and the input capacitance (C_{IN}) form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted into the noise gain transfer function by adding the feedback capacitor (C_F).

The *Transimpedance Considerations for High-Speed Amplifiers Application Report* discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The bandwidth and compensation equations from the application report are available in an Excel® calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator.

The equations and calculators in the referenced application report and blog posts are used to model the bandwidth (f_{-3dB}) and noise (I_{RN}) performance of the OPA859 configured as a TIA. The resultant performance is shown in Figure 9-2 and Figure 9-3. The left-side Y-axis shows the closed-loop bandwidth performance, whereas the right side of the graph shows the integrated input-referred noise. The noise bandwidth to calculate I_{RN} for a fixed R_F and C_{PD} is set equal to the f_{-3dB} frequency. Figure 9-2 shows the amplifier performance as a function of photodiode capacitance (C_{PD}) for R_F = 10 kΩ and 20 kΩ. Increasing C_{PD} decreases the closed-loop bandwidth. To maximize bandwidth, make sure to reduce any stray parasitic capacitance from the PCB. The OPA859 is designed with 0.8 pF of total input capacitance to minimize the effect of stray capacitance on system performance. Figure 9-3 shows the amplifier performance as a function of R_F for C_{PD} = 1 pF and 2 pF. Increasing R_F results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage. Increasing R_F by a factor of X increases the signal level by X, but only increases the resistor noise contribution by √X, thereby improving SNR.

The OPA859 configured as a unity-gain buffer drives a dc offset voltage of 2.95 V into the lower half of the THS4520. To maximize the dynamic range of the ADC, the two OPA859 amplifiers drive a differential common-mode of 3.5 V and 2.95 V into the THS4520. The dc offset voltage of the buffer amplifier can be derived using Equation 1.

$$V_{BUF\_DC} = V_{TIA\_CM} - \left(\frac{1}{2} \times \frac{V_{ADC\_DIFF\_IN}}{\left(\frac{R_F}{R_G} \right)} \right) \quad (1)$$

where

- V_{TIA_CM} is the common-mode voltage of the TIA (3.5 V)
- $V_{ADC\_DIFF\_IN}$ is the differential input voltage range of the ADC (1.1 V_{PP})
- R_F and R_G are the feedback resistance (499 Ω) and gain resistance (499 Ω) of the THS4520 differential amplifier

The low-pass filter between the THS4520 and the ADC54J64 minimizes high-frequency noise and maximizes SNR. The ADC54J64 has an internal buffer that isolates the output of the THS4520 from the ADC sampling-capacitor input, so a traditional charge bucket filter is not required.

9.2.1.3 Application Curves

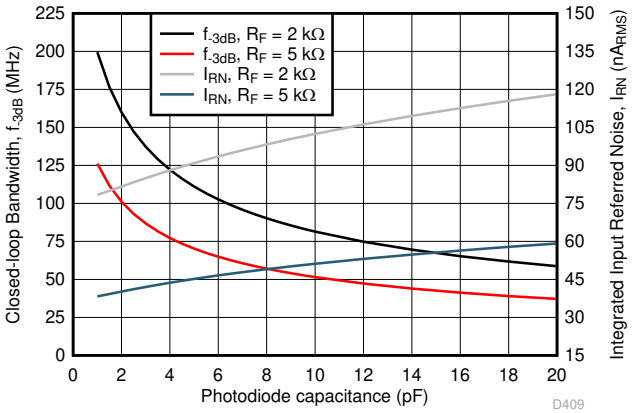


Figure 9-2. Bandwidth and Noise vs Photodiode Capacitance

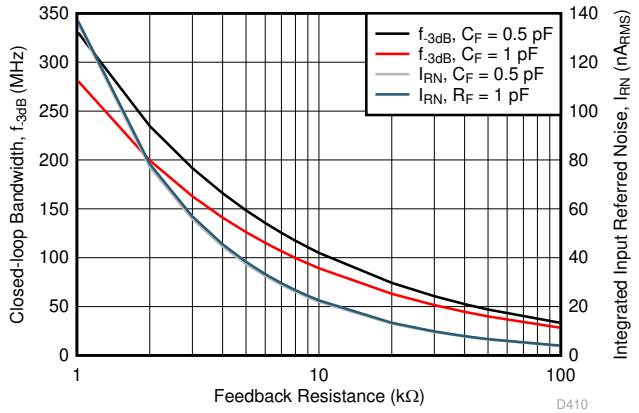


Figure 9-3. Bandwidth and Noise vs Feedback Resistance

9.3 Power Supply Recommendations

The OPA859 operates on supplies from 3.3 V to 5.25 V. The OPA859 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA859 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

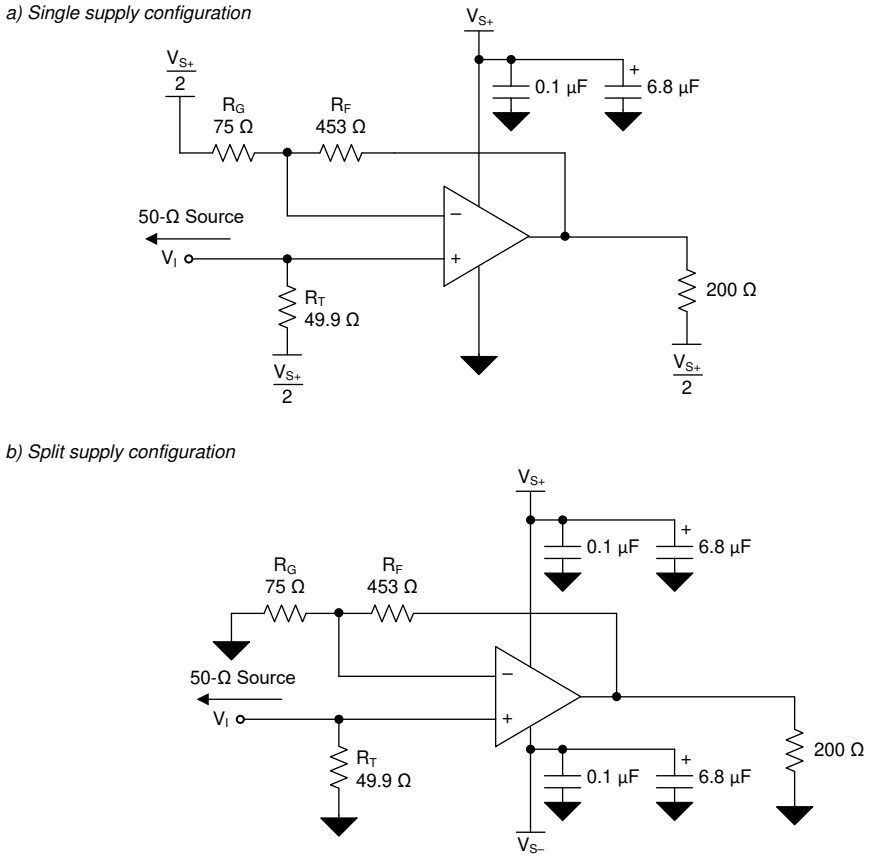


Figure 9-4. Split and Single Supply Circuit Configuration , Gain = 7 V/V

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA859 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA859.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wire-wound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA859 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

9.4.2 Layout Example

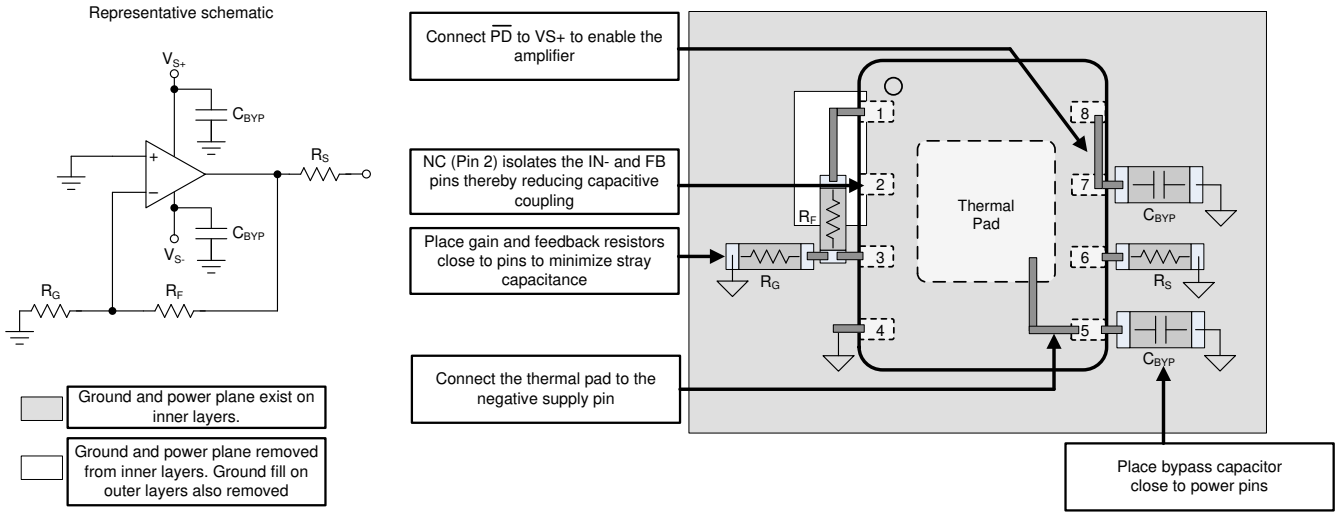


Figure 9-5. Layout Recommendation

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- *LIDAR Pulsed Time of Flight Reference Design*
- *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters*
- *Wide Bandwidth Optical Front-end Reference Design*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA858EVM user's guide*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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Excel® is a registered trademark of Microsoft Corporation.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision * (September 2018) to Revision A (May 2025)	Page
• Added bare die package and associated content to data sheet	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA859IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	859
OPA859IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	859
OPA859IDSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	859
OPA859IDSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	859
OPA859YR	Active	Production	DIESALE (Y) | 0	3000 | LARGE T&R	Yes	Call TI	N/A for Pkg Type	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA859 :

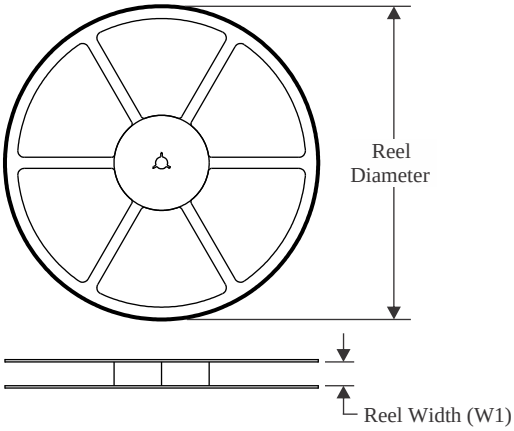
- Automotive : OPA859-Q1

NOTE: Qualified Version Definitions:

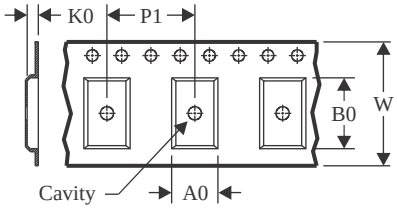
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

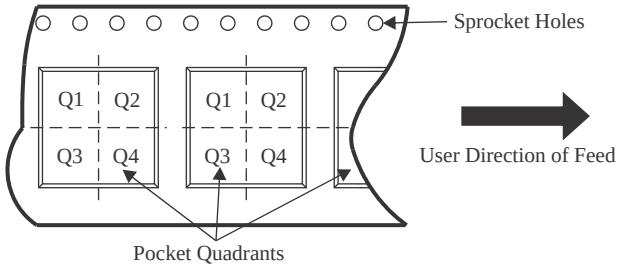


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

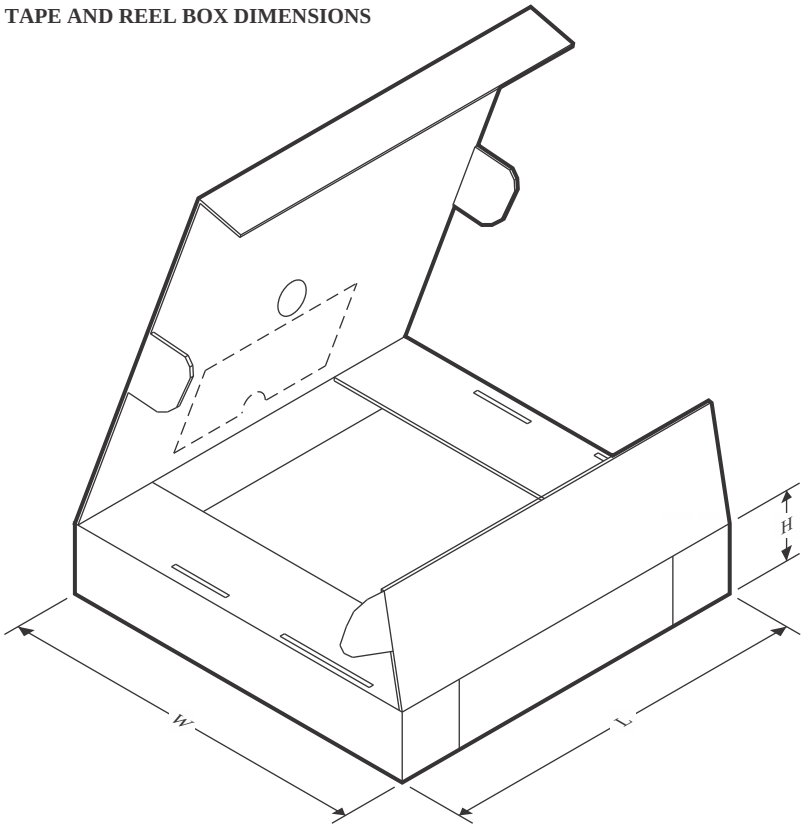
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA859IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA859IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA859YR	DIESALE	Y	0	3000	180.0	8.4	0.74	0.78	0.45	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA859IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA859IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
OPA859YR	DIESALE	Y	0	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

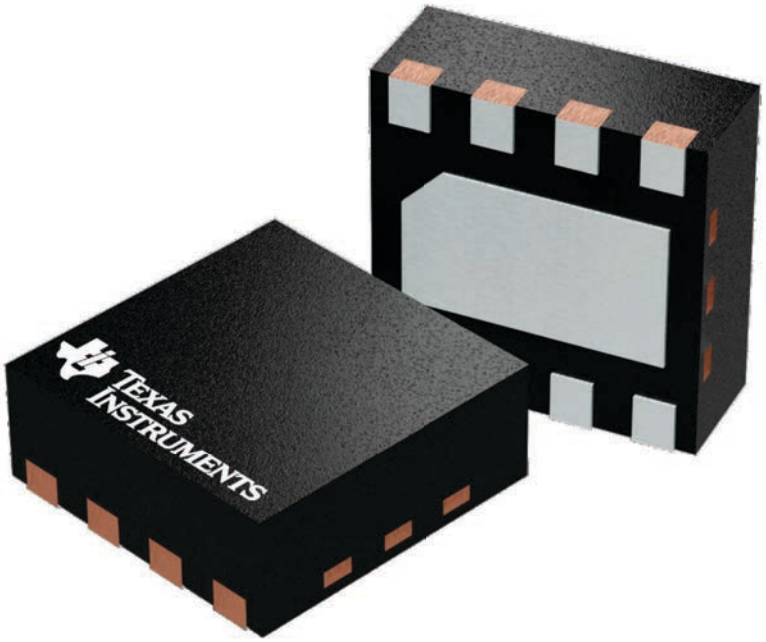
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



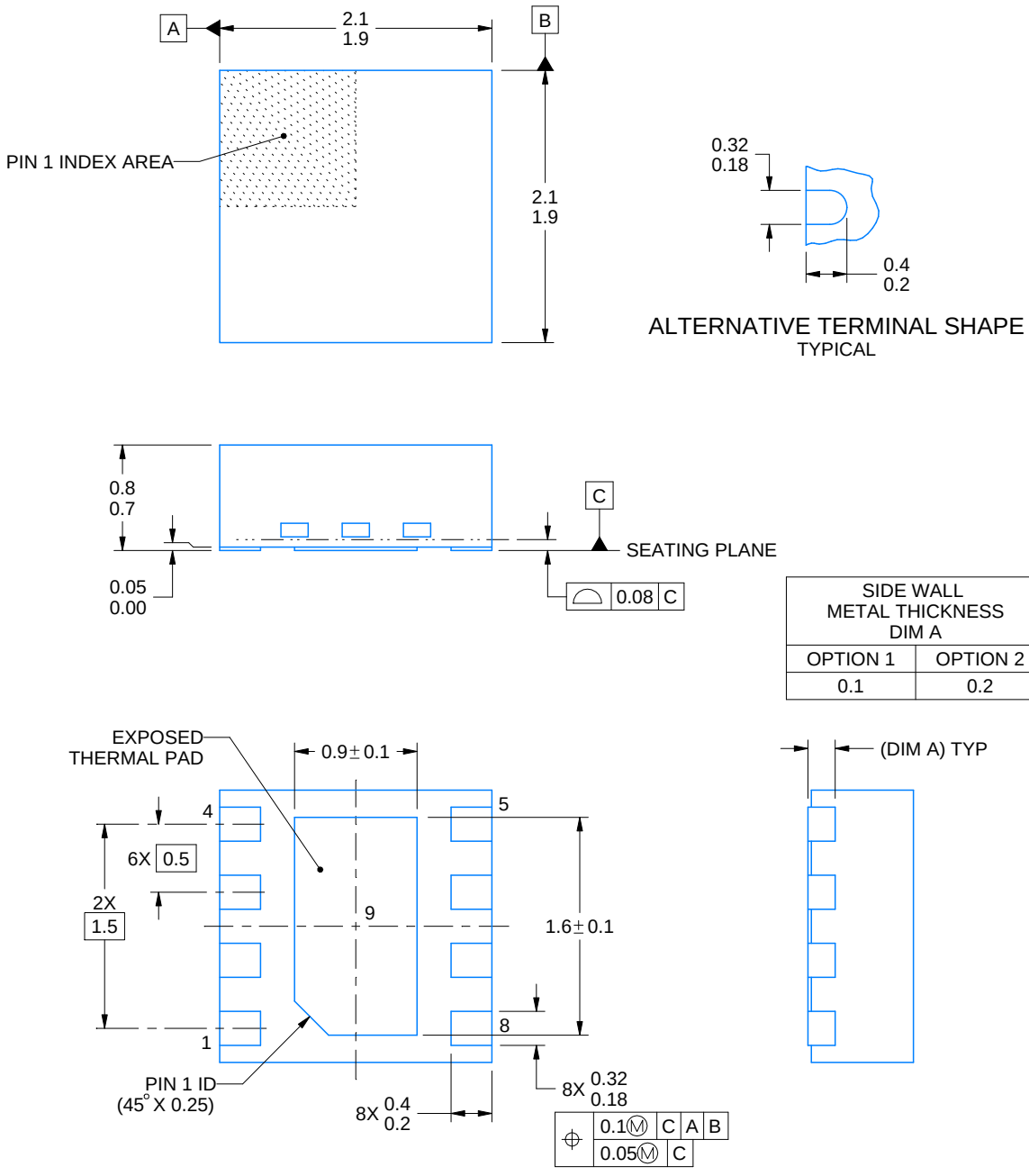
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

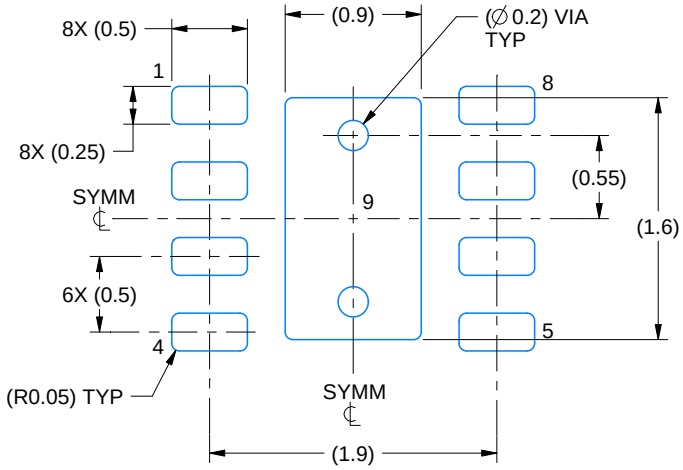
PLASTIC SMALL OUTLINE - NO LEAD



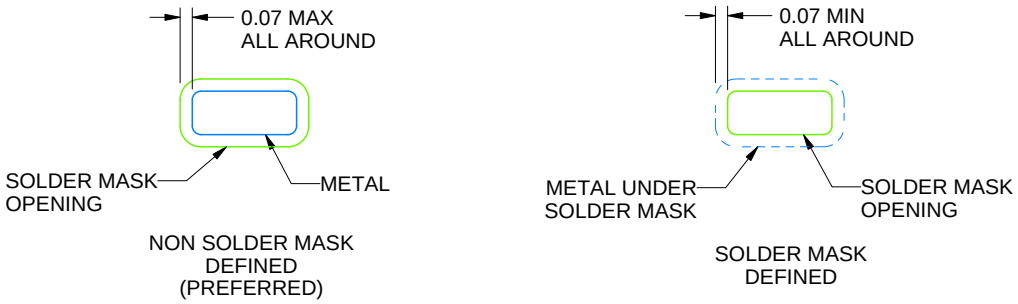
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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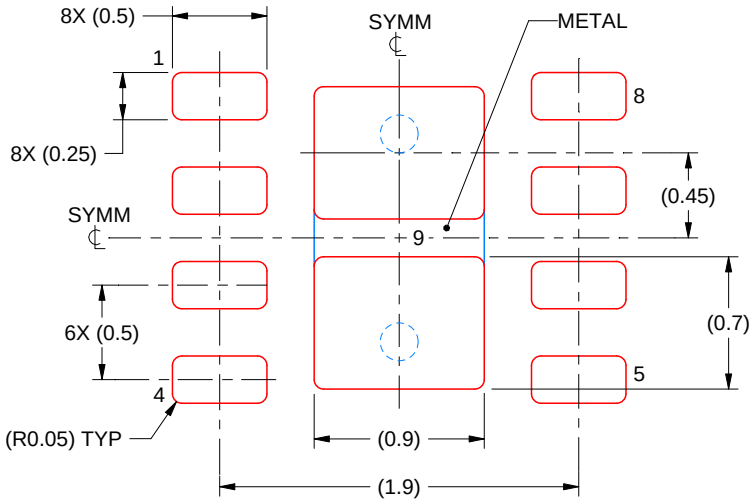
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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