2.2V to 5.5V, Low-Power, 12-Bit, 100kSPS, 8-Channel Data Acquisition System with PGA and SPI™ Interface

Check for Samples: ADS8201

FEATURES

- **Low-Power, Flexible Supply Range:**
  - **2.2V to 5.5V Analog Supply**
  - **1.32mW (100kHz, +VA = 2.2V, +VD = 2.2V)**
  - **4.5mW (100kHz, +VA = 5V, +VD = 5V)**
- **Up to 100kSPS Throughput Rate**
- **Excellent DC Performance:**
  - **±0.5 LSB typ, ±1.5 LSB max INL**
  - **±0.5 LSB typ, ±1.0 LSB max DNL**
  - **±6 LSB Offset Error at +VA =5V**
  - **±0.1%FS Gain Error at +VA = 5V**
- **Flexible Analog Inputs:**
  - **True Differential Input**
  - **Differential/Unipolar Input Range (0 to V_{REF})**
  - **TAG Bit Output**
  - **Programmable Averaging Function**
  - **Onboard, Eight Single-Ended/Four Differential Channel Mux:**
    - **High Input Impedance**
    - **High-Performance PGA (Gain = 1/2/4/8)**
    - **PGA Breakout**
    - **Auto/Manual Channel Select with Gain**
    - **Auto/Manual Trigger**
    - **Mixed Type Partial Scan**
- **Built-in Hardware Features:**
  - **On-chip Conversion Clock (CCLK)**
  - **Hardware/Software Reset**
  - **Programmable Status/Polarity for BUSY/INT**
- **Flexible I/O:**
  - **SPI-/ DSP™-Compatible Serial Interface**
  - **Separate I/O Supply (2.2V to 5.5V)**
  - **Onboard 8×1 FIFO Buffer**
  - **SCLK up to 25MHz (VD = 5V)**
- **Multi-Chip Ready and Fully Enabled:**
  - **Global $\overline{\text{CONVST}}$ (Independent of $\overline{\text{CS}}$)**
- **Power-Down Mode**
- **24-Pin 4×4 QFN Package**

APPLICATIONS

- **Portable Communications**
- **Transducer Interfaces**
- **Portable Medical Instruments**
- **Data Acquisition Systems**
- **GPS Chipsets**

DESCRIPTION

The ADS8201 is a low-power, complete on-chip data acquisition system optimized for portable applications that require direct connections, wide dynamic range, and automatic operation with very low power consumption. The device includes a 12-bit, capacitor-based, successive approximation register (SAR) analog-to-digital converter (ADC); a high-performance, continuous-time programmable gain amplifier (PGA); and a fully automatic scan, 8-to-1 multiplexer (mux) with breakout to allow for system design flexibility.

Many other features are included to further optimize system operation. Conversion results may be saved in an onboard first-in/first-out (FIFO) buffer and read out at a later time. Each channel has a gain setting that can be loaded automatically when it is selected. To simplify the serial port design, the ADS8201 offers a high-speed, wide-voltage serial interface. The ADS8201 is ideal for sensor applications (for example, bridge sensors, pressure sensors, accelerometers, gyrosensors, temperature sensors, etc.) as used in gaming and navigation.

The ADS8201 is available in a 24-lead, 4x4 QFN package, and is specified over the –40°C to +85°C industrial temperature range.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	MAXIMUM OFFSET ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8201I	±1.5	±1	±6	QFN-24	RGE	–40°C to +85°C	ADS8201	ADS8201IRGET	Tape and Reel, 250
								ADS8201IRGER	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		ADS8201I	UNIT
Voltage	+IN_I to AGND	–0.3 to +VA +0.3	V
	–IN_I to AGND	–0.3 to +VA +0.3	V
Voltage range	+VA to AGND	–0.3 to 7	V
	+VD to DGND	–0.3 to 7	V
	AGND to DGND	–0.3 to +0.3	V
Digital input voltage to DGND		–0.3 to VD +0.3	V
Digital output voltage to DGND		–0.3 to VD +0.3	
Operating free-air temperature range, T_A		–40 to +85	°C
Storage temperature range, T_{STG}		–65 to +150	°C
Junction temperature, T_J max		+150	°C
Package dissipation ratings: 4 × 4 QFN-16		$(T_J max – T_A)/\theta_{JA}$	
Thermal impedance, θ_{JA}		46	°C/W

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, 2.2V < VA = V_{REF} < 5.5V, 2.2V < VD < 5.5V, f_{SAMPLE} = 100kHz, and gain = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8201I			UNIT
			MIN	TYP	MAX	
ANALOG INPUT (IN0 to IN7)						
FSR	Full-scale input range	(IN_I – $IN_{I–1}$), gain = 1	0		V_{REF}	V
V_{IN}	Absolute input voltage range	+IN_I pin	AGND + 0.1		+VA – 0.1	V
C_{IN}	Input capacitance	With input selected		4		pF
I_{IL}	Input leakage current	No mux switching, dc input		1		nA
	Input channel crosstalk	IN = V_{REF}/2, IN_{I+1}, IN_{I-1}= 0 – V_{REF} span at 1kHz		105		dB

ELECTRICAL CHARACTERISTICS (continued)

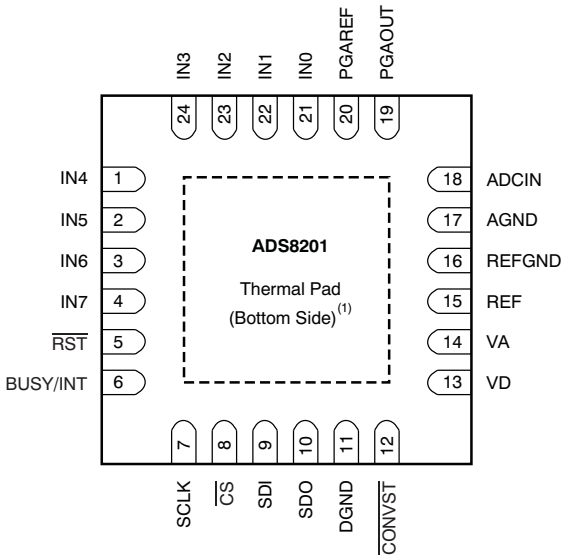
At T_A = –40°C to +85°C, 2.2V < VA = V_{REF} < 5.5V, 2.2V < VD < 5.5V, f_{SAMPLE} = 100kHz, and gain = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8201I			UNIT
			MIN	TYP	MAX	
DC ACCURACY						
	Resolution			12		Bits
	No missing codes		12			Bits
INL	Integral nonlinearity		–1.5	±0.5	+1.5	LSB
DNL	Differential nonlinearity		–1	±0.5	+1	LSB
V_{OS}	Offset error(1)		–7.5	3	+7.5	mV
	Offset error drift			0.2		ppm/°C
	End-point error	Single-ended input, gain = 1	–0.1		+0.1	%
G_{ERR}	Gain error	All gains	–0.1	0.05	+0.1	%
	Gain error drift			0.3		ppm/°C
CMRR	Common-mode rejection ratio	At dc, PGAREF = V_{REF}/2		66		dB
	Noise			600		μV_{RMS}
PSS	Power-supply sensitivity			0.8		LSB
PSRR	Power-supply rejection ratio			68		dB
SAMPLING DYNAMICS						
t_{CONV}	Conversion time			10		µs
	Throughput rate			100		kHz
CLOCK						
f_{CLK}	Internal conversion clock frequency		3.2	4	4.8	MHz
SCLK	External serial clock	Used as I/O clock			25	MHz
EXTERNAL REFERENCE INPUT						
V_{REF}	Input voltage range, V_{REF} = (REF+ – REFGND)	2.2V ≤ VA ≤ 5.5V	2.048		VA	V
R_{REF}	Reference input resistance			360		kΩ
DIGITAL INPUT/OUTPUT						
	Logic family		CMOS			
V_{IH}	High-level input voltage	VD ≥ 2.2V	0.80 × (+VD)		+VD + 0.3	V
V_{IL}	Low-level input voltage	VD ≥ 2.2V	–0.3		0.20 × (+VD)	V
I_{IN}	Input current	V_{IN} = +VD or DGND		10		nA
C_{IN}	Input capacitance			5		pF
V_{OH}	High-level output voltage	VD ≥ 2.2V, I_{OUT} = 100µA	0.8 × (+VD)			V
V_{OL}	Low-level output voltage	VD ≥ 2.2V, I_{OUT} = 100µA	0		0.2 × (+VD)	V
C_{OUT}	Output capacitance			10		pF
C_{LOAD}	Load capacitance				100	pF
	Data format		Straight Binary			
POWER SUPPLY						
VD	Digital supply voltage		2.2		5.5	V
VA	Analog supply voltage		2.2		5.5	V
I_{QA} + I_{QD}	Supply current	VA = 5V		900	1500	µA
		VA = 2.2V		600		µA
I_{PD}	Power-down current(2)	V_{IN} = FS at V_{REF} = 5V, gain = 1		0.5	2	µA
P_{DISS}	Power dissipation	VA = 5V		4.5	7.5	mW
		VA = 2.2V		1.32		mW
TEMPERATURE RANGE						
T_A	Operating		–40		85	°C

(1) Includes mux + PGA + ADC offset error.
(2) With SCLK disabled.

PIN CONFIGURATION

RGE PACKAGE
QFN-24
(TOP VIEW)



(1) Thermal pad should be tied to AGND.

PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN4	1	I	Input channel single-ended 4 or differential pair 3
IN5	2	I	Input channel single-ended 5 or differential pair 3
IN6	3	I	Input channel single-ended 6 or differential pair 4
IN7	4	I	Input channel single-ended 7 or differential pair 4
$\overline{\text{RST}}$	5	I	External hardware reset
BUSY/INT	6	O	Status output. If programmed as the BUSY pin, this pin is low (default) when a conversion is in progress. If programmed as an interrupt (INT), this pin is low for a preprogrammed duration after the end of a conversion and valid data are to be output. The polarity of either BUSY or INT is programmable.
SCLK	7	I	Serial interface clock
$\overline{\text{CS}}$	8	I	Chip select input for SPI interface slave select ($\overline{\text{SS}}$)
SDI	9	I	Serial data in
SDO	10	O	Serial data out
DGND	11	I/O	Interface ground
$\overline{\text{CONVST}}$	12	I	Starts conversion
VD	13	I	Interface supply
VA	14	I	Analog supply (+2.2VDC to +5.5VDC)
REF	15	I	External reference input
REFGND	16	I/O	Reference ground
AGND	17	I/O	Analog ground
ADCIN	18	I	ADC input
PGAOUT	19	O	Mux output. Output can be further filtered before sending to ADCIN.
PGAREF	20	I	PGA Reference
IN0	21	I	Analog channel single-ended 0 or differential pair 0
IN1	22	I	Analog channel single-ended 1 or differential pair 0
IN2	23	I	Analog channel single-ended 2 or differential pair 1
IN3	24	I	Analog channel single-ended 3 or differential pair 1

TIMING CHARACTERISTICS

All specifications typical at –40°C to +85°C, 2.2V < VA = V_{REF} < 5.5V, and 2.2V < VD < 5.5V, unless otherwise noted.

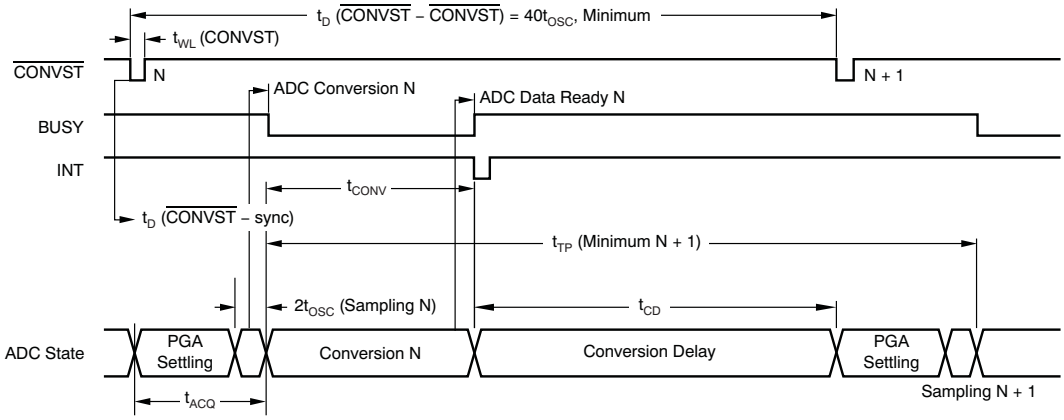


Figure 1. Convert Timing

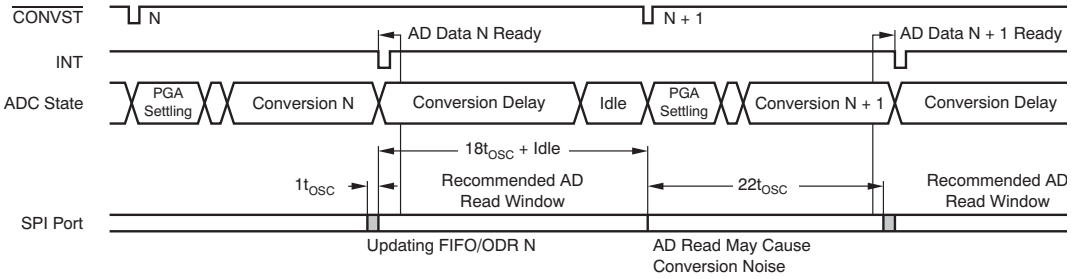


Figure 2. Read Timing

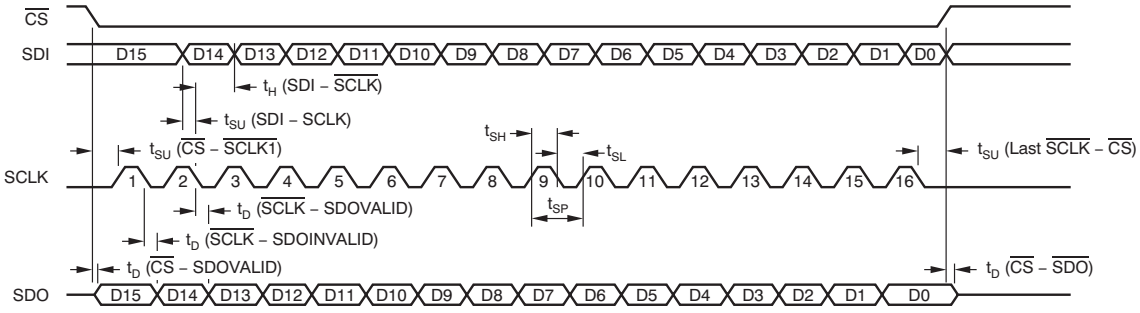


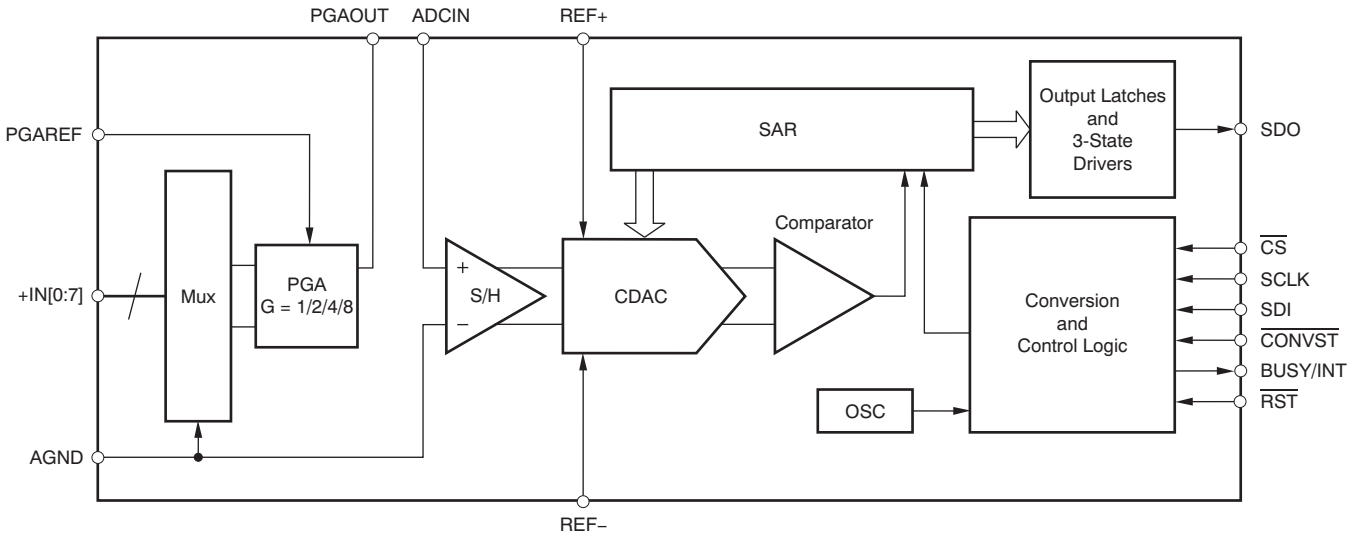
Figure 3. SPI Convert Timing

TIMING CHARACTERISTICS (continued)

Table 1. Timing Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WL}	CONVST (Convert Start) pulse width		40			ns
t_{OSC}	Oscillation time			250		ns
t_H	Hold time		2			ns
t_{SU}	Setup time		10			ns
t_D	Delay time				20	ns
t_{SH}	Clock high time		10			ns
t_{SL}	Clock low time		10			ns
t_{SP}	Clock period			40		ns
t_{CD}	Conversion delay time			18		t_{OSC}
t_{ACQ}	Acquisition time			8.5		t_{OSC}
t_{CONV}	Conversion time			13.5		t_{OSC}
t_{TP}	Throughput time			40		t_{OSC}

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

LINEARITY ERROR vs CODE

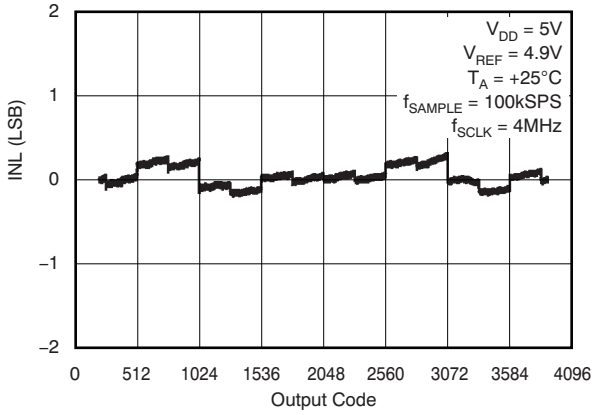


Figure 4.

DIFFERENTIAL LINEARITY ERROR vs CODE

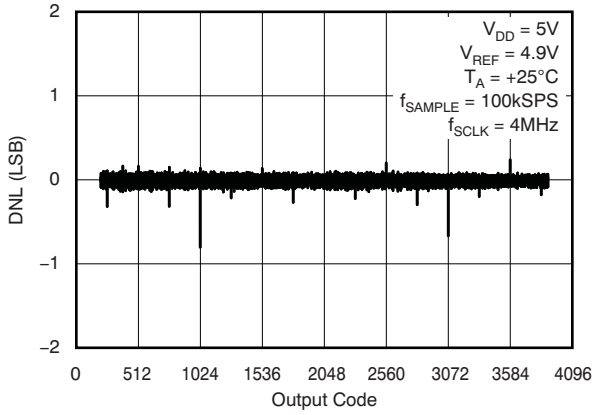


Figure 5.

LINEARITY ERROR vs CODE

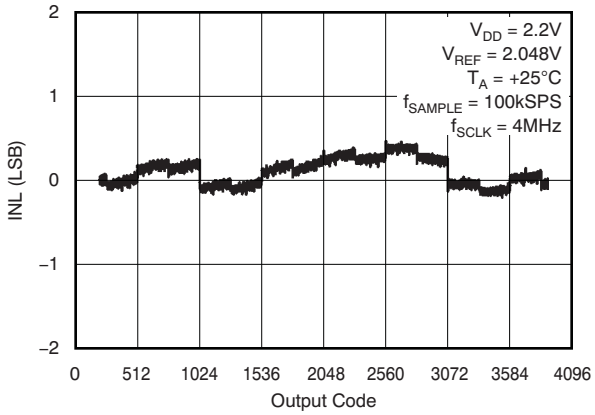


Figure 6.

DIFFERENTIAL LINEARITY ERROR vs CODE

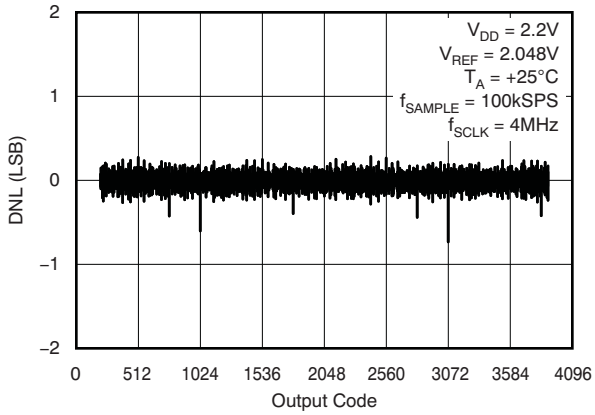


Figure 7.

POWER-SUPPLY CURRENT vs TEMPERATURE

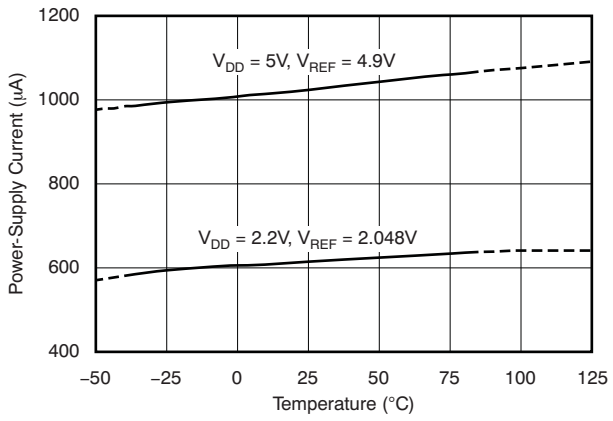


Figure 8.

POWER-DOWN CURRENT vs TEMPERATURE

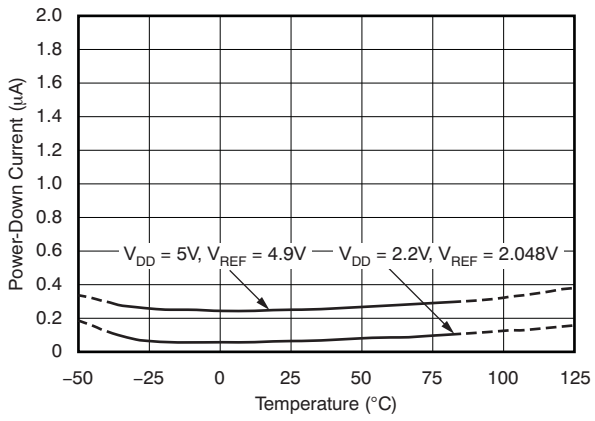


Figure 9.

TYPICAL CHARACTERISTICS (continued)

SINGLE-ENDED OFFSET VOLTAGE vs TEMPERATURE

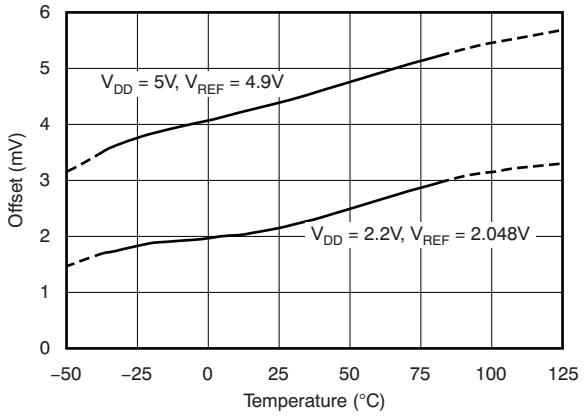


Figure 10.

SINGLE-ENDED GAIN ERROR vs TEMPERATURE

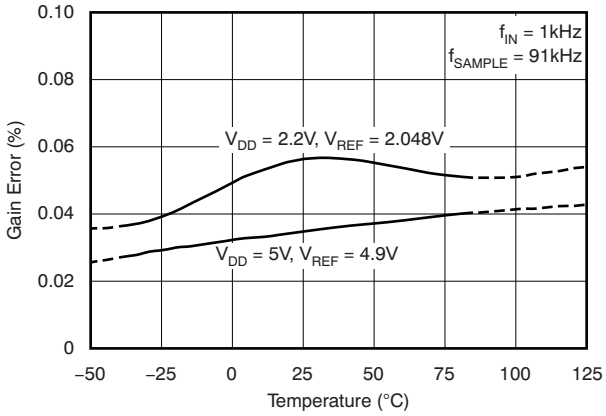


Figure 11.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

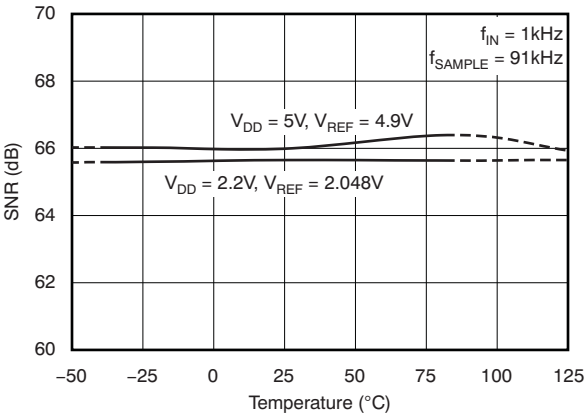


Figure 12.

SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE

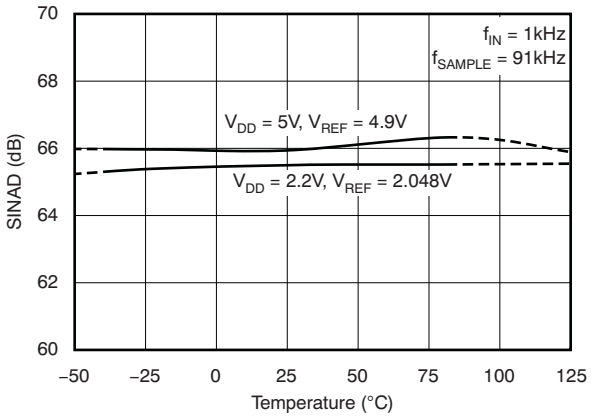


Figure 13.

SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

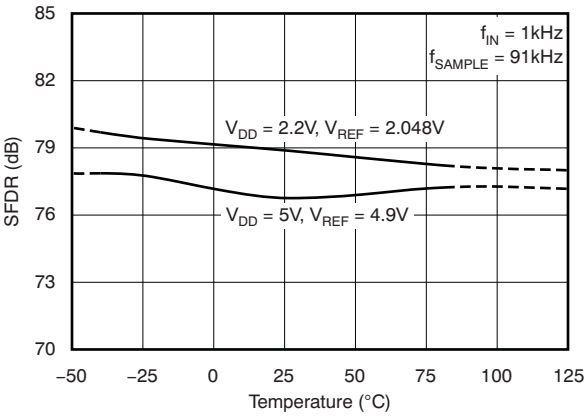


Figure 14.

TOTAL HARMONIC DISTORTION vs TEMPERATURE

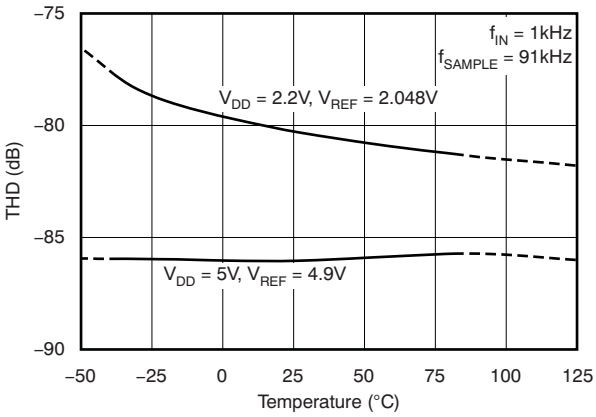


Figure 15.

TYPICAL CHARACTERISTICS (continued)

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

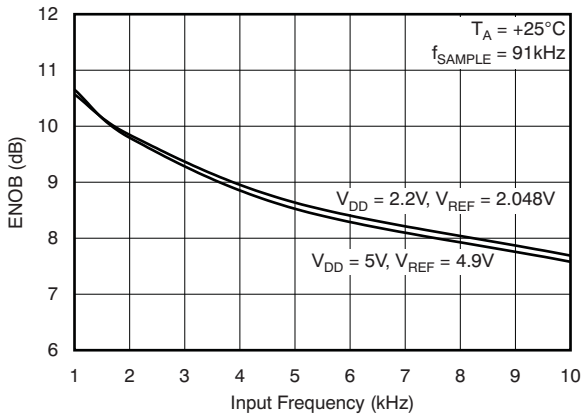


Figure 16.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

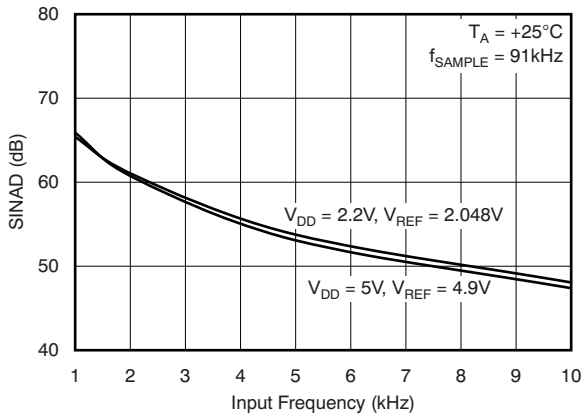


Figure 17.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

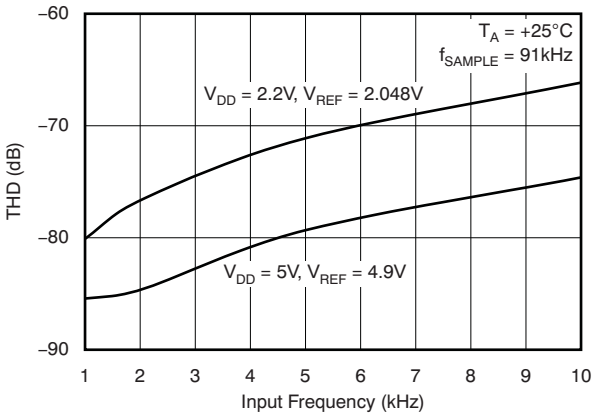


Figure 18.

CROSSTALK vs INPUT FREQUENCY

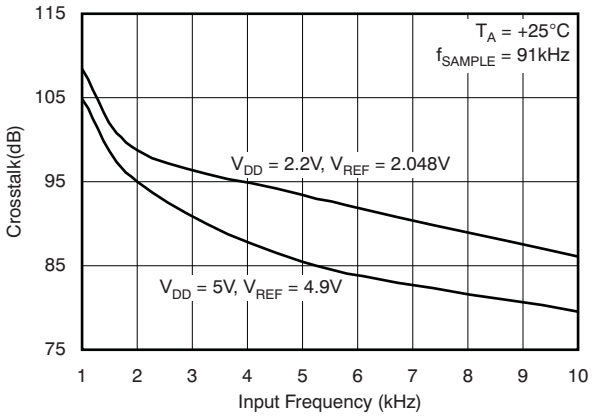


Figure 19.

OUTPUT CODE HISTOGRAM FOR A DC INPUT

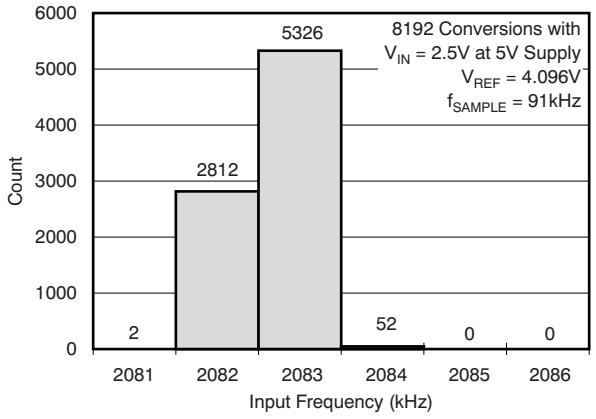


Figure 20.

OUTPUT CODE HISTOGRAM FOR A DC INPUT

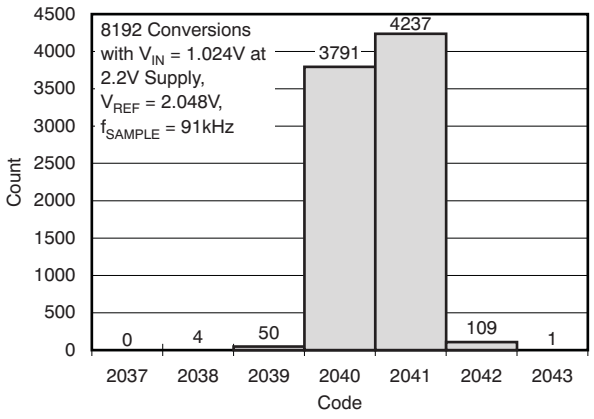


Figure 21.

THEORY OF OPERATION

The ADS8201 is a low-power data acquisition system that includes a 12-bit successive approximation register (SAR) analog-to-digital converter (ADC), eight-channel mux, and a first-in first-out (FIFO) buffer. The SAR architecture is based on charge redistribution, which inherently includes a sample/hold (S/H) function.

The ADS8201 uses an internal clock to run the conversions.

The ADS8201 has eight analog inputs. The analog inputs are either single-ended or differential, depending on the channel configuration. When a conversion is initiated, the input on these pins is sampled on the internal capacitor array. While a conversion is in progress, the inputs are disconnected from any internal function. The device can be programmed for manual channel selection or programmed into an auto-channel select mode that sweeps through all $+IN_I$ channels automatically.

A programmable gain amplifier (PGA) allows for a gain selection of 1, 2, 4, or 8. Individual channels can be programmed to different gains. This feature allows the ADS8201 to be used in a wide range of applications. The channel gain mapping feature is very useful in applications where different sensors around different common-mode voltages must be digitized. Appropriate gain settings can also be chosen to take advantage of the full range of the converter.

ANALOG INPUT

When the converter enters the hold mode, the voltage on the analog input channel of interest is captured on the internal capacitor array. The input span is limited to the range of 0.1V to (VA – 0.1V). The PGA front-end provides a high input impedance that removes the loading effect issues typically associated with high source impedances.

Care must be taken regarding the absolute analog input voltage. To maintain converter linearity, the +IN and –IN inputs and the span of [+IN – (–IN)] should be within the limits specified. Exceeding these ranges may cause the converter linearity to not meet its stated specifications. To minimize noise, use low bandwidth input signals with low-pass filters.

Care should also be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this matching is not observed, the two inputs could have different settling times. These different times may result in offset error, gain error, and linearity error, which all change with temperature and input voltage.

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The ADS8201 features an integrated PGA with gain options of 1, 2, 4, and 8. Each individual channel can be configured for different gain settings depending on the application. An appropriate gain should be chosen for each application to take advantage of the full range of the converter.

At power-up, the system settling time is approximately 40μs. This period includes the PGA turn-on time and settling time to a 12-bit level. Once the device has been configured, the PGA settling time during channel switching is optimized to provide a throughput of 100k samples-per-second (SPS) in auto-trigger and auto-channel update modes.

The ADS8201 also provides a PGAOUT pin that can be used for further signal conditioning before inputting to the ADC. If no additional conditioning is required, the PGAOUT pin should be tied to the ADCIN pin.

BIPOLAR/UNIPOLAR OPERATION

The PGAREF pin allows the ADS8201 to be operated in true differential and bipolar modes. This type of operation is achieved by setting the PGAREF pin. If this pin is set to GND, the device operates in unipolar mode. If the PGAREF pin is set to $V_{REF}/2$, the ADS8201 operates in a bipolar mode. Both +IN and –IN inputs can swing differentially $\pm V_{REF}/2$. All common-mode signals from 0V to V_{REF} can be eliminated when the ADS8201 is configured in differential mode. See the *Application Information* section for an example of a typical circuit diagram.

REFERENCE

The ADS8201 requires an external reference. A clean, low-noise, well-decoupled supply voltage on this pin is required to ensure good converter performance. A low-noise bandgap reference such as the REF3240 can be used to drive this pin. A 10μF ceramic decoupling capacitor is required between the REF and REFGND pins of the converter. These capacitors should be placed as close as possible to the respective device pins. The REFGND pin should be connected by its own via to the analog ground plane of the printed circuit board (PCB) with the shortest possible trace. The minimum reference supported by the ADS8201 is 2.048V.

CONVERTER OPERATION

The ADS8201 has an internal clock that controls the conversion rate; the frequency of this clock is 4MHz, however, this clock can have a variance of up to 20%. The Conversion Delay System Configuration Register (SCR) at address 0Ah can be used to offset the conversion clock variance. This register allows the conversion delay to be programmed after conversion from a range of 0.5μs to 15μs. The default conversion delay is set to 4.5μs; however, the appropriate conversion delay can be selected to achieve maximum throughput. Unless the device is in power-down mode, the internal clock is always on. The minimum acquisition time is 8.5 clock cycles (this period is equivalent to 2.125μs at 4MHz) after $\overline{\text{CONVST}}$ is asserted. It takes 13.5 conversion clocks (CCLKs), or approximately 3.375μs, to complete one conversion. The data can be clocked out during the next 4.5μs through the serial interface. Care must be taken to ensure that the next conversion is not initiated until 10μs after the first convert start is asserted.

ADC OPERATING MODE SUMMARY

Table 2 summarizes the ADC operating modes for the ADS8201.

Table 2. ADC Operating Modes

ADC OPERATING MODE	ADC TRIGGER	CHANNEL CONTROL	DELAY MUX	MULTI-SCAN	AUTO PD	MODE DESCRIPTION
0 (000)	Idle (no trigger)	N/A	N/A	N/A	N/A	ADC idle
1 (001b)	Reserved					
2 (010b)	Manual trigger	Manual	Off	N/A	Off	Manual trigger with manual-channel
3 (011b)	Manual trigger	Manual	On	N/A	Off	Manual trigger with manual-channel and delay mux
4 (100b)	Auto trigger	Manual	On	N/A	Off	Auto trigger with manual-channel
5 (101b)	Auto trigger	Auto increment	N/A	Single scan	Off	Auto trigger with auto-channel and single-scan
6 (110b)	Auto trigger	Auto increment	N/A	Multi-scan	Off	Auto trigger with auto-channel and multi-scan
7 (111b)	Reserved					

MANUAL TRIGGER (See ADC Trigger SCR, Address 08h, Bits[2:0])

Manual-Trigger mode (Modes 2 and 3) can be selected by writing to the ADC Trigger SCR (see the SCR Register Map). In these modes, it is required to issue a convert start (CONVST) pulse through the $\overline{\text{CONVST}}$ pin or an ADC read command if bit 0 of the ADC SCR is set to '1' to allow a conversion to initiate through the serial interface. CCR[0:3] can be used to configure each channel according to the specific application requirements. For Mode 3, see the Delay Mux Description section for details. Table 3 lists the selection options for manual channel selection.

Table 3. Manual Channel Selection(1)

SELECTION OPTION	BIT SETTINGS
Delay mux select enabled(1)	ADC SCR, bit D[1] = '1'; FIFO buffer enabled (as shown in Figure 22)
	ADC SCR, bit D[1] = '0'; FIFO buffer disabled (as shown in Figure 22)
Delay mux select disabled(1)	ADC SCR, bit D[1] = '1'; FIFO buffer enabled (as shown in Figure 22)
	ADC SCR, bit D[1] = '0'; FIFO buffer disabled (as shown in Figure 22)

(1) See ADC Trigger SCR, bits D[2:0].

Mode 2 (manual trigger with manual-channel update) provides complete control over the ADS8201 timing. The user controls when to issue a CONVST and when to read the output data. A switch can be made to any channel without following any particular sequence. The device can also be configured to enable or disable the FIFO buffer in this mode.

Mode 3 (manual trigger with manual-channel update and delay mux) allows the ADS8201 to switch the mux to the next input channel after the current sampling is complete. This capability maximizes the time required for the PGA to settle for the next channel and subsequently provides faster throughput. See Figure 22 and Figure 25 for timing details. This increased throughput is the key difference between this mode and Mode 2. The delay mux feature allows for full 100kSPS throughput, in spite of being in manual trigger and manual channel update mode.

There are two ways to set up the delay mux in this mode. If using the following sequence, then data from first channel are not repeated:

1. The first channel of interest is set.
2. Mode 3 is selected.
3. The second channel of interest is set.
4. The $\overline{\text{CONVST}}$ pin is asserted.

However, if the second channel of interest is set after the $\overline{\text{CONVST}}$ pin is asserted, then the first conversion result should be treated as a *dummy* conversion because the conversion result from the first channel is repeated twice. Subsequent channels should be selected before asserting the next $\overline{\text{CONVST}}$ in order to achieve the benefit of the delay mux feature.

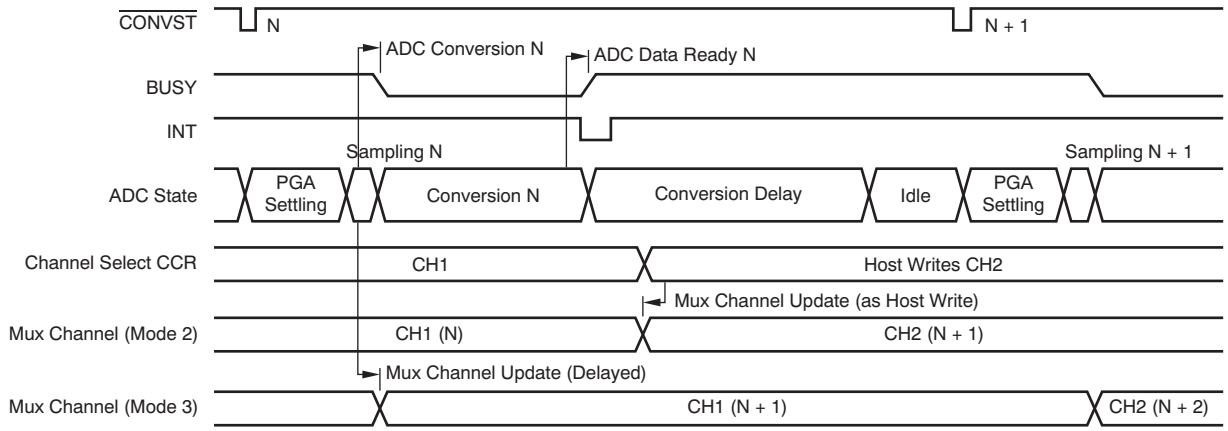


Figure 22. Mode 2, Mode 3 Timing

AUTO TRIGGER (See ADC Trigger SCR, Address 08h, Bits[2:0])

Auto-trigger mode can be selected by writing to the ADC Trigger SCR (see the SCR Register Map). In Auto-Trigger (Modes 4, 5, and 6), Auto-Channel (Modes 5 and 6) or Manual-Channel (Mode 4) selection must be enabled after all the channels have been configured according to the specific application.

In Auto-Trigger with Auto-Channel Update and Single-Scan mode (Mode 5), the internal device logic triggers conversions and all selected channels are converted sequentially. After the completion of the selected channel conversions, an SPI command must be issued to initiate the next scan event. In this mode, the FIFO buffer can be enabled or disabled. If the FIFO buffer is enabled and the next scan event is initiated, the contents of the FIFO buffer are overwritten. Ensure that all results from the FIFO buffer have been read before issuing the command to start the next scan event. This mode is useful for applications where an external source triggers the scan event; however, the trigger is not periodic.

In Auto-Trigger with Auto-Channel Update and Multi-Scan mode (Mode 6), the internal device logic triggers conversions and all selected channels are converted sequentially. In this mode, if the FIFO buffer is disabled, and the ADS8201 continues to trigger conversions for the selected channels in a cyclical mode until an SPI command is sent to stop the conversion. For example, if channel 4 is selected as the starting channel number, the ADS8201 converts channels 4, 5, 6, 7, 4, 5, 6, 7, etc., until this mode is disabled. If the FIFO buffer is enabled and Interrupt SCR, bit D[1] is set, the ADS8201 issues a scan data ready interrupt. It is important to note that in Mode 6, the FIFO buffer contents must be read when the buffer is full (eight conversions = complete); otherwise, subsequent conversions will overwrite the data in the FIFO buffer. This mode is useful when continuous conversion of the input signals across single or multiple channels is required. Figure 26 illustrates the timing for a shared single-scan and multiple-scan mode event.

In Auto-trigger with Manual Channel Update mode (Mode 4), the user must select the next channel. In this mode, the delay mux feature is always enabled. Table 4 and Table 5 summarize the selection options for auto channel update and manual channel update, respectively. This mode is useful when the user wants to have flexibility in the channel selection and does not want to use consecutive channels. The delay-mux feature provides full 100kSPS speed in spite of using manual channel update mode.

There are two ways to set up the delay mux in this mode. If using the following sequence, then data from first channel are not repeated:

1. The first channel of interest is set.
2. Mode 4 is selected.
3. The second channel of interest is set within 10µs after setting Mode 4.
4. The $\overline{\text{CONVST}}$ pin is asserted.

However, if the second channel of interest is not set within 10µs after triggering the delay mux mode, then the first conversion result should be treated as a dummy conversion because the conversion result from the first channel is repeated twice.

Table 4. Auto Channel Update(1)

SELECTION OPTION	BIT SETTINGS
Single-Scan Mode (Mode 5)(1)	ADC SCR, bit D[1] = '1'; FIFO buffer enabled (as shown in Figure 23)
	ADC SCR, bit D[1] = '0'; FIFO buffer disabled (as shown in Figure 23)
Multi-Scan Mode (Mode 6)(1)	ADC SCR, bit D[1] = '1'; FIFO buffer enabled (as shown in Figure 24)
	ADC SCR, bit D[1] = '0'; FIFO buffer disabled (as shown in Figure 24)

(1) See ADC Trigger SCR:D[2:0].

Table 5. Manual Channel Update(1)

SELECTION OPTION	BIT SETTINGS
Delay mux select (Mode 4) (This is the only option with auto channel select mode and manual trigger)	ADC SCR, bit D[1] = '1'; FIFO buffer enabled (as shown in Figure 25)
	ADC SCR, bit D[1] = '0' ; FIFO buffer disabled (as shown in Figure 25)

(1) See ADC Trigger SCR, bits D[2:0].

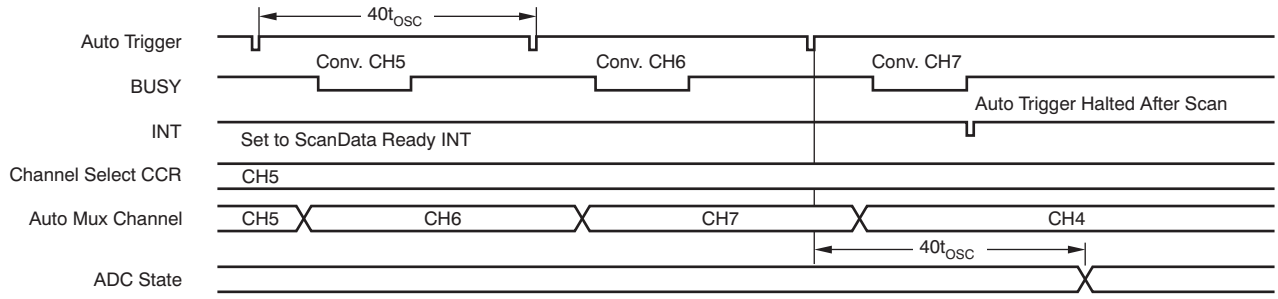


Figure 23. Mode 5 Timing

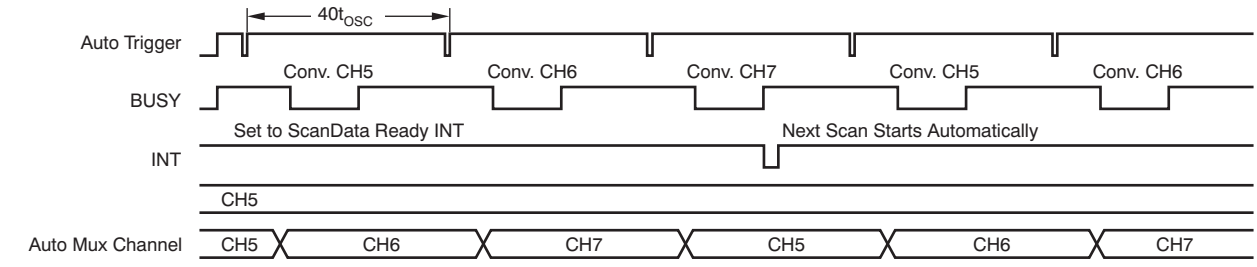


Figure 24. Mode 6 Timing

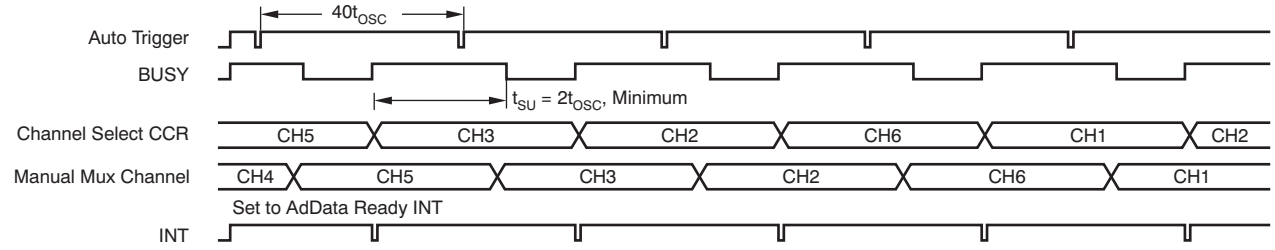
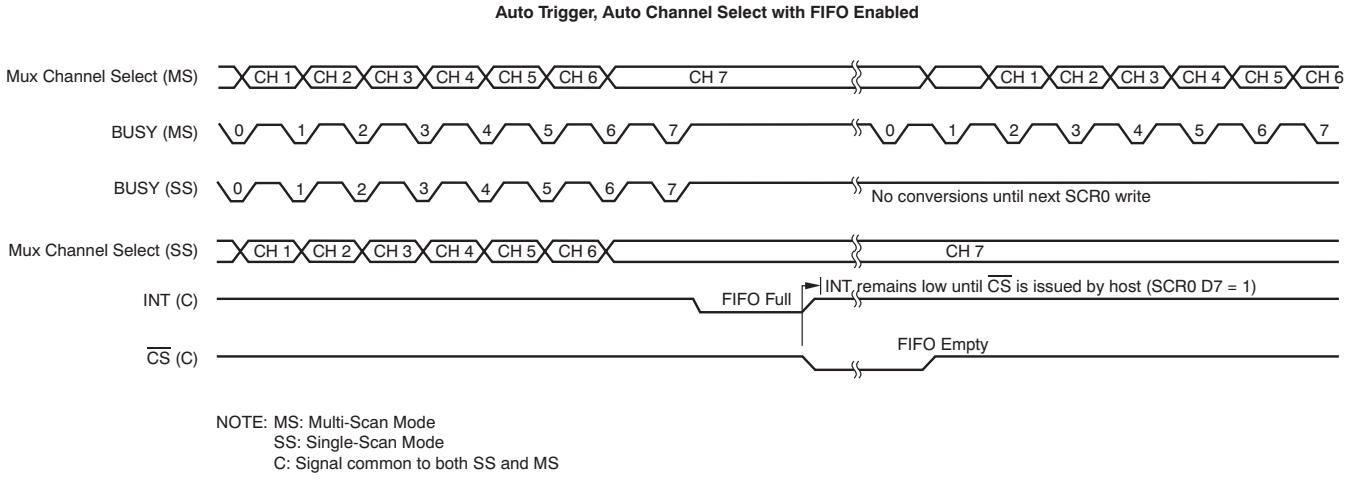


Figure 25. Mode 4 Timing



NOTE: MS: Multi-Scan Mode
SS: Single-Scan Mode
C: Signal common to both SS and MS

Figure 26. Single-Scan/Multiple-Scan Mode Event with FIFO Buffer Enabled

CONVERSION START

A conversion is initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 40ns. After the minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high. $\overline{\text{CONVST}}$ acts independently of $\overline{\text{CS}}$, so it is possible to use one common $\overline{\text{CONVST}}$ for applications that require simultaneous sample/hold events. The ADS8201 requires 8.5 conversion clock (CCLK) cycles for acquisition and 13.5 CCLK edges to complete a conversion. The conversion time is equivalent to approximately 3.375μs with a 4MHz internal clock. The minimum time between two consecutive $\overline{\text{CONVST}}$ signals is 40 CCLKs, or approximately 10μs.

Conversion can also be initiated without using the $\overline{\text{CONVST}}$ pin if the device is properly programmed (ADC SCR, bit D[0] = '1'). In this case, an ADC read command must be issued. The conversion start is then issued through the SPI interface. When the converter is configured in Auto-Trigger mode, the next conversion automatically starts 18 CCLKs after the end of a conversion. These 18 conversion clocks are used as the data acquisition time as well as the PGA settling time. The PGA must settle to a 12-bit level. In this case, the time to complete one acquisition and conversion cycle is exactly 22 CCLKs.

BUSY/INT PIN DESCRIPTION

BUSY Pin Functionality

The BUSY/INT pin can be programmed as BUSY by configuring the ADC System Configuration Register (ADC SCR, bit D[2] = '1') . When the status pin is programmed as BUSY and the polarity is set as active low, this pin works in the following manner:

- **In Manual-Trigger mode:** the BUSY output goes low up to 8.5 CCLKs after $\overline{\text{CONVST}}$ goes low. BUSY stays low throughout the conversion process and returns high when the conversion completes. See Figure 1 through Figure 3 for detailed timing diagrams.
- **In Auto-Trigger mode:** the BUSY output goes low for 13.5 CCLKs. See Figure 1 through Figure 3 for detailed timing diagrams. It is important to note that if BUSY/INT pin is programmed as BUSY, then bits D[3:0] of the Interrupt SCR (address 06h) are inactive. Those interrupts only take effect when the BUSY/INT pin is programmed as INT.

INT Pin Functionality

The BUSY/INT pin can be programmed as INT by configuring the ADC System Configuration Register (ADC SCR, bit D[2] = '0'). The interrupt can be programmed to be edge-triggered or level-triggered by configuring the ADC SCR, bit D[4]. This option is only available when the pin is configured as INT. For the INT pin to be active, the interrupt SCR must be configured with the type of interrupt required for the specific application. This procedure can be done by configuring one of the four bits, D[3:0], of the Interrupt SCR (address 06h). For example, if the interrupt function is desired after the ADC data are ready, set the Interrupt SCR, bit D[0] = '1').

If the FIFO buffer is disabled and Interrupt SCR, bit D[0] is set, the ADS8201 issues an interrupt pulse after the end of a conversion.

If the FIFO buffer is enabled and Interrupt SCR, bit D[2] is set, the ADS8201 issues an interrupt pulse after the FIFO buffer is full.

POWER-DOWN MODE

The ADS8201 has a comprehensive, built-in, power-down feature. Contents of the configuration register are not affected when in power-down mode. Power-down mode can be activated by setting the Interrupt SCR, bit D[7] = '1'. Care must be taken to ensure that the ADC is in idle mode before writing to the Interrupt SCR. When the device is in power-down mode, every block except the interface is in a power-down state. The analog blocks receive no bias currents and the internal oscillator is turned off. In this mode, power dissipation falls from 900μA to < 1μA in 2μs. The wake-up time from power-down mode is 40μs. Power-down or power-on status of the ADC can be read through the Status SCR, bit D[0]. To bring the device out of power down, set the Interrupt SCR (address 06h), bit D[7] = '0'.

READING CONVERSION RESULTS

The conversion result is available to the input of the Output Data Register (ODR) at the end of the conversion, and presented to the output of the Output Register at the next falling edge of $\overline{CS}$. The host processor can then shift the data out through the SDO pin at any time except during the quiet zone. The quiet zone is 18 CCLKs after BUSY goes high, If BUSY is programmed as active low.

Be careful not to place the falling edge of $\overline{CS}$ at the precise moment that the conversion ends (by default, the end of conversion is when BUSY goes high); otherwise, the conversion data could be corrupted. The falling edge of $\overline{CS}$ should be at least one CCLK either before or after the end of conversion. If $\overline{CS}$ is placed before the end of conversion, the previous conversion result is read. If $\overline{CS}$ is placed after the end of conversion, the current conversion result is read.

The conversion result is represented by 12-bit data in straight binary format, as shown in Table 6. Therefore, it is normally clocked out within 12 SCLKs. In order to read the averaging bits and the TAG bits, 20 CLK cycles must be provided. See the TAG Mode section for more details. Data output from SDO are left-aligned and MSB first. SDO remains low until $\overline{CS}$ goes high again.

The serial output (SDO) is active when $\overline{CS}$ is low. The rising edge of $\overline{CS}$ puts the SDO output into a 3-state mode. Note that whenever SDO is not in a 3-state mode (that is, when $\overline{CS}$ is low and SCLK is running), a portion of the conversion result shows up on the SDO pin. The number of bits that appear depends on how many SCLKs are supplied. The exception is that SDO outputs all 1's during the cycle immediately after any reset event (hardware or software) occurs.

Table 6. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full-Scale Range	V_{REF}	BINARY CODE	HEX CODE
Least Significant Bit (LSB)	$V_{REF}/4096$		
Full-Scale	V_{REF} – 1LSB	1111 1111 1111	FFFF
Midscale	$V_{REF}/2$	1000 0000 0000	8000
Midscale – 1LSB	$V_{REF}/2$ – 1LSB	0111 1111 1111	7FFF
Zero	0V	0000 0000 0000	0000

TAG MODE

The ADS8201 has a TAG feature that shows which channel the converted result comes from. An address bit that indicates the conversion result channel number is added after the LSB of the SDO readout. There are four TAG bits: the first three identify the channel and the fourth identifies either single-ended or differential operating mode. To read the TAG bits, 20 CLK cycles must be provided; see Figure 30. If the TAG bits do not need to be read, only 16 CLK cycles should be provided.

AVERAGING MODE

The ADS8201 offers multiple averaging options for applications that may require greater than 12-bit resolution. This feature allows for better noise performance by a factor of $1/\sqrt{Number\ of\ Samples}$. The result is output as a maximum of 14-bit resolution. Bits D[7:5] of the ADC SCR (address 05h) can be used to select different averaging options. Two distinct averaging features, fast averaging and accurate averaging, are available:

- **Fast Averaging:** An average of 4,8, or 16 results can be selected to increase overall resolution to a 13-bit or 14-bit level. In Fast Averaging, after the first conversion is complete (approximately 4μs), the next conversion starts immediately without the 6μs delay for PGA settling. This mode should be used when the input to the PGA is stable and is within the 12-bit level.
- **Slow Averaging:** An average of 4, 8, or 16 results can be selected to increase output accuracy compared to the fast averaging mode. In Slow Averaging mode, each conversion requires 10μs. This mode should be used when the input to the PGA is not stable.

FIFO BUFFER DESCRIPTION

The ADS8201 offers a first-in/first out (FIFO) buffer that allows the user to store up to eight independent conversion results. The FIFO buffer can be enabled or disabled by setting bit D[1] of the ADC SCR. To extract the data from the FIFO buffer, $\overline{CS}$ must be enabled for every conversion result. As an example, if all eight conversion results are to be extracted from the FIFO buffer, $\overline{CS}$ must be asserted low eight times. During the time that $\overline{CS}$ is low, there is the option to provide as many CLK cycles as desired to extract the data of interest. If 12 CLKs are provided, only the 12-bit conversion result is extracted. If the the TAG information is to be extracted as well, then 20 CLKs must be provided. See Figure 30 for details on the optional bits available. The functionality of the FIFO buffer can vary depending on the mode selected.

1. **Auto-Trigger and Auto Channel Select mode:** In this mode, whether or not the FIFO buffer is seen as full is defined by the number of channels in the specific scan event. For example, if channel 3 is chosen as the starting channel number and all channels are in single-ended mode, once the conversion is complete for channels 3, 4, 5, 6, and 7, a *scan data ready* interrupt is issued. Note that there are only five results in the buffer. If a multi-scan event is enabled (Mode 6 of the ADC SCR), conversions are initiated in a cyclical manner. If a single-scan event is enabled, the devices wait for a $\overline{CONVST}$ pulse before starting the next conversion.
2. **Auto-Trigger and Manual Channel Select mode:** This mode acts in a similar manner to the previous mode, except that the next conversion channel must be manually selected.
3. **Manual-Trigger and Manual Channel Select mode:** In this mode, eight conversions must be completed before a *FIFO buffer full* interrupt is issued. This mode provides the flexibility to choose any sequence of channels for conversion.

INTERRUPT DESCRIPTION

The ADS8201 offers multiple interrupts for various user-defined options. The Interrupt SCR defines the various interrupts available in the ADS8201.

1. **FIFO Buffer Not Empty Interrupt:** If this interrupt is enabled (Interrupt SCR, bit D[3] = '1'), the ADS8201 generates an interrupt if the FIFO buffer is not empty. In applications where the CPU can allocate additional processing time, use of this interrupt is recommended to improve the system throughput.
2. **FIFO Buffer Full Interrupt:** If this interrupt is enabled (Interrupt SCR, bit D[2] = '1'), the ADS8201 generates an interrupt if the FIFO buffer is full. For applications where the CPU is processing multiple tasks, this interrupt is recommended because it requires minimum processing power.
3. **Scan Data Ready Interrupt:** If this interrupt is enabled (Interrupt SCR, bit D[1] = '1'), the ADS8201 generates an interrupt when scan data are ready. This interrupt is only applicable in Auto-trigger and Auto channel select modes, and tells the user when the scan event is complete for the selected channels. For example, in single-ended configuration, if channel 3 is selected as the starting channel number, the interrupt is issued after conversion is complete for channels 3, 4, 5, 6, and 7.
4. **ADC Data Ready Interrupt:** If this interrupt is enabled (Interrupt SCR, bit D[0] = '1'), the ADS8201 issues an interrupt after the first 12 bits of conversion data are available, if averaging is disabled. If averaging is enabled, the interrupt is issued after all conversions required for averaging are complete.

DELAY MUX DESCRIPTION

The Delay Mux feature is only available in the following modes:

- Manual-trigger with manual channel update (Mode 3 of ADC Trigger SCR)
- Auto-trigger with manual channel update (Mode 4 of ADC Trigger SCR)

This feature allows the ADS8201 to switch the mux to the next input channel after the current sampling is complete. This capability maximizes the time required for the PGA to settle for the next channel and subsequently provides faster throughput. Care must be taken, however, to ensure that the PGA does not settle to the 12-bit level for throughput less than 10μs. See Figure 22 and Figure 25 for timing details. In this mode, the mux channel is changed after the completion of next sampling period.

RESET OPERATION

The ADS8201 can be reset in two ways: hardware reset and software reset. A hardware reset can be asserted via the $\overline{RST}$ pin. A software reset can be asserted through the serial interface by writing AAh to the Reset SCR (address 09h). While hardware reset can be asserted at any time, software reset cannot be initiated if the device is in power-down mode. As long as the device is in any other of the ADC operating modes, a software reset can be issued. Once the reset is issued, the device comes back up in Mode 2 configuration. Once the reset is issued, all digital logic and configuration registers are set to the respective default states (see the Channel Configuration Map and System Configuration Map sections for default values). Any conversion in process is aborted as soon as a reset is issued. Data stored in the FIFO buffer are also reset. The channels and system registers must be reconfigured.

DEVICE CONFIGURATION

WRITING TO/READING FROM THE REGISTERS

The ADS8201 can be configured by writing to a total of 10 configuration registers: five channel configuration registers (CCRs) and five system configuration registers (SCRs). The Interrupt and Status SCRs provide the status of various interrupts. Figure 27 illustrates a state diagram for the ADC modes. Figure 28 through Figure 30 show the details of the Register Read, Register Write, and ADC Read operations, respectively. Table 7 summarizes the register addresses. It is important to note that except for registers 04h, 08h, and 09h (which can be accessed from any mode), all other registers must be accessed from ADC idle mode only.

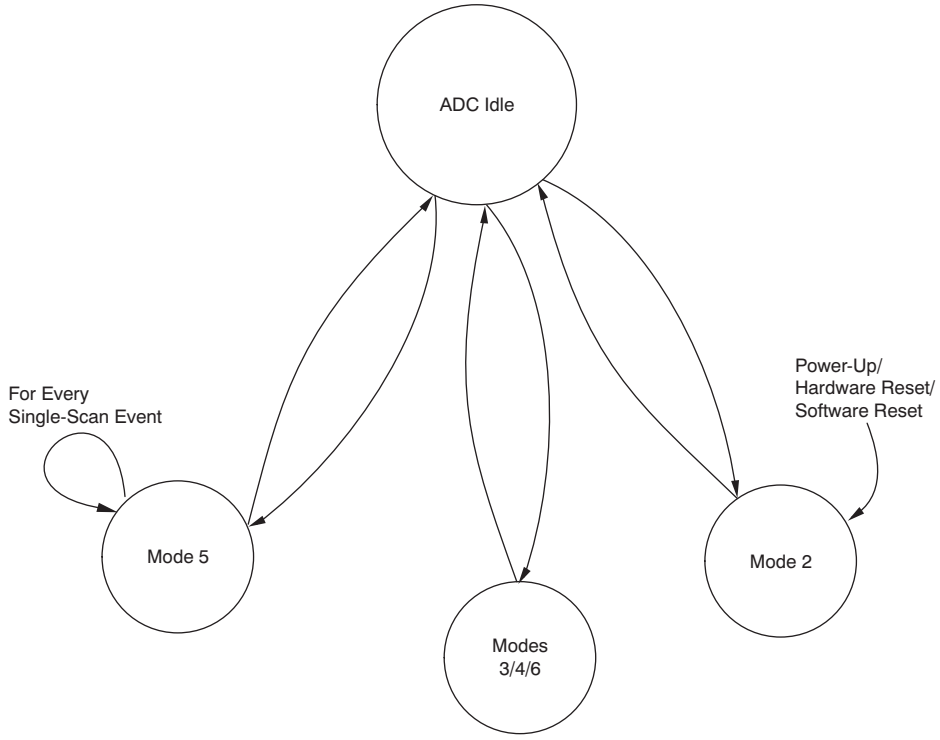


Figure 27. ADC Mode State Diagram

	ADDRESS								DATA							
SDIN	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	X	X	X
SDOUT	X	X	X	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

Figure 28. Register Read

	ADDRESS								DATA							
SDIN	1	0	A3	A2	A1	A0	X	X	D7	D6	D5	D4	D3	D2	D1	D0
SDOUT	X	X	X	0	0	0	0	0	X	X	X	X	X	X	X	X

Figure 29. Register Write

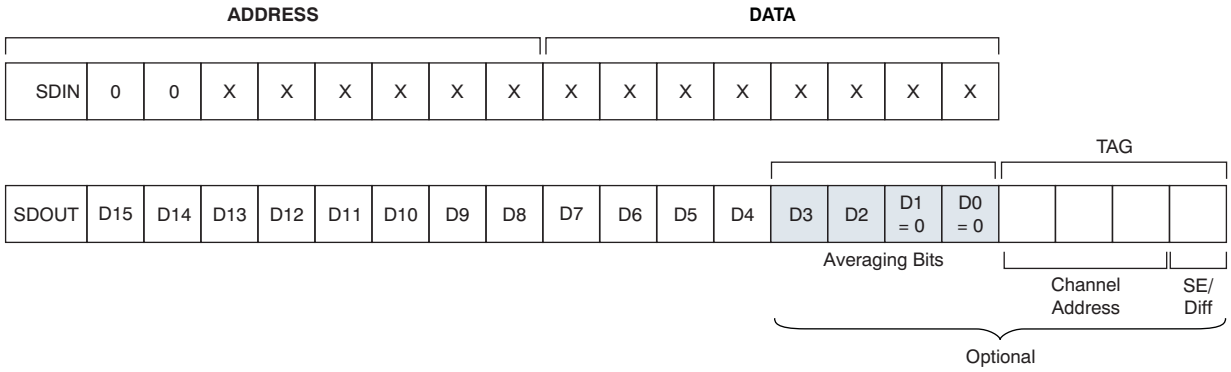


Figure 30. ADC Read

Table 7. Register Addresses

REGISTER	A3	A2	A1	A0
Channel 0/1 CCR	0	0	0	0
Channel 2/3 CCR	0	0	0	1
Channel 4/5 CCR	0	0	1	0
Channel 6/7 CCR	0	0	1	1
Channel Select CCR	0	1	0	0
ADC SCR	0	1	0	1
Interrupt SCR	0	1	1	0
Status SCR	0	1	1	1
ADC Trigger SCR	1	0	0	0
RESET SCR	1	0	0	1
Conversion Delay SCR	1	0	1	0

CHANNEL CONFIGURATION REGISTER (CCR) MAP

Channel 0/1 CCR (Address 00h)

D[7:6]	**Not used** [0:0]
D[5:4]	**Channel 1 Gain Single-Ended** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8
D[3]	**Channel 0 Differential Odd/Even Polarity** 0: Even polarity (default) 1: Odd polarity
D[2]	**Channels 0/1 Single-Ended/Differential** 0 : Ch0/1 Single-ended (default) 1: Ch0/1 Differential
D[1:0]	**Channel 0 Gain** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8

Channel 2/3 CCR (Address 01h)

D[7:6]	**Not used** [0:0]
D[5:4]	**Channel 3 Gain Single-Ended** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8
D[3]	**Channel 2 Differential Odd/Even Polarity** 0: Even polarity (default) 1: Odd polarity
D[2]	**Channels 2/3 Single-Ended/Differential** 0 : Ch2/3 Single-ended (default) 1: Ch2/3 Differential
D[1:0]	**Channel 2 Gain** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8

Channel 4/5 CCR (Address 02h)

D[7:6]	**Not used** [0:0]
D[5:4]	**Channel 5 Gain Single-Ended** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8
D[3]	**Channel 4 Differential Odd/Even Polarity** 0: Even polarity (default) 1: Odd polarity
D[2]	**Channels 4/5 Single-Ended/Differential** 0 : Ch4/5 Single-ended (default) 1: Ch4/5 Differential
D[1:0]	**Channel 4 Gain** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8

Channel 6/7 CCR (Address 03h)

D[7:6]	**Not used** [0:0]
D[5:4]	**Channel 7 Gain Single-Ended** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8
D[3]	**Channel 6 Differential Odd/Even Polarity** 0: Even polarity (default) 1: Odd polarity
D[2]	**Channels 6/7 Single-Ended/Differential** 0 : Ch6/7 Single-ended (default) 1: Ch6/7 Differential
D[1:0]	**Channel 6 Gain** 00: G = 1 (default) 01: G = 2 10: G = 4 11: G = 8

CHANNEL SELECT REGISTER MAP

Channel Select Register (Address 04h)

D[7:3]	**Not used** [0:0]
D[2:0]	**Select Mux Input Channel/Start Channel Number if in Auto-Scan Mode** 000: Channel 0 (default) 001: Channel 1 010: Channel 2 011: Channel 3 100: Channel 4 101: Channel 5 110: Channel 6 111: Channel 7

SYSTEM CONFIGURATION REGISTER (SCR) MAP

ADC SCR (Address 05h)

D[7:5]	**Average Select** 000: No average (default) 001: Fast average of four results 010: Fast average of eight results 011: Fast average of 16 results 100: No average 101: Accurate average of four results 110: Accurate average of eight results 111: Accurate average of 16 results
D[4]	**Interrupt Select** 0: Level triggered (default) 1: Edge triggered. Period of pulse is 250ns.
D[3]	**BUSY/INT Level** 0: Active low (default) 1: Active high
D[2]	**BUSY/INT Select** 0 : INT (default) 1: BUSY
D[1]	**FIFO Buffer Enable** 0: FIFO buffer disabled (default) 1: FIFO buffer enabled
D[0]	**RD/CONVST Trigger** 0 : Issue CONVST from the pin (default) 1: Convert start is issued through the SPI after the first read of the ADC. Ignore the first read.

Interrupt SCR (Address 06h)

D[7]	**Power-Down Control** 0: Normal conversion mode (default) 1: Power-down idle mode
D[6:4]	**Always Reads '0'**
D[3]	**FIFO Buffer Not Empty Interrupt** Read 0: Interrupt not generated (default) Read 1: Interrupt generated when FIFO buffer is not empty Write 0: Disable interrupt Write 1: Enable interrupt
D[2]	**FIFO Buffer Full Interrupt**
	Read 0: Interrupt not generated (default) Read 1: Interrupt generated when FIFO buffer is full Write 0: Disable interrupt Write 1: Enable interrupt
D[1]	**Scan Data Ready Interrupt** Read 0: Interrupt not generated (default) Read 1: Interrupt when scan data are ready. Only applicable in auto channel and auto-trigger mode. Write 0: Disable interrupt Write 1: Enable interrupt
D[0]	**ADC Data Ready Interrupt** Read 0: Interrupt not generated (default) Read 1: Interrupt generated when ADC data are ready. Write 0: Disable interrupt Write 1: Enable interrupt

Status SCR (Address 07h)

D[7:4]	**FIFO Buffer Level: Number of Entries**
D[3]	**FIFO buffer Not Empty** 0: FIFO buffer empty 1: FIFO buffer not empty
D[2]	**FIFO Buffer Full** 0: FIFO buffer not full 1: FIFO buffer full
D[1]	**Scan Data Ready** 0: Not ready 1: Ready
D[0]	**ADC Data Ready** 0: Not ready 1: Ready

ADC Trigger SCR (Address 08h)

D[7:3]	**Not used**
D[2:0]	**ADC Trigger** 000: ADC idle 001: Reserved 010: Manual trigger with manual channel update (default) 011: Manual trigger with manual channel and delay mux 100: Auto-trigger with manual channel update. Delay mux is always enabled. 101: Auto-trigger with auto channel update in single-scan event mode. 110: Auto-trigger with auto channel update in multi-scan event mode. 111: Reserved

Reset SCR (Address 09h)

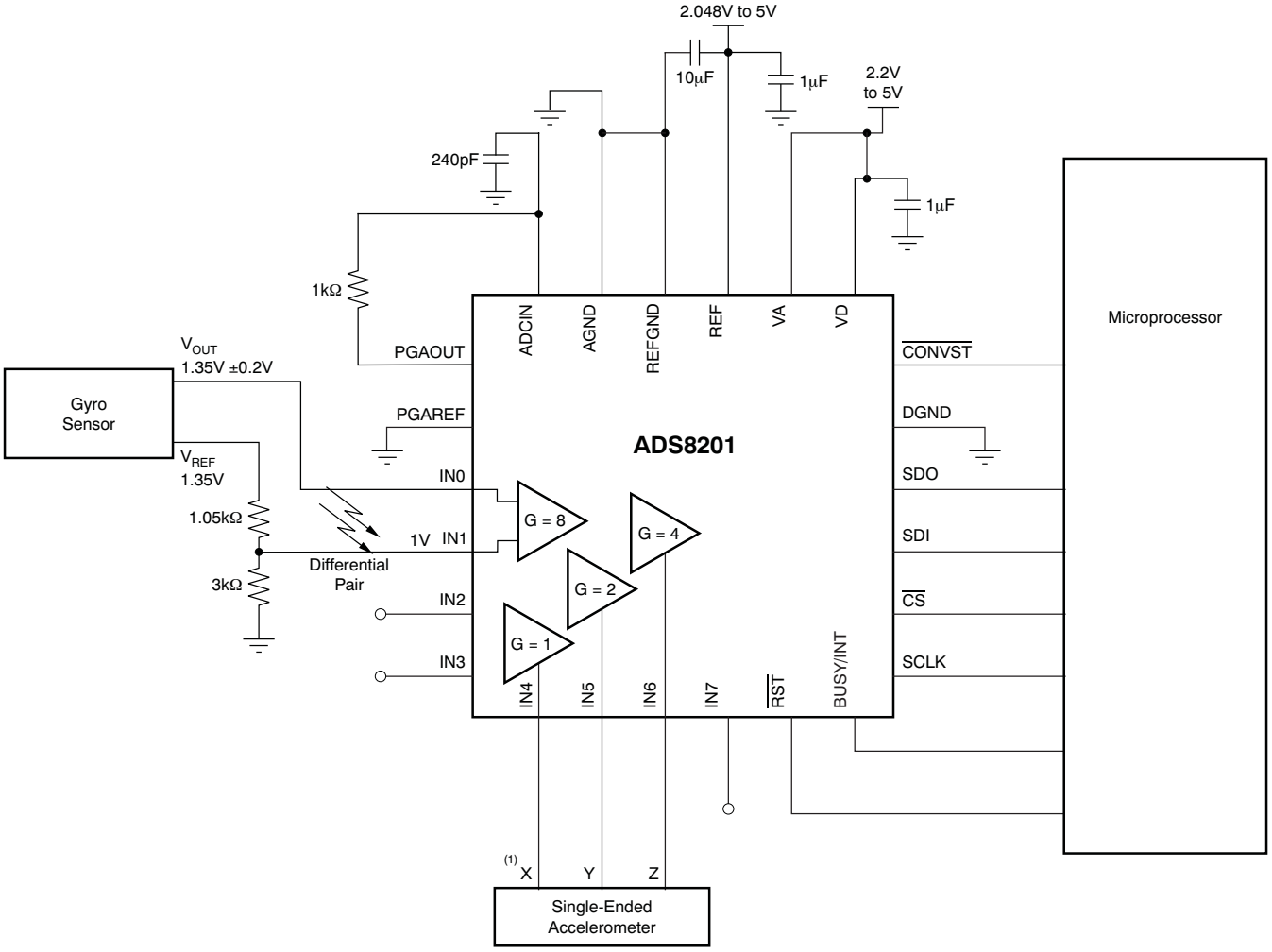
D[7:0]	**Device Reset** Default = 00 Read : Always 00 Write: AAh to reset the device

Conversion Delay SCR (Address 0Ah)

D[7:3]	Not Used				
D[2:0]	Select PGA Delay After Conversion				
	D[2:0]	ACQUISITION TIME (μs)	ADC CONVERSION TIME (μs)	CONVERSION DELAY (μs)	ADC THROUGHPUT (μs)
	000	2.125	3.375	0.5	6
	001	2.125	3.375	2.5	8
	010	2.125	3.375	4.5	10
	011	2.125	3.375	6.5	12
	100	2.125	3.375	8.5	14
	101	2.125	3.375	10.5	16
	110	2.125	3.375	12.5	18
	111	2.125	3.375	14.5	20

APPLICATION INFORMATION

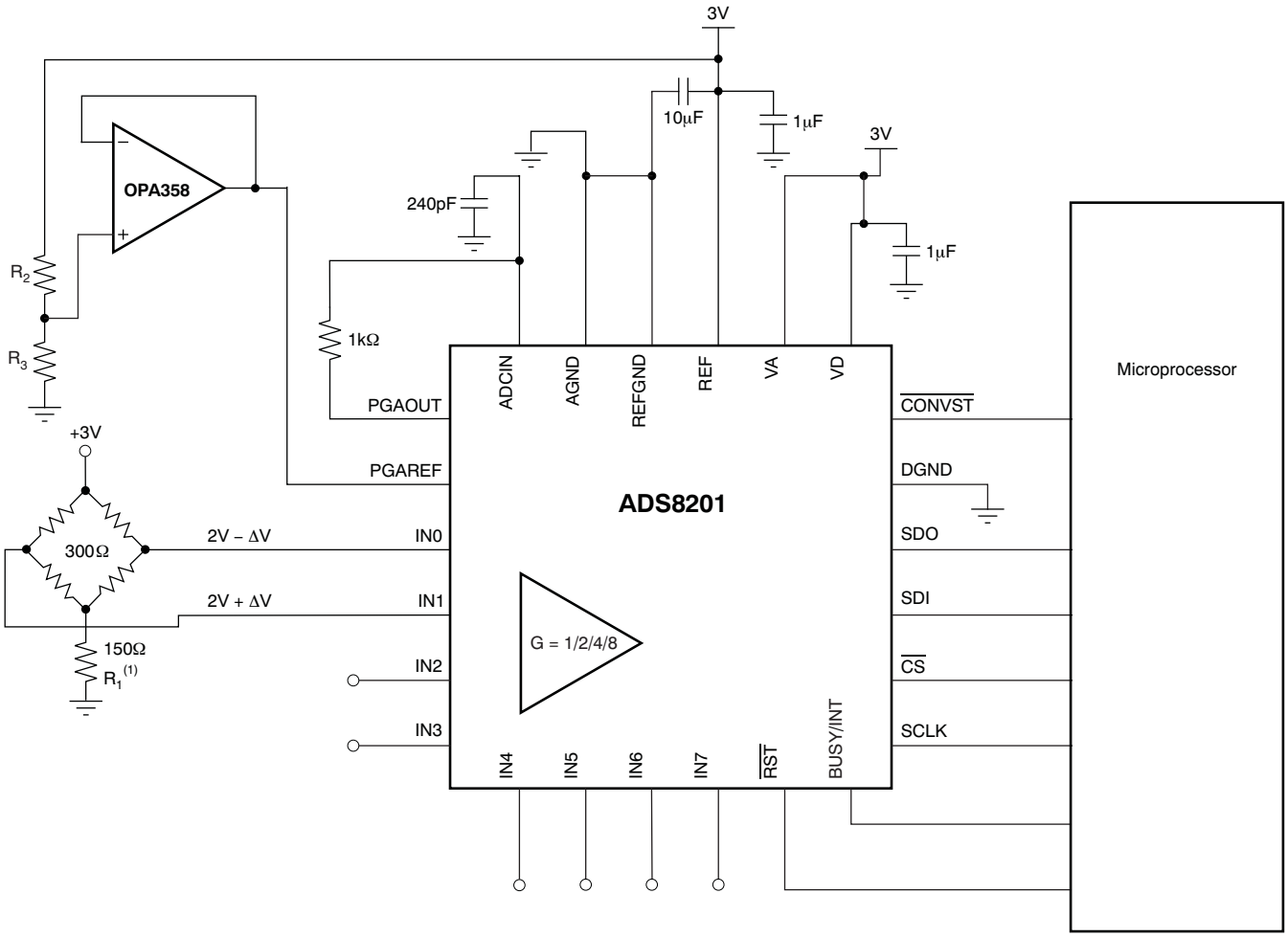
Figure 31 illustrates an example precision positioning application.



(1) X = 100mV < V_{IN} < V_A –100mV; Y = 100mV < V_{IN} < V_A/2; Z = 100mV < V_{IN} < V_A/4

Figure 31. Precision Positioning Application

A bridge sensor application is shown in Figure 32.



(1) R_1 creates proper common-mode voltage only for low-voltage operation.

Figure 32. Bridge Sensor Application

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revision B	Page
• Changed unit, and min and max values for *Offset Error* parameter in *Electrical Characteristics* table	3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8201IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8201
ADS8201IRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8201
ADS8201IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8201
ADS8201IRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

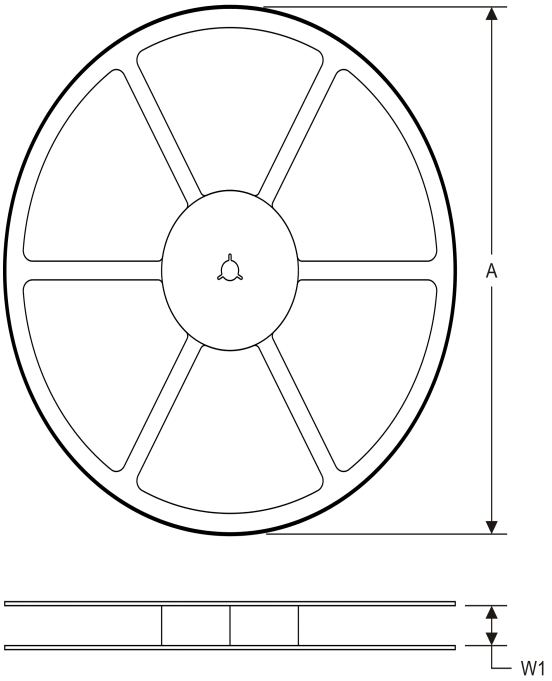
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

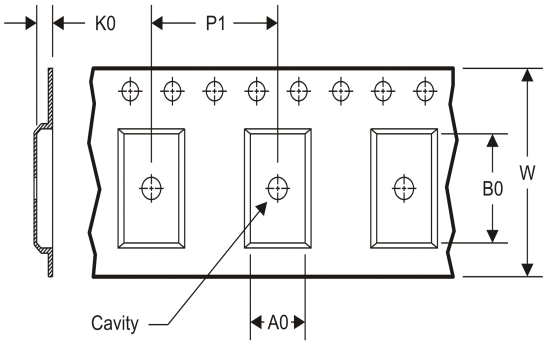
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



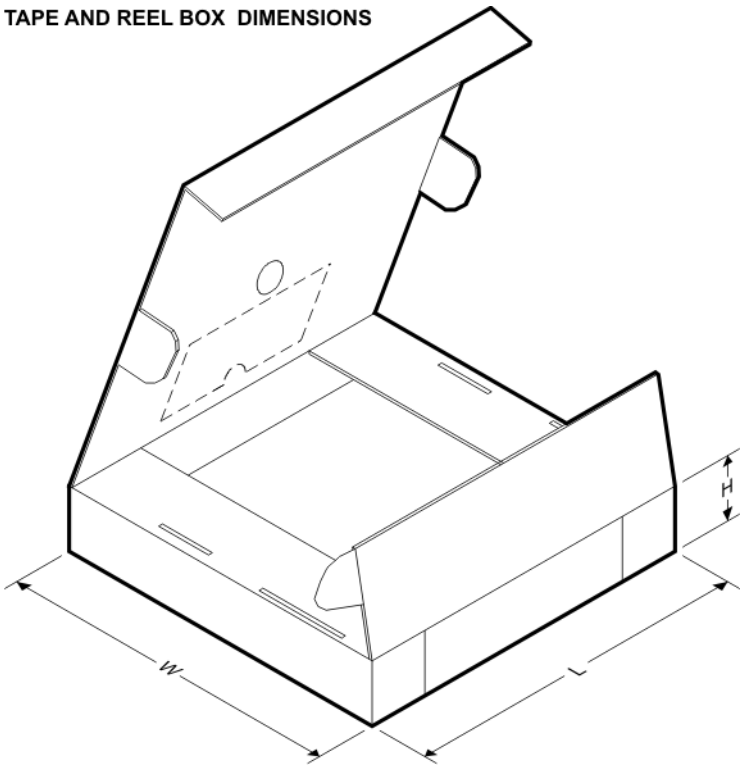
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8201IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8201IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



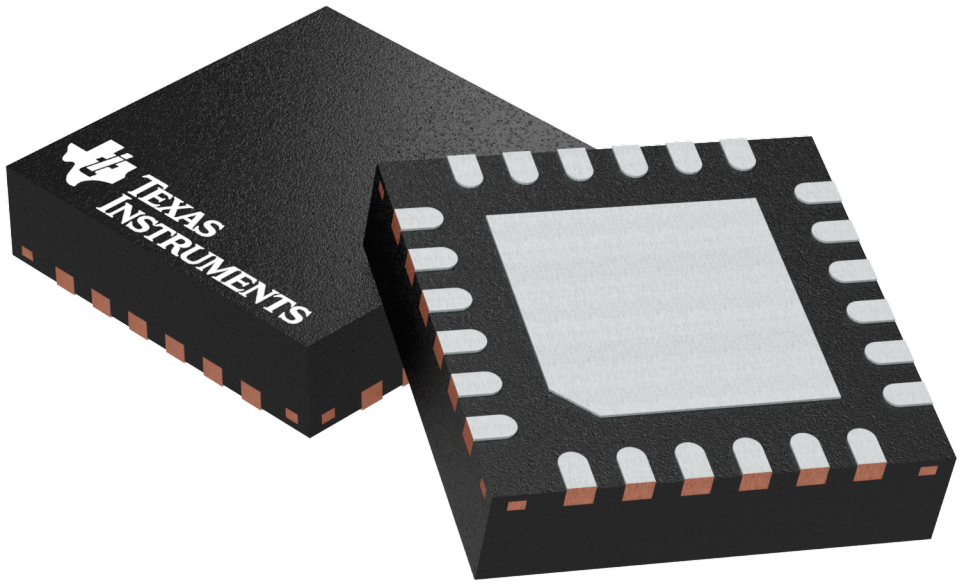
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8201IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8201IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

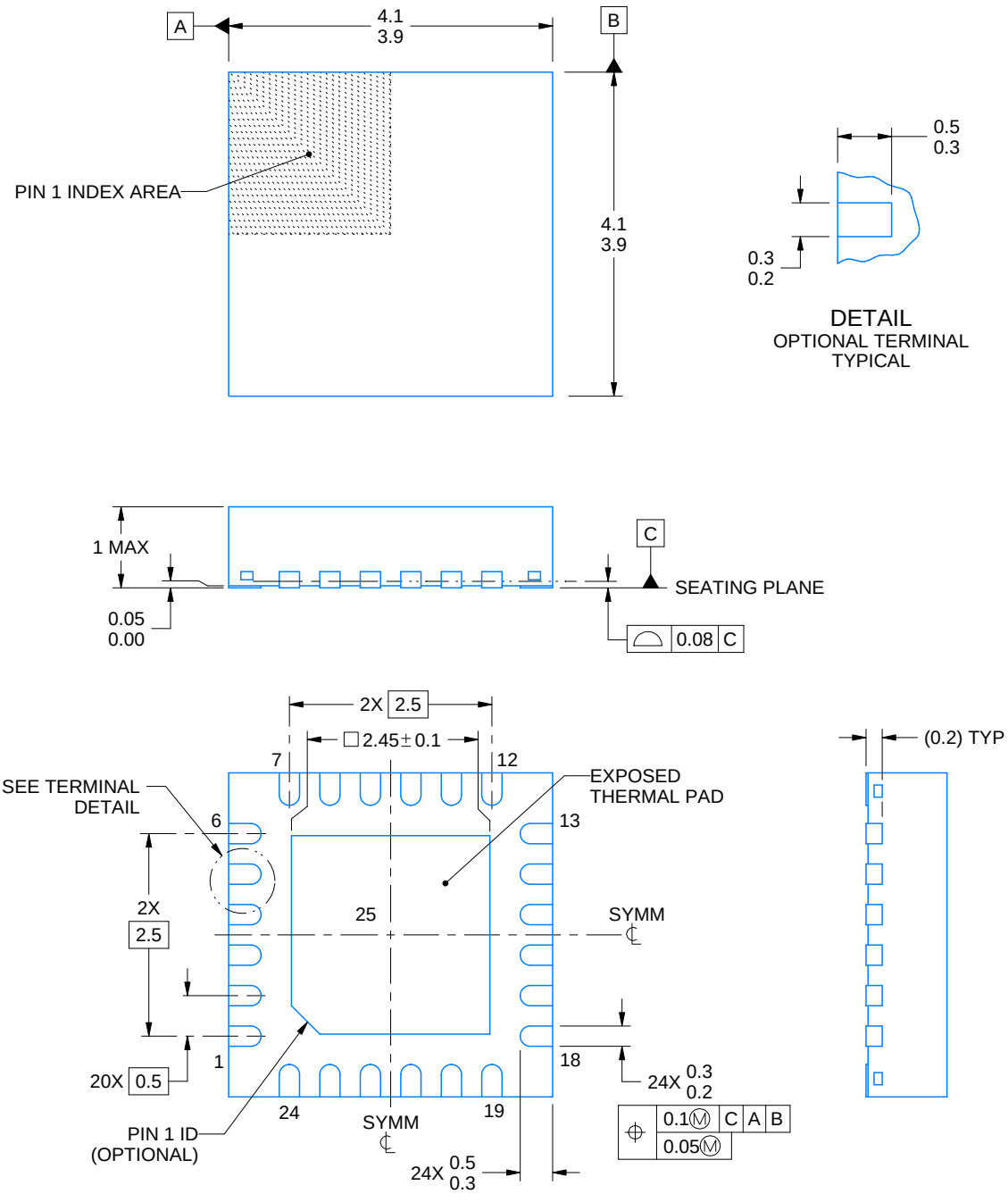
4204104/H

PACKAGE OUTLINE

RGE0024B

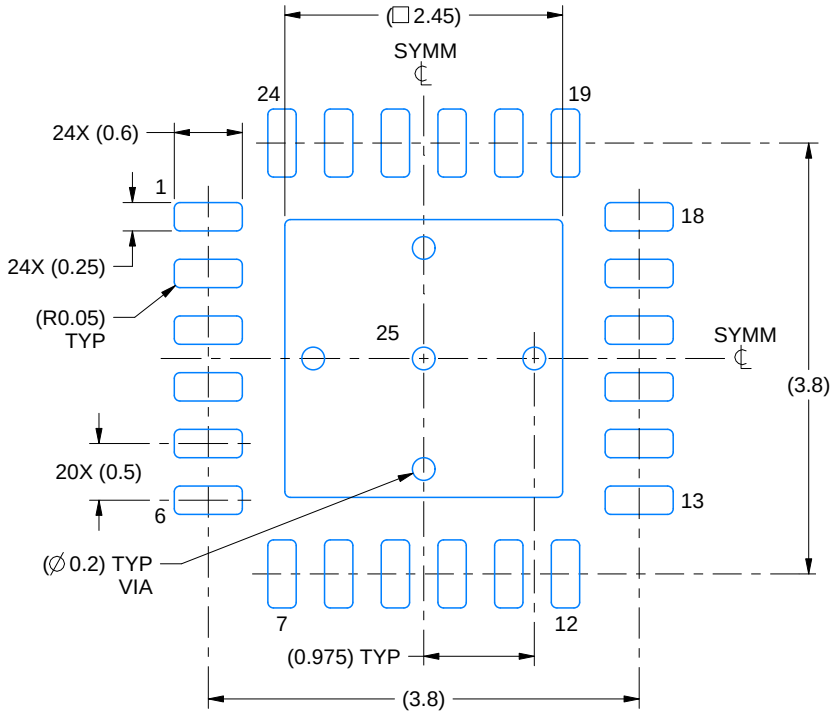
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

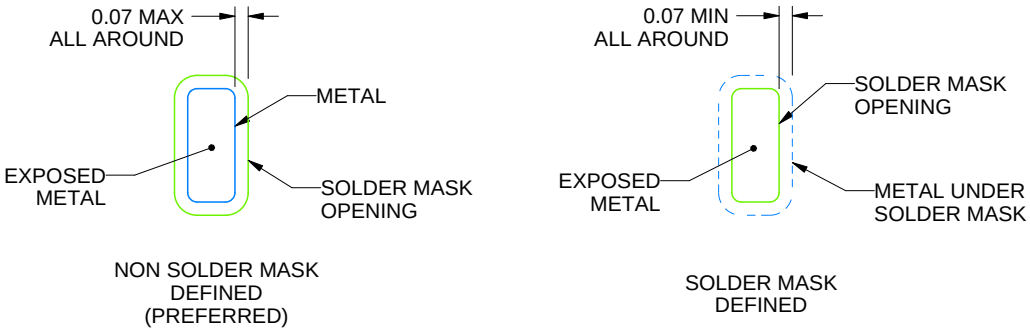


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

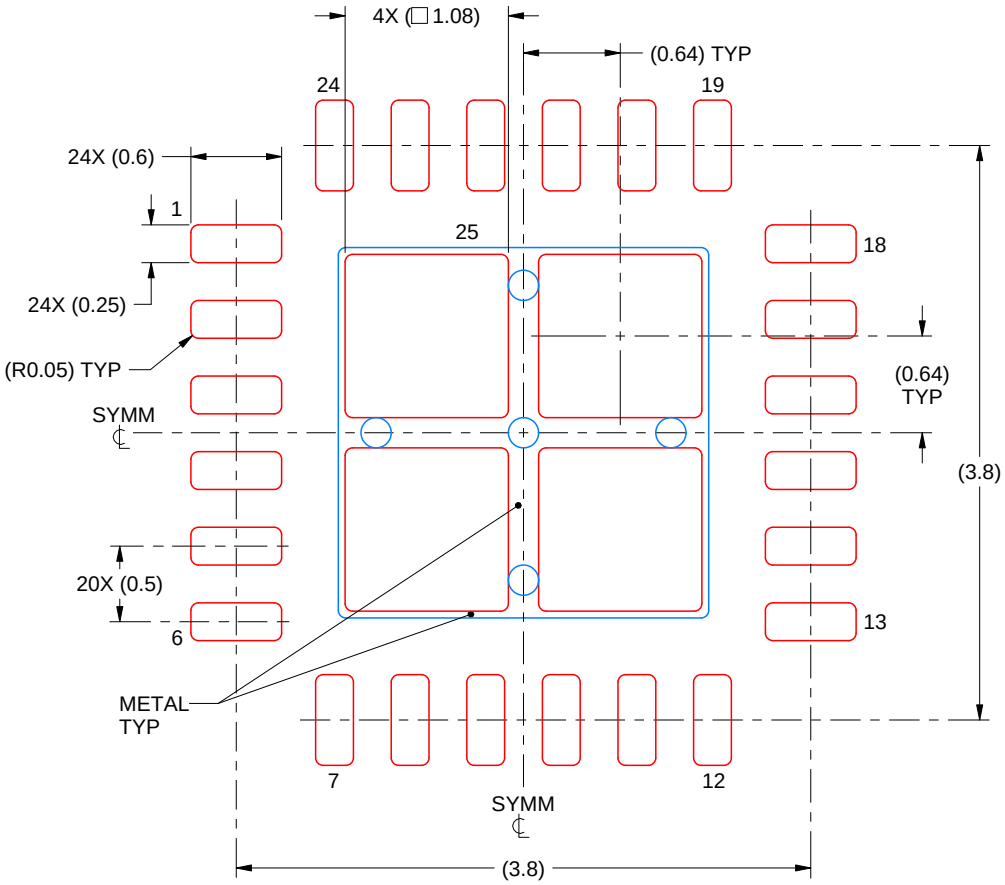


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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