Test Report: PMP41114 3.6kW, 54V, Single-Phase, AC-to-DC Rectifier Reference Design With all GaN Switches



Description

This reference design is a digitally controlled 3.6kW, 54V, single-phase, AC-to-DC rectifier with all GaN switches. This design is a demonstration for modular hardware system common redundant power supply (M-CRPS) with standard form factor. The input stage chooses a single-phase, totem-pole bridgeless power factor correction (PFC), and the output stage chooses a full-bridge, inductor-inductor-capacitor (FB LLC) converter with full-bridge synchronous rectifier (FB SR). The LLC stage efficiency achieved 98.5% at the half load, and the PFC stage efficiency achieved 98.92% at the half load.



Whole Board With Shell

Features

- · System reference design for server power
- 3.6kW, 54V output with 185mm × 73.5mm × 40mm (including case)
- Higher than 80 plus titanium efficiency with all GaN switches
- · Ultra-compact LLC module with PCB windings
- Fully functioning demonstration with Open Compute Project (OCP) M-CRPS standards

Applications

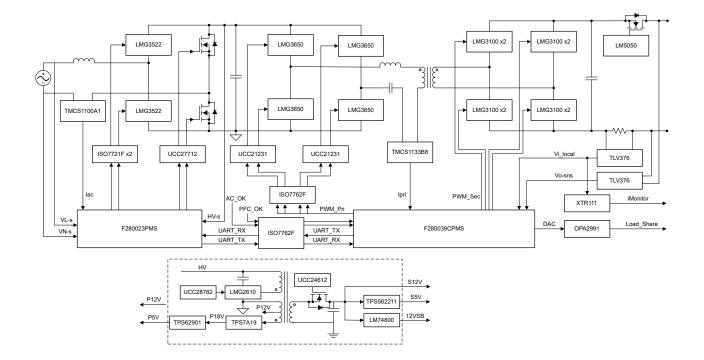
- Rack and server power
- Telecom rectifiers
- Industrial AC-DC



Right Angle of Board

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PMP41114 Detailed Block Diagram



1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

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PARAMETER	SPECIFICATIONS				
Input Voltage	85VAC to 264VAC				
Input Current	0A to 16A				
Main Output Voltage	54VDC				
Main Output Current	0A to 67A				
Standby Output Voltage	12VDC				
Standby Output Current	0A to 3A				

1.2 Required Equipment

- Computer with Code Composer Studio[™] and DigitalPower SDK installed
- Programmable AC power supply, 300V 20A
- Programmable DC power supply, 500V 15A
- Electronic load, 60V 120A
- Dual-channel isolated DC power supply, 12V, 3A
- AC power analyzer
- Oscilloscope (minimum 100MHz bandwidth)
- Current probe (minimum 100kHz bandwidth)
- · Multichannel temperature tester

1.3 Considerations

All testing in this report is done on the LLC stage only, without the PFC stage and auxiliary power stage. TDG supported testing on the ferrite cores in the LLC module. The PMP23338 tool page has information about the PFC stage. See also the PMP23146 tool page for information about the auxiliary power stage. This design is still in development and can be updated in the future, please contact TI to get the latest design file for your development.

1.4 Dimensions

Board size: 159mm × 70mm × 37mm, (open frame without golden finger).

1.5 Test Setup

Figure 1-1 shows the test setup for the LLC stage.

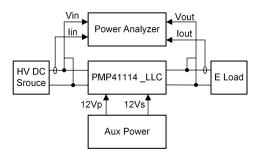


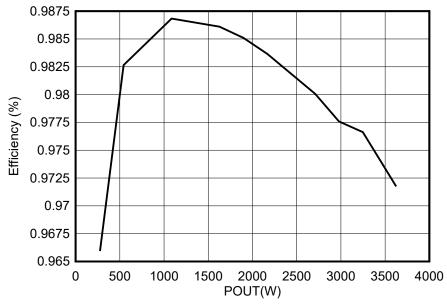
Figure 1-1. Test Setup



2 Testing and Results

2.1 Efficiency Graphs

The efficiency graph represented in Figure 2-1 is tested with the ferrite core of TPG33B, the EC25 shape is used for primary resonant, and the PQ32 shape is used for the transformer.





2.2 Efficiency Data

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Table 2-1 shows the efficiency data of LLC stage.

V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	P _{IN} (W)	P _{OUT} (W)	P _{LOSS} (W)	EFFICIENCY (%)	
399.94	0.15857	54.27	1	63.42	54.27	9.15	85.57%	
399.91	0.7128	55.069	5	285.06	275.35	9.71	96.59%	
399.79	1.3812	54.261	10	552.19	542.61	9.58	98.27%	
399.65	2.7511	54.25	20	1099.48	1085.00	14.48	98.68%	
399.55	4.1295	54.234	30	1649.94	1627.02	22.92	98.61%	
399.5	4.8225	54.225	35	1926.59	1897.88	28.71	98.51%	
399.44	5.519	54.212	40	2204.51	2168.48	36.03	98.37%	
399.32	6.923	54.188	50	2764.49	2709.40	55.09	98.01%	
399.25	8.331	54.14	60	3326.15	3248.40	77.75	97.66%	
399.15	9.348	54.117	67	3731.25	3625.84	105.42	97.17%	

2.3 Thermal Images

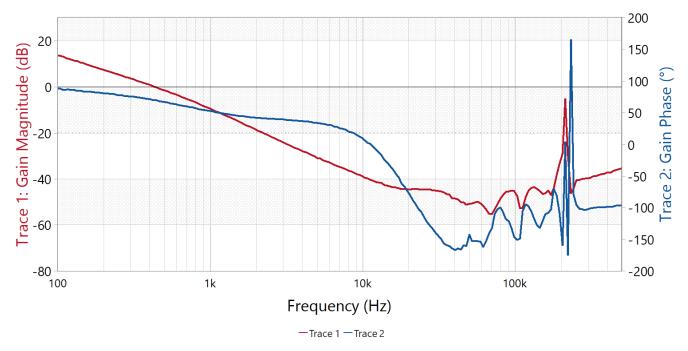
Figure 2-2 shows the thermal image under full load.



Figure 2-2. Thermal Image

2.4 Bode Plots

Figure 2-3 through Figure 2-8 show the PMP41114 Bode plots.





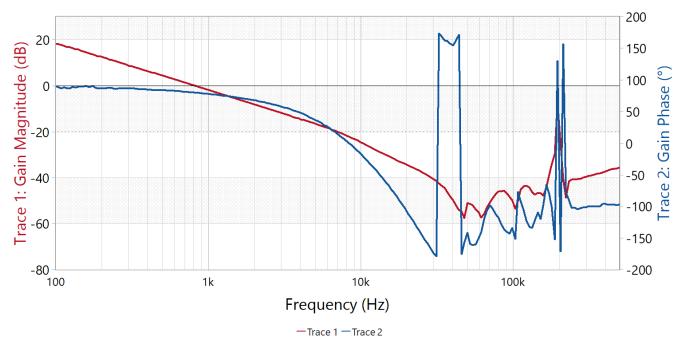


Figure 2-4. Bode Plot With 400V Input and 5A Load



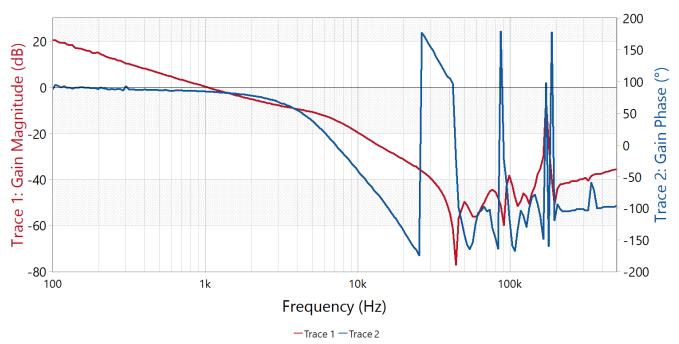


Figure 2-5. Bode Plot With 400V Input and 33.5A Load

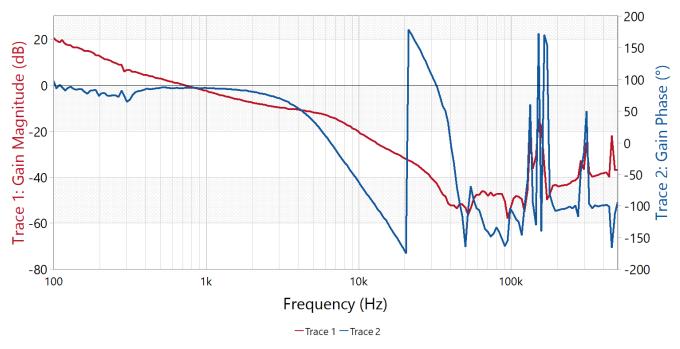
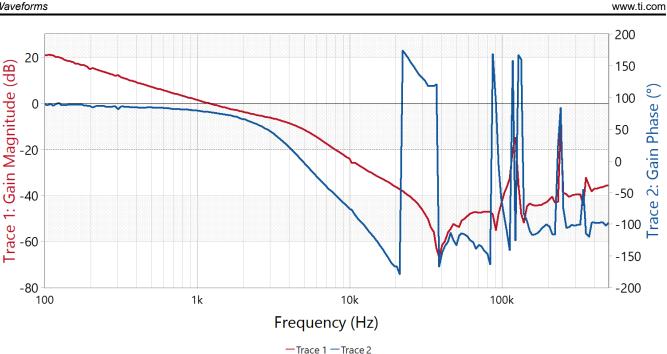
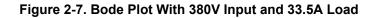


Figure 2-6. Bode Plot With 400V Input and 67A Load

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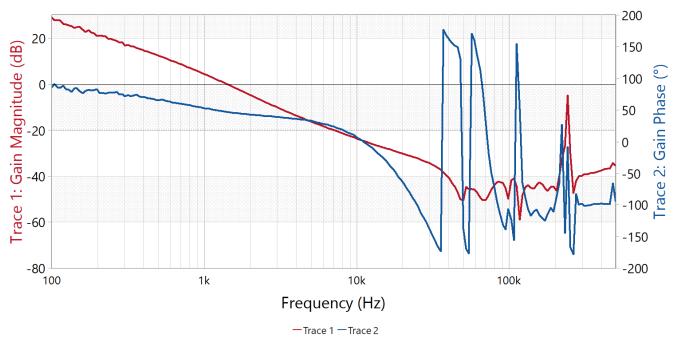


Figure 2-8. Bode Plot With 420V Input and 33.5A Load

3 Waveforms

3.1 Switching

Figure 3-1 through Figure 3-7 show the switching behavior. Each waveform reflects the following parameters:

- Ch 1 (dark blue) is load current
- Ch 2 (light blue) is switching voltage of one primary side half bridge
- Ch 3 (purple) is output voltage
- Ch 4 (green) is resonant current in primary side ٠

Texas Instruments



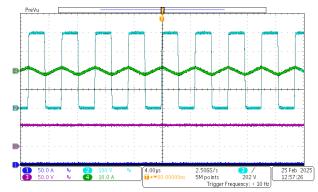


Figure 3-1. Switching Waveform Under 400V Input and No Load

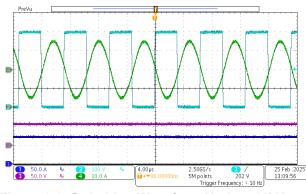


Figure 3-3. Switching Waveform Under 400V Input and 67A Load

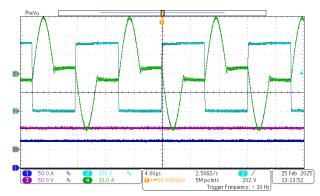


Figure 3-5. Switching Waveform Under 360V Input and 67A Load

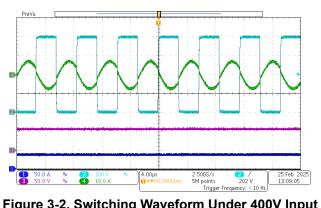


Figure 3-2. Switching Waveform Under 400V Input and 33.5A Load

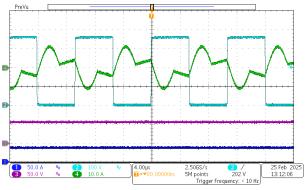


Figure 3-4. Switching Waveform Under 360V Input and 33.5A Load

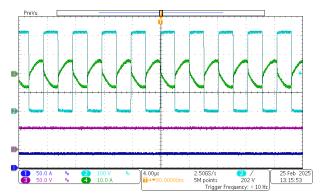


Figure 3-6. Switching Waveform Under 420V Input and 33.5A Load

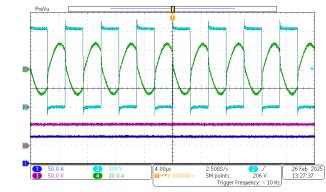


Figure 3-7. Switching Waveform Under 420V Input and 67A Load

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3.2 Output Voltage Ripple

Figure 3-8 through Figure 3-10 show the output voltage ripple. Each waveform reflects the following parameters:

- Ch 3 (purple) is output voltage with ac coupled
- Ch 4 (green) is resonant current in primary side

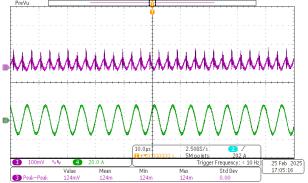


Figure 3-8. Output Voltage Ripple With 400V Input and 67A Load

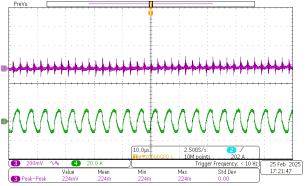


Figure 3-9. Output Voltage Ripple With 420V Input and 67A Load

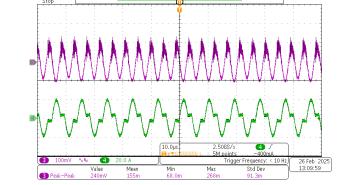


Figure 3-10. Output Voltage Ripple With 380V Input and 67A Load



3.3 Load Transients

Figure 3-11 through Figure 3-13 show the load transient response waveforms.

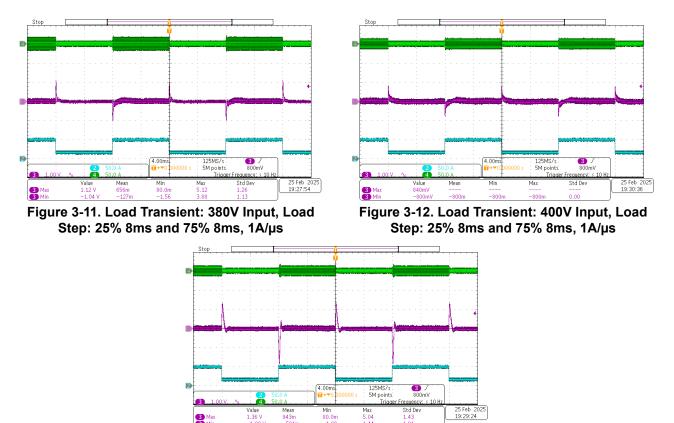


Figure 3-13. Load Transient: 420V Input, Load Step: 25% 8ms and 75% 8ms, 1A/µs

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