Reduce buck-converter EMI and voltage stress by minimizing inductive parasitics

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Introduction

High-frequency conducted and radiated emissions from synchronous buck converters occur based on the transient voltage (dv/dt) and transient current (di/dt) generated during hard switching. Such electromagnetic interference (EMI) is an increasingly vexing issue in the design and qualification cycle, especially given the increased switching speed of power MOSFETs. This article identifies the significant role of power-stage inductive parasitics in EMI generation and offers suggestions for their minimization to reduce the broadband EMI signature.

Critical converter loops with high slew-rate currents

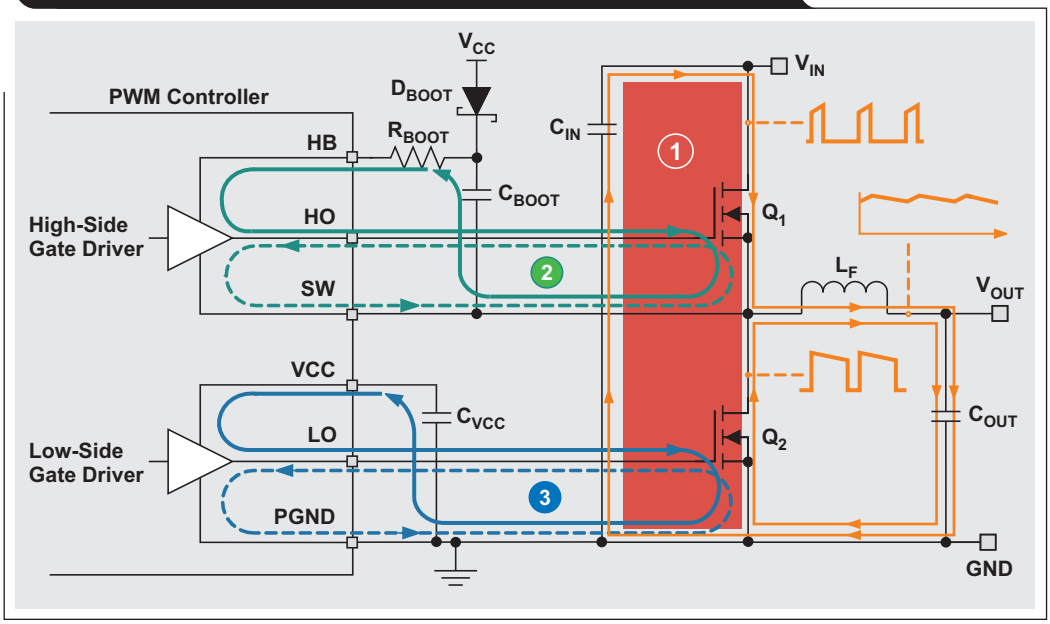
A compact, optimized layout of a power stage lowers EMI for easier regulatory compliance. In translating a converter schematic to a board layout, one essential step is to pinpoint the high slew-rate current loops, with an eye to recognizing the layout-induced parasitic or stray inductances that cause excessive noise, overshoot, ringing and ground bounce.[1]

Consider the turn-on of the high-side MOSFET, Q_1, in the synchronous buck converter of Figure 1. Current flowing originally from source to drain of the synchronous MOSFET, Q_2, ramps to zero, and the current in Q_1 increases to the inductor current level. Hence, the loop shaded in red and labeled "1" in Figure 1 is designated as the high-frequency switching power loop (or "hot" loop).

In contrast, the current flowing in the inductor, L_F, is largely DC with superimposed triangular ripple. The rate of change of the current is inherently limited by the inductor and any parasitic inductance contributed by the series connections is essentially benign.

Loops 2 and 3 in Figure 1 are classified as gate loops for the power MOSFETs. Specifically, loop 2 represents the high-side MOSFET's gate driver supplied by bootstrap capacitor, C_{BOOT}. Likewise, loop 3 corresponds to the low-side MOSFET's gate driver supplied by V_{CC}. The gate turn-on and turn-off current paths are delineated in each case by solid and dashed lines, respectively.

Figure 1. Critical high-frequency AC loops with high slew-rate currents are the power loop and gate-drive loops



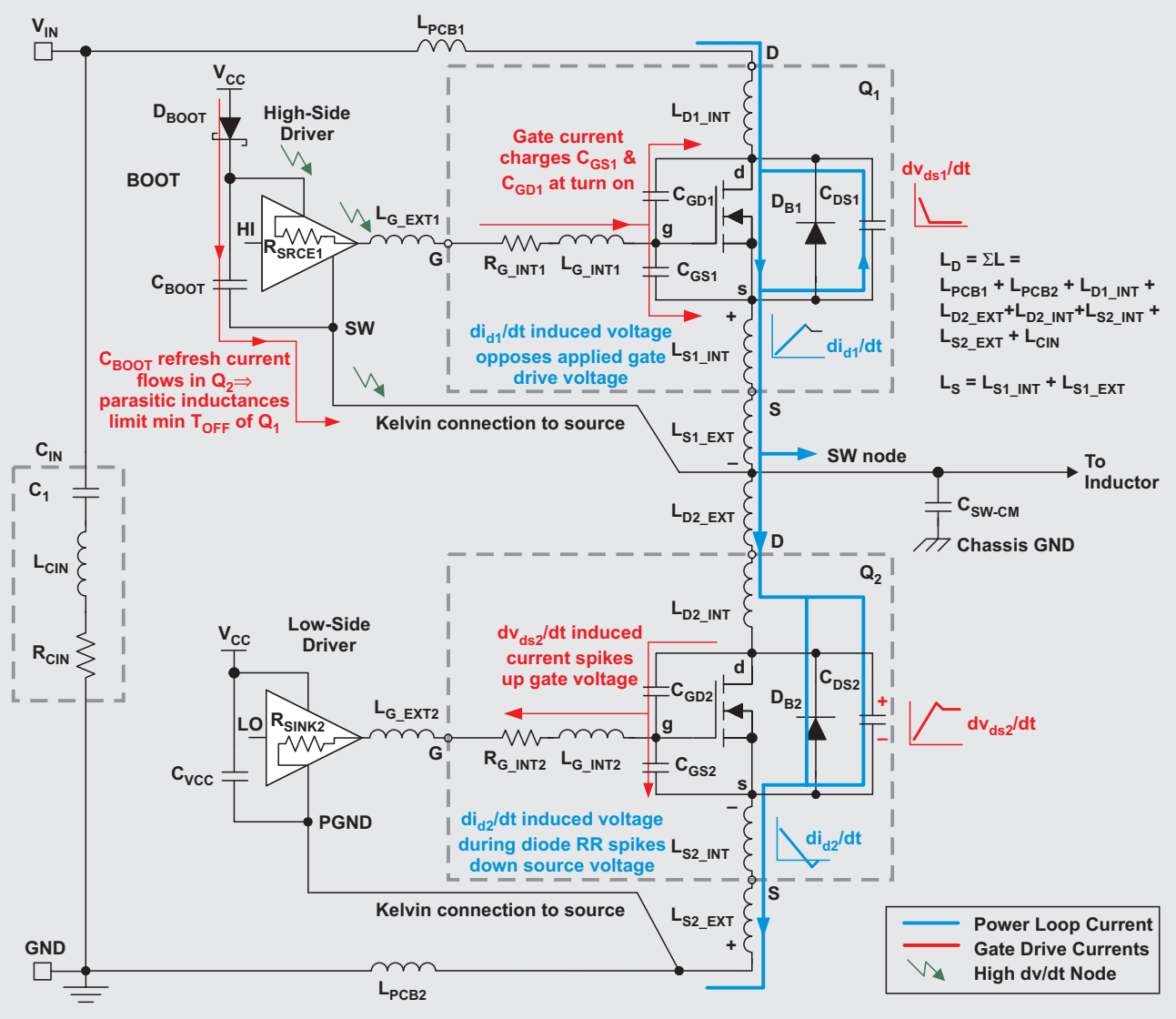
Parasitic inductances

In general, the behavior of MOSFET switching and the consequences for waveform ringing, power dissipation, device stress, and EMI are correlated with the parasitic inductances of the power-loop and gate-drive circuits. Figure 2 provides a comprehensive illustration of the parasitic elements arising from component placement, device package, and printed circuit board (PCB) layout routing that affect switching performance and EMI of the synchronous buck converter.

The effective high-frequency power-loop inductance, L_{LOOP}, is the sum of the total drain inductance, L_D, and the common-source inductance, L_S, that results from the series inductance of the input capacitor and PCB traces, and the package inductances of the power MOSFETs. As expected, the power-loop inductance is highly related to the layout geometry of the input capacitor-MOSFET loop denoted by the red-shaded area in Figure 1.

Meanwhile, the gate-loop self-inductance, L_G, includes lumped contributions from the MOSFET package and PCB trace routing. An inspection of Figure 2 reveals that the common-source inductance of Q_1 exists mutually in both the power and gate loops. It increases switching loss because the di/dt of the power loop creates a negative feedback voltage that impedes rise and fall times of the gate-source voltage. Another factor that leads to increased component stress is the common-source inductance of Q_2, which contributes to spurious turn-on of the low-side MOSFET during body-diode reverse recovery.[2]

Figure 2. MOSFET and gate-driver stage with inductive and capacitive parasitic elements



EMI frequencies and coupling modes

Delineated in Table 1 are the three loosely-defined frequency ranges over which a synchronous buck converter excites and propagates EMI. During MOSFET switching, where the slew rate of the commutating current may exceed 5 A/ns, just 2 nH of parasitic inductance results in a voltage overshoot of 10 V. Furthermore, the current waveforms in the power loop with fast switching edges and leading-edge resonant ringing are rich in harmonic content, posing a severe threat of magnetic field coupling and radiated EMI.

Table 1. Converter EMI frequency classification

Converter Noise Type		Dominant Noise Source	Frequency Range	Conducted/ Radiated Emissions
1	Low-frequency noise	Switching-frequency harmonics	150 kHz to 50 MHz	Conducted
2	Broadband noise	MOSFET voltage and current rise/ fall times, resonant ringing	50 MHz to 200 MHz	Both
3	High-frequency noise	Body-diode reverse recovery	Above 200 MHz	Radiated

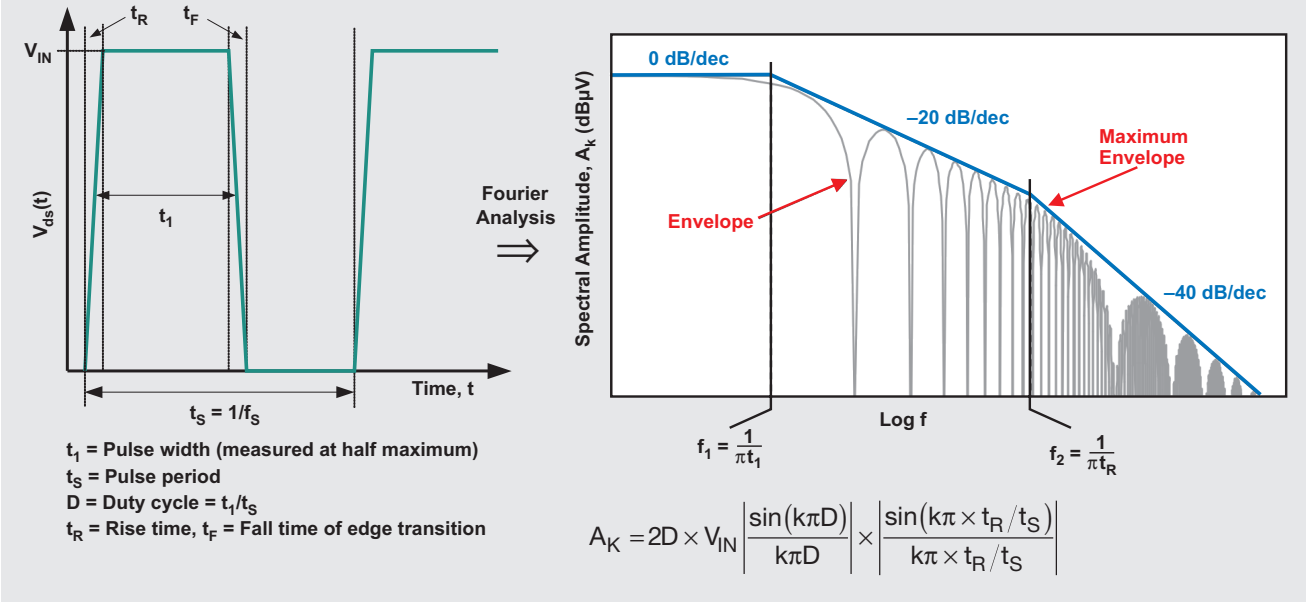
To get an idea of the harmonic frequency amplitudes of the switch (SW) voltage waveform, consider an input having a periodic trapezoidal pulse with finite rise and fall times (Figure 3). Using Fourier analysis, it is shown that the harmonic-amplitude envelope is a double-sinc function with corner frequencies of f_1 and f_2, depending on the pulse width and rise/fall time of the time-domain waveform.[3] A similar analysis applies for the instantaneous current in the power loop.

Three dominant noise-coupling paths are identified as:
(1) conducted noise through the DC input lines;
(2) magnetic field coupling from the power loop; and
(3) electric field coupling from the SW-node copper surface.[4]

Power-loop inductance, L_{LOOP}, increases MOSFET switching loss and the peak drain-to-source voltage spike. It also exacerbates SW-voltage ringing, affecting broadband EMI in the 50- to 200-MHz range. Clearly, it is vital to minimize the effective loop length and enclosed area of the power loop. This reduces parasitic inductance and magnetic field self-cancellation, and makes it possible to reduce the magnetically-coupled radiated energy emanating from what effectively is a loop antenna structure.[3, 4, 5]

Conducted noise coupling is most likely on the converter input side as the ratio of loop inductance and input-capacitor series inductance (ESL) determines the filtering. Reducing L_{LOOP} increases the input-filter attenuation requirement. Fortunately, the noise conducted to the output is minimal if the filter inductor has a high self-resonant frequency (SRF) and also provides high transfer impedance from the SW to V_{OUT} nets. The output noise is additionally filtered by low-impedance output capacitor(s).

Figure 3. The switch-voltage waveform and spectral envelope that depends on pulse width and rise/fall times

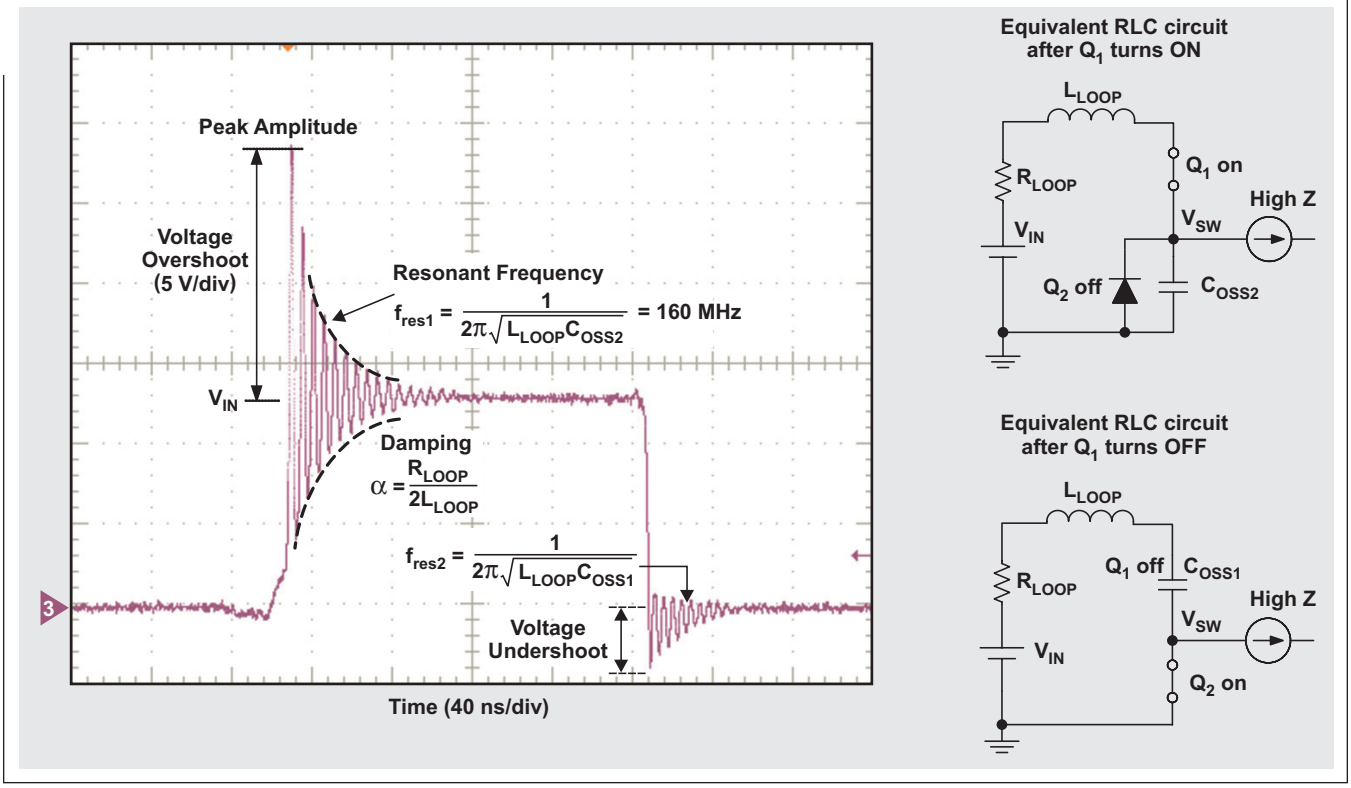


Equivalent resonant circuit

Referring to the SW voltage waveform in Figure 4, a resonance is excited by the parasitic energy stored during MOSFET switching. Simplified equivalent circuits are included on the right side of Figure 4 for analyzing the switching behavior. The switch-voltage overshoot above V_{IN} and undershoot below ground (GND) are evident during the rising and falling edges, respectively. The oscillation amplitude depends on the distribution of partial inductances within the loop, and the subsequent ringing is damped by the effective loop AC resistance. This contributes to voltage stress of the MOSFETs and gate drivers, and it also correlates to the frequency at which the broadband-radiated EMI is centered.[4]

Note that two important aspects during resonance are the resonant frequency and the loss or damping factor at that resonance. The main design goal is to push the resonant frequency as high as possible by minimizing the power-loop inductance. This decreases the stored reactive energy and lowers the resonant peak voltage. Also, the damping factor is increased at a higher frequency due to the skin effect.

Figure 4. Practical SW-node voltage waveform and equivalent RLC circuits for a synchronous buck



EMI mitigation begins at the schematic

When studying a converter schematic prior to PCB layout, it is often convenient to highlight the high-current traces, the high-dv/dt circuit nodes, and the noise-sensitive nets, as shown in Figure 5. This example shows a 2.2-MHz converter intended for noise-sensitive automotive applications that uses a current-mode synchronous-buck controller, such as TI's LM5141-Q1.

EMI mitigation at the PCB

Minimizing the physical size of the loop by paying attention to component placement is central to reducing power-loop impedance. Noise coupling also depends on field distribution and orientation, making design of the PCB's inner layers also important.

A passive shield layer (Figure 6) is established using a ground plane as close as possible to the switching loop by using minimum dielectric thickness. The horizontal current flow on the top layer sets up a vertical flux pattern. The resultant magnetic field induces a current in the shield layer opposite in direction to the current in the switching loop. By Lenz's law, the current in the shield layer generates a magnetic field to counteract the originating magnetic field. The result is H-field self-cancellation that results in lower parasitic inductance relative to what the loop area would suggest.[4]

Having an uninterrupted, continuous shield plane on layer 2 with close proximity to the switching loop offers optimal performance for enhanced suppression of RF energy, and its importance cannot be overstated. Low intra-layer z-axis spacing is specified in the PCB stack-up specification, for example by using a 5-mil core dielectric.[6] Shield-layer effectiveness is maximized by avoiding vias to the extent that all of the noise current is kept on the top layer.

Figure 5. Schematic of synchronous buck converter that shows EMI-related circuit areas

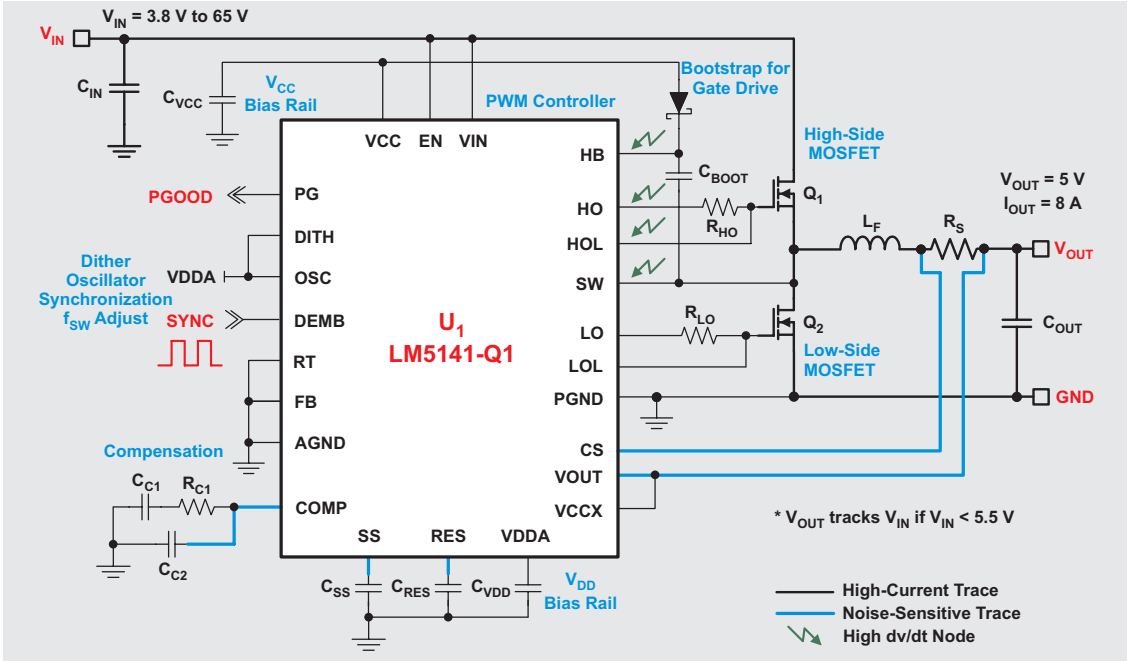
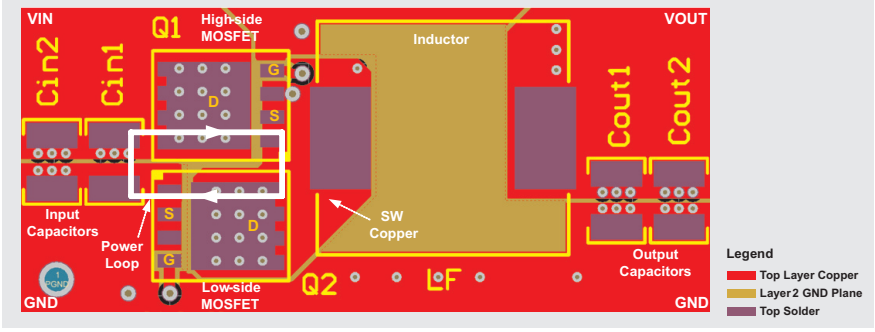


Figure 6. Single-sided power stage component placement (top view)



Provisioning for EMI also places an emphasis on a small SW-node copper area to reduce capacitive coupling related to high-dv/dt SW-node voltage swings. The SW-node copper pour should be short and wide. A full ground plane under the SW node contributes a very small increase in SW-to-GND parasitic capacitance, but is recommended for a multi-layer stack-up PCB to diminish the electrically-coupled radiated energy.[5] A copper-pour keepout is maintained on the top layer under the inductor to minimize capacitive coupling from SW to V_{OUT}.

EMI mitigation using controller features

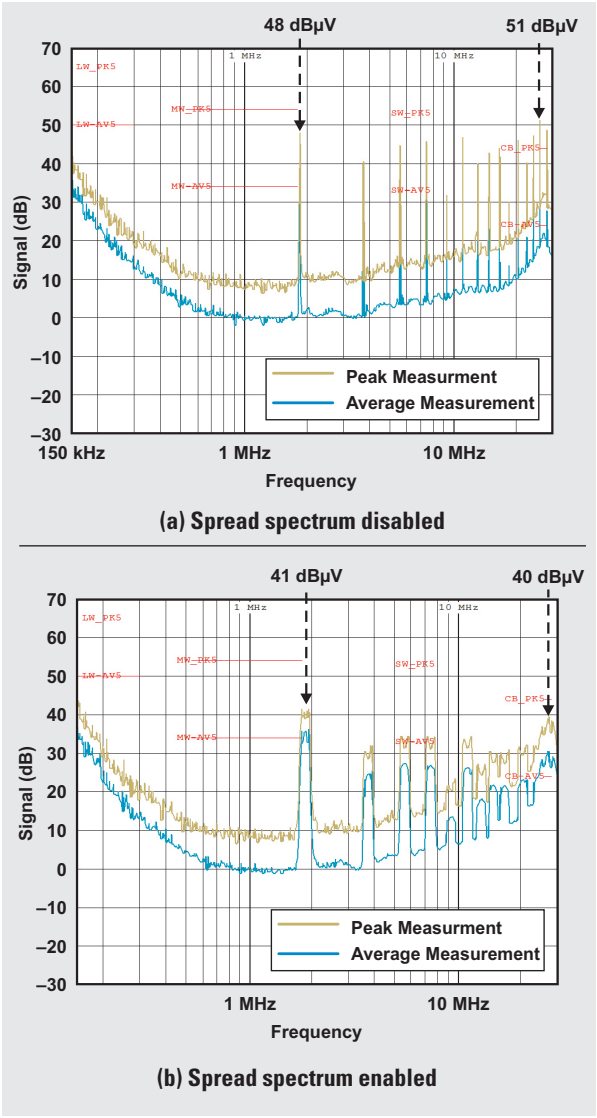
When the PCB layout is fixed, various noise-reduction features integrated in synchronous buck controllers are most useful when dealing with EMI in the latter design stages. For example, the LM5141-Q1 includes asymmetric gate-drive slew-rate control, external clock synchronization, an internal oscillator, and on-the-fly frequency hopping for adaptive tuning to avoid sensitive AM radio bands in automotive systems. Pulse skipping at light loads is inhibited during synchronization, or when the DEMB/SYNC pin is pulled low to reduce noise and RF interference. For added reliability, this device is rated for negative SW-node and gate-drive transients of –5 V with up to 20-ns duration.

To further diminish the EMI signature, a novel technique of spread-spectrum frequency modulation (SSFM), also known as dithering, disperses the spectral energy of the switching signal. Based on the CISPR 25 class 5 automotive specification, Figure 7 shows a substantial improvement in conducted emissions when spread-spectrum is enabled with the LM5141-Q1.

Conclusion

Synchronous buck converters generally switch under 3 MHz, but generate broadband noise and EMI up to 1 GHz. Understanding the key converter switching loops from the schematic and diligently minimizing these loop areas during PCB design is imperative to reduce both conducted and radiated EMI. Controller-integrated EMI mitigation techniques, such as dither and slew-rate control, are convenient options in the latter design phases when a PCB spin is unacceptable.

Figure 7. CISPR 25 class 5 conducted emissions measurement from 150 kHz to 30 MHz



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