Application Report
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Build High-Density, High-Refresh Rate, Multiplexing LED Panel with TLC5958

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ABSTRACT

This application report describes how to build high-density, high refresh rate, multiplexing panel with the TLC5958; a 48 channel, 16-bit ES-PWM LED driver with pre-charge FET, LED open detection and display data memory supporting 32-multiplexing.

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LGSE is a trademark of Texas Instruments.

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1 Introduction

The TLC5958 is a 48 channel, constant-current sink driver for multiplexing system with 1 to 32 duty ratio. Each channel has an individually-adjustable, 65536-step, pulse width modulation (PWM) grayscale (GS).

The 48K bit display memory is implemented to increase the visual refresh rate and to decrease the GS data writing frequency.

The TLC5958 implements Low Gray Scale Enhancement (LGSE™) technology to improve the display quality at low gray scale condition. This feature makes the TLC5958 more suitable for high-density multiplexing application.

The output channels are grouped into three groups, each group has 16 channels. Each group has a 512-step color brightness control (CC) function. The maximum current value of all 48 channels can be set with 8-step global brightness control (BC) function. CC and BC can be used to adjust the brightness deviation between LED drivers. GS, CC, and BC data are accessible via a serial interface port.

The TLC5958 has one error flag: LED open detection (LOD), which can be read via a serial interface port. The TLC5958 also has a power-save mode that sets the total current consumption to 0.8 mA (typ) when all outputs are off.

The TLC5958 has the following features:

- 48 channels constant current sink output
- Low Gray Scale Enhancement (LGSE™) technology
- Sink Current Capability with Max BC/CC data:
  - 25 mA at 5 VCC
  - 20 mA at 3.3 VCC
- Global Brightness Control (BC): 3 bit (8 Step)
- Color Brightness Control (CC) for Each Color Group: 9-Bit (512 Step), Three Groups
- Grayscale (GS) control with multiplexed enhanced spectrum (ES) PWM: 16 bit
- 48K bit Grayscale data memory support 32-multiplexing
- LED power-supply voltage up to 10 V
- Vcc = 3.0 V to 5.5 V
- Constant current accuracy
  - Channel to Channel = ±1% (Typ), ±3% (Max)
  - Device to Device = ±1% (Typ), ±2% (Max)
- Data Transfer Rate: 25 MHz
- Gray Scale Clock: 33 MHz
- LED Open Detection (LOD)
- Thermal Shut Down (TSD)
- Iref resistor Short Protection (ISP)
- Power-Save Mode (PSM) with high speed recovery
- Delay switching to prevent inrush current
- Pre-charge FET to avoid ghosting phenomenon
- Operating temperature: –40°C to 85°C

The TLC5958 is mainly targeted for the following applications:

- LED video displays with multiplexing system
- LED signboards with multiplexing system
- High refresh rate and high-density LED panels

Figure 1 is a typical application circuit of the TLC5958.

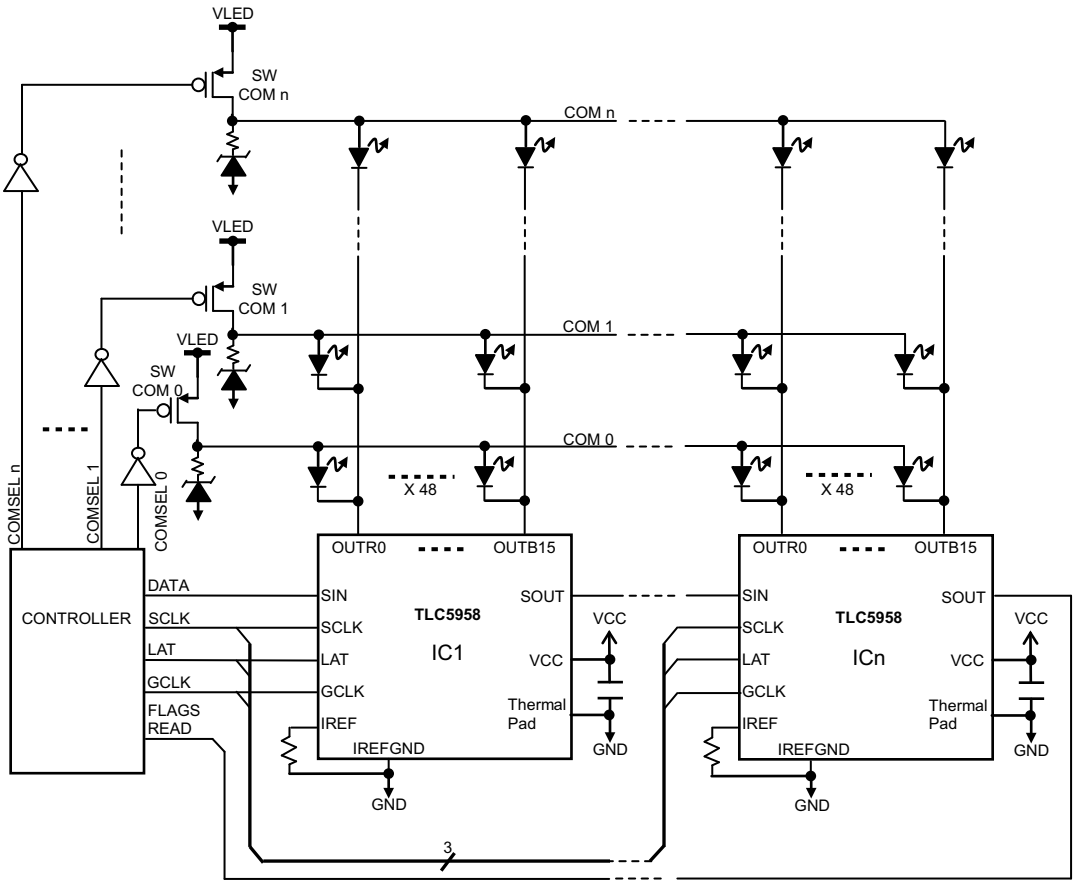


Figure 1. Typical Application Circuit (Multiple Daisy Chained TLC5958s)

2 Device Specification

2.1 Basic Information

Basic information, such as electrical characteristics, thermal package information, and recommended operation conditions, can be found in (SLVSCE7).

The TLC5958 functional block diagram, pin-out information, and pin description is also found in the datasheet (SLVSCE7).

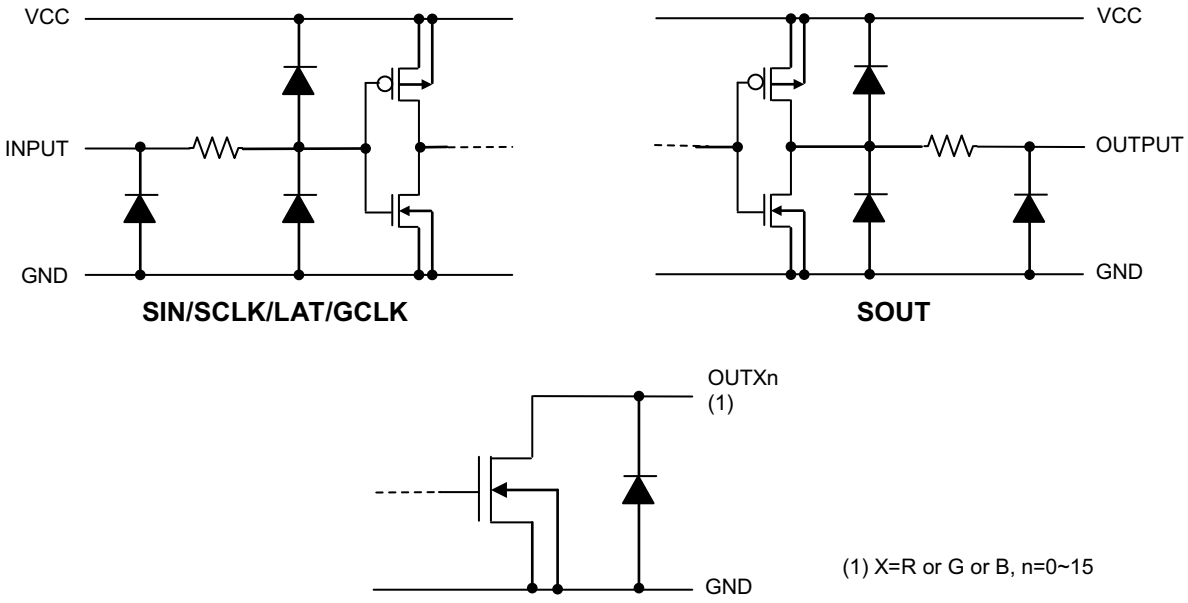
2.2 Switching Characteristics

At V_{CC} = 3.0–5.5 V, T_A = –40–85°C, C_L = 15 pF, R_L = 4 kΩ, target at 1 mA IoLC, VLED = 5.0 V. Typical values are at VCC = 3.3 V, T_A = +25°C(unless otherwise noted)

Parameter		Test Conditions		MIN	TYP	MAX	Unit
t_{R0}	Rise time	SOUT			2	5	ns
t_{R1}		OUTx0–15, x = R/G/B, BC = 7h, CCR/G/B = 1FFh, RIREF = 7.41 kΩ (25-mA target), T_A = +25°C, R_L = 160 Ω			30		ns
t_{F0}	Fall time	SOUT			2	5	ns
t_{F1}		OUTx0–15, x = R/G/B, BC = 4h, CCR/G/B = 1FFh, RIREF = 12 kΩ(10-mA target), T_A = +25°C, R_L = 400 Ω			20		ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT, SEL_TD0 = 00b			15		ns
		SCLK↑ to SOUT, SEL_TD0 = 01b			23		ns
		SCLK↑ to SOUT, SEL_TD0 = 10b			32		ns
		SCLK↓t o SOUT, SEL_TD0 = 11b			12		ns
t_{D1}		LAT↓ to SOUT, ReadFC1/2, ReadSID			26	50	ns
t_{D2}		GCLK↓ to OUTR0/7/8/15 turn on or turn off	RIREF = 7.41 kΩ (25-mA target), BC = 7h, CCR/G/B = 1FFh, T_A = +25°C, SEL_GDLY = 1		13		ns
t_{D3}		Propagation delay time between group and next group (OUTR0/7/8/15 turn-on/off to OUTR1/6/9/14 turn-on/off; OUTR1/6/9/14 turn-on/off to OUTR2/5/10/13 turn-on/off; OUTR2/5/10/13 turn-on/off to OUTR3/4/11/12 turn-on/off)			5		ns
t_{D4}		Propagation delay time between color and next color in same group (OUTRx turn-on/off to OUTGx turn-on/off; OUTGx turn-on/off to OUTBx turn-on/off, x = 0 – 15)			1.67		ns

2.3 Parameter Measurement Information

2.3.1 Pin Equivalent Input and Output Schematic Diagrams



(1) X = R or G or B, n = 0–15

Figure 2. Pin Schematic Diagrams

2.3.2 Test Circuit

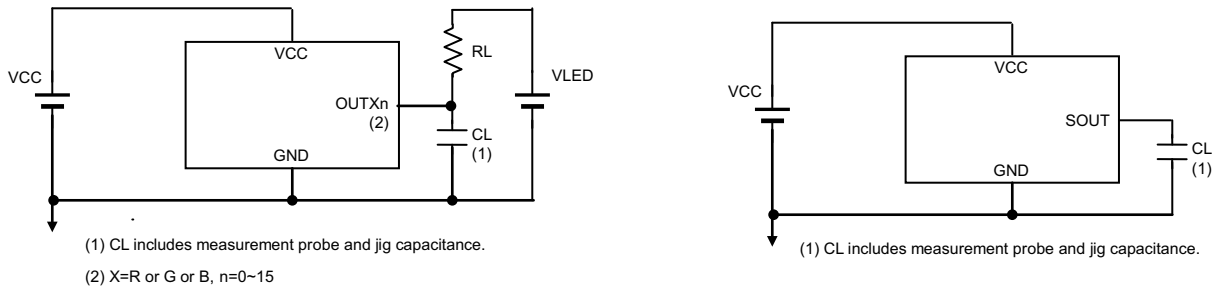
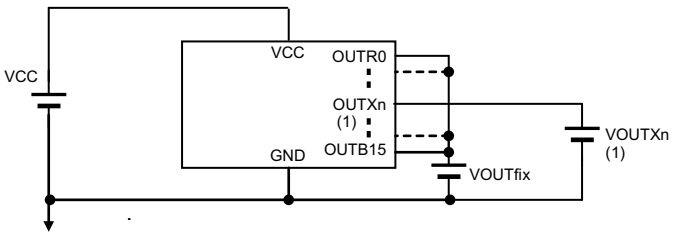


Figure 3. Rise Time and Fall Time Test Circuit

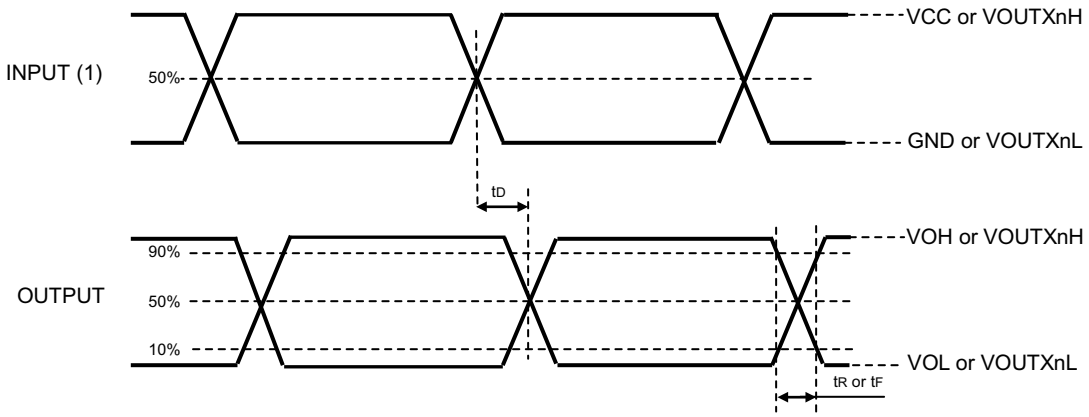


(1) X = R or G or B, n = 0–15

Figure 4. Constant Current Test Circuit for OUTXn

2.4 Timing Diagrams

t_{R0}, t_{R1}, t_{F0}, t_{F1}, t_{D0}, t_{D1}, t_{D2}, t_{D3}, t_{D4}



(1) Input pulse rise and fall time is 1–3 ns.

(2) X = R or G or B, n = 0–15

Figure 5. Output Timing

3 Detailed Description

3.1 How to use the TLC5958

After power on, all OUTXn of the TLC5958 are turned off. All the internal counters and function control registers (FC1/FC2) are initialized. The following steps summarize operation of the TLC5958, providing a general idea how this part works. After that, the function block related to each step is detailed in following sections.

1. According to required LED current, choose BC and CC code, select the current programming resistor R_{IREF}.
2. Send WRTFC command to set FC1/2 register value if the default value needs to change.
3. Write GS data of all lines (max 32 lines) into one of the two memory BANKs.
4. Send Vsync command, the BANK with the GS data just written is displayed.
5. Input GCLK continuously, 257GCLK (or 513GCLK) as a segment. Between the interval of two segments, supply voltage should be switched from one line to next line accordingly.
6. During the same period of step 5, GS data for the next frame should be written into another BANK.
7. When the time of one frame ends, the Vsync command should be input to swap the purpose of the two BANKs.

Repeat step 5–7…

3.2 Step 1 — Choose BC and CC, Select R_{IREF}

3.2.1 What is BC Function?

The TLC5958 is able to adjust the output current of all constant-current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs is programmed with a 3-bit word, thus, all output currents can be adjusted in 8 steps from 12.9% to 100% (see Table 2) for a given current programming resistor (R_{IREF}).

BC data can be set via the serial interface. When the BC data changes, the output current also changes immediately. When the device is powered on, the BC data in the function control(FC) register FC1 is set to 4h as the initial value.

3.2.2 What is CC Function?

The TLC5958 is able to adjust the output current of each of the three color groups OUTR0-OUTR15, OUTG0-OUTG15, and OUTB0-OUTB15 separately. This function is called *color brightness control* (CC). For each color, there is a 9-bit data latch CCR, CCG, or CCB in FC1 register (see Table 4 for FC1 register bit assignment). Thus, all color group output currents can be adjusted in 512 steps from 0% to 100% of the maximum output current, I_{OLCMax}. See next section for more details about I_{OLCMax}. The CC data are entered via the serial interface. When the CC data changes, the output current also changes immediately.

When the IC is powered on, the CC data are set to '100h'. Equation 1 calculates the actual output current.

$$Iout\ (mA) = I_{OLCMax}\ (mA) \times (CCR/511d \text{ or } CCG/511d \text{ or } CCB/511d) \quad (1)$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by BC data and R_{IREF} (see Equation 2)
CCR/G/B = the color brightness control value for each color group in the FC1 register (000h to 1FFh)

Table 1 shows the CC data versus the constant-current against I_{OLCMax}.

Table 1. CC Data vs Current Ratio and Set Current Value

CC Data (CCR or CCG or CCB)			Ratio of Output Current to IolcMax(%, typical)	Output Current (mA, RIREF = 7.41 kΩ)	
Binary	Decimal	HEX		BC = 7h (IolcMax = 25 mA)	BC = 0h (IolcMax = 3.2 mA)
0 0000 0000	0	0	0	0	0
0 0000 0001	1	1	0.2	0.05	0.006
0 0000 0010	2	2	0.4	0.1	0.013
—	—	—	—	—	—
1 0000 0000 (Default)	256 (Default)	100 (Default)	50.1	12.52	1.621
—	—	—	—	—	—
1 1111 1101	509	1FD	99.6	24.9	3.222
1 1111 1110	510	1FE	99.8	24.95	3.229
1 1111 1111	511	1FF	100	25	3.235

3.2.3 How to Select R_{IREF} for a given BC

The maximum output current per channel, I_{OLCMax}, is decided by a resistor, R_{IREF}, which is placed between the IREF and IREFGND pins, and the BC code in FC1 register (see Table 4 for FC1 register bit assignment). The voltage on IREF is typically 1.2 V. R_{IREF} can be calculated by Equation 2.

$$Riref\ (k\Omega) = Viref(V) / I_{OLCMax}(mA) \times Gain \quad (2)$$

Where:

V_{IREF} = the internal reference voltage on IREF (1.20 V, typical)
I_{OLCMax} is the largest current for each output at CCR/G/B = 1FFh.
Gain = the current gain at a selected BC code (see Table 2)

Table 2. Current Gain Versus BC Code

BC Data		Gain	Ratio of Gain/Gain_max (at Max BC[1])
Binary	HEX		
000 (recommend)	0 (recommend)	20	12.90%
1	1	39.5	25.60%
10	2	58.6	37.90%
11	3	80.9	52.40%
100 (default)	4 (default)	100	64.70%
101	5	113.3	73.30%

(1) Recommend to use smaller BC code for better performance. For noise immunity purpose, suggest R_{IREF} < 60 kΩ.

Table 2. Current Gain Versus BC Code (continued)

BC Data		Gain	Ratio of Gain/Gain_max (at Max BC[1])
Binary	HEX		
110	6	141.6	91.70%
111	7	154.5	100%

3.2.4 How to Choose BC/CC for Different Application

BC is mainly used for global brightness adjustment between day and night. Suggested BC is 4h, which is in the middle of the range, thus, one can change brightness up and down flexibly.

CC can be used to fine tune the brightness in 512 steps, this is suitable for white balance adjustment between RGB color group. To get a pure white color, the general requirement for the luminous intensity ratio of R, G, B LED is 3:6:1. Depending on LED's characteristics (Electro-Optical conversion efficiency), the current ratio of R, G, B LED will be much different from this ratio. Usually, the Red LED will need the largest current. One can choose 511d (the max value) CC code for the color group which need the largest current at first, then choose proper CC code for the other two color groups according to the current ratio requirement of the LED used.

3.2.4.1 Example 1: Red LED Current is 20 mA, Green LED Needs 12 mA, Blue LED Needs 8 mA

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 x 12 mA / 20 mA = 306.6, thus, choose 307d for CCG. With same method, choose 204d for CCB.
3. According to the required red LED current, choose 7h for BC.
4. According to Equation 2, Riref = 1.2 V / 20 mA × 154.5 = 9.27 kΩ.

In this example, we choose 7h for BC, instead of using the default 4h. This is because that the Red LED current is 20 mA, which is approaching the upper limit of current range. To prevent the constant output current from exceeding the upper limit in case a larger BC code is input accidently, we choose the max BC code here.

3.2.4.2 Example 2: Red LED Current is 5 mA, Green LED Needs 2 mA, Blue LED Needs 1 mA

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 x 2 mA / 5 mA = 204.4, thus choose 204d for CCG. With same method, choose 102d for CCB.
3. According to the required Blue LED current, choose 0h for BC.
4. According to Equation 2, Riref = 1.2 V / 5 mA x 20 = 4.8 kΩ.

In this example, we choose 0h for BC, instead of using the default 4h. This is because the Blue LED current is 1 mA, which is approaching the lower limit of current range. To prevent the constant output current from exceeding the lower limit in case a lower BC code is input accidently, the min BC code is selected here.

In general, if LED current is in the middle of the range (that is, 10 mA), one can just use the default 4h as BC code.

3.3 Step 2 — Write Function Control Register FC1 and FC2

3.3.1 Input Data for FC1/2 Through Common Shift Register

The common shift register is 48 bits long and is used to shift data from the SIN pin into the TLC5958. The data shifted into the register can be latched into GS memory unit, or latched into function control (FC) registers FC1/2 depending on which command is received.

Figure 6 shows the configuration of the common shift register and the data latches.

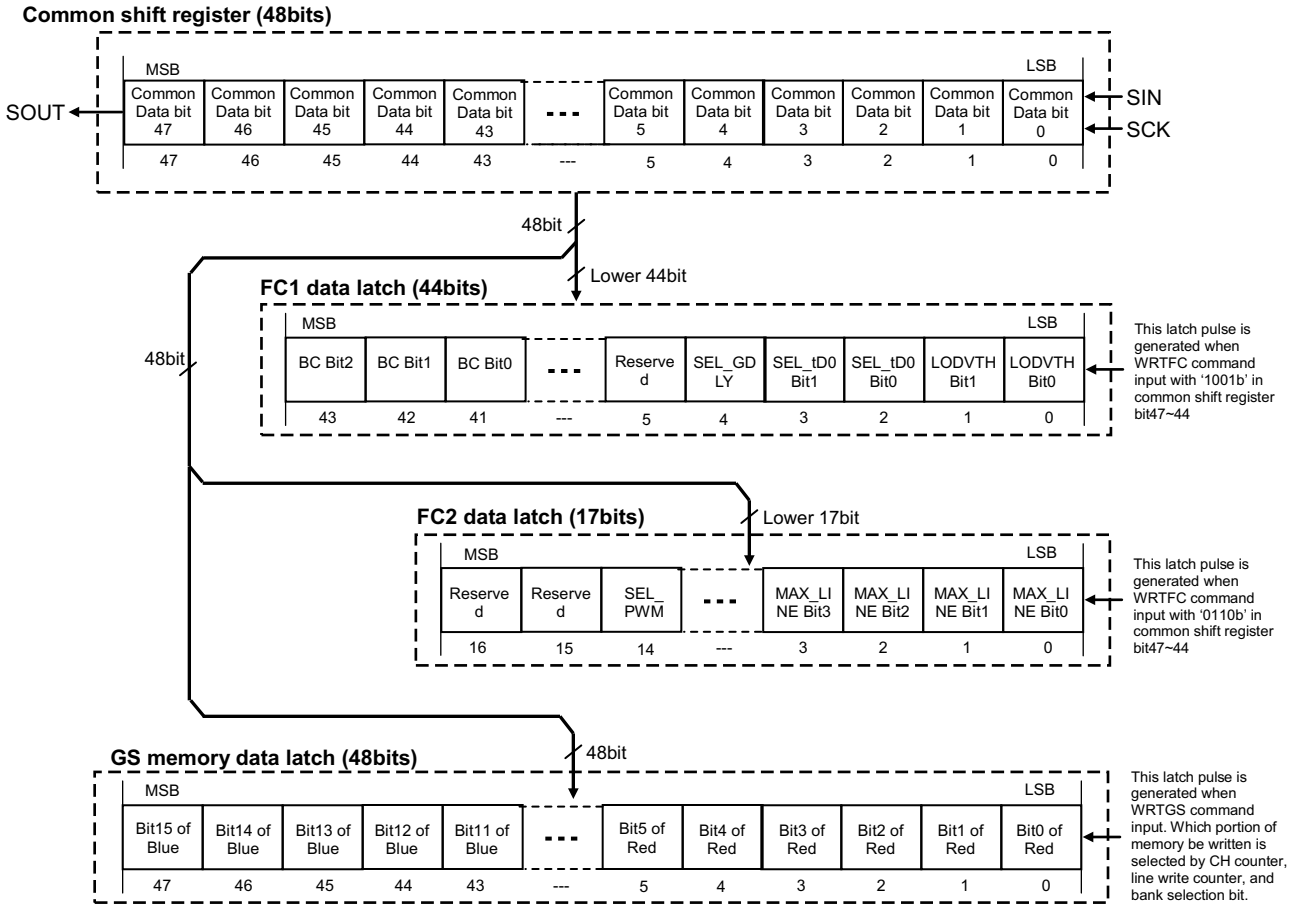


Figure 6. Common Shift Register and Data Latch Configuration

The LSB of the common shift register is connected to SIN and the MSB is connected to SOUT. On each rising edge of SCLK, the data on SIN are shifted into the LSB and all 48 bits are shifted towards the MSB. The register MSB is always connected to SOUT.

When the device is powered on, all 48 bits of the common shift register are set to '0'.

3.3.2 How to Write Function Control Register

TLC5958 use commands FCWRTEN and WRTFC to latch the data of common shift register into FC1/FC2. These commands are distinguished by the number of SCLK rising edge included in the LAT pulse. Table 3 describes more about these two commands.

Table 3. WRTFC/FCWRTEN Commands Description

Command Name	SCLK Rising Edges While LAT is High	Description
WRTFC (FC data write)	5	The lower 44-bit data or the lower 17-bit data in common shift registers are copied to the FC1 or FC2 register. Bit47–44 of the common shift register will be used to choose which FC register be written to. If '1001b' is received for bit47–44 of common shift register, then the lower 44-bit in common shift register will be copied to FC1 register. If '0110b' is received for bit47–44 of common shift register, then the lower 17-bit in common shift register will be copied to FC2 register. Refer to Figure 7 for a timing diagram of this command operation.
FCWRTEN (FC write enable)	15	FC writes are enabled by this command. This command must always be input before the FC data write occurs. Refer to Figure 7 for a timing diagram of this command operation.

Note that the FCWRTEN command must be input before inputting the WRTFC command, otherwise this WRTFC command will be neglected.

When inputting the WRTFC command, the bit47–bit44 of common shift register is used to choose which FC register be written to. See Table 3 for more details.

Refer to Figure 7 for a detailed command input timing diagram.

3.3.3 Function Control (FC) Register FC1

FC1 is used to select BC/CC code, group delay, low grayscale enhancement feature, and LED open detection (LOD) voltage.

Table 4 shows the FC1 register bit assignment.

Table 4. FC1 Register Bit Assignment

Bit No.	Bit Name	Default Value (Binary)	Description
1-0	LODVTH	01b	LOD detection threshold voltage. These two bits select the detection threshold voltage for the LED open detection (LOD). Table 5 shows the detect voltage truth table.
32	SEL_TD0	01b	TD0 select. SOUT hold time is decided by TD0 definition and selection. Table 6 shows the detail.
4	SEL_GDLY	1b	Group delay select. When this bit is '0', there is no delay between channels. All channels turn on at same time. When this bit is '1', channels turn on with different delay times, thus the inrush current is minimized. See Table 7 for more detail.
6-5	LGSE1-B	00b	Low Gray Scale Enhancement for blue color, can be used to solve the 1st line issue which commonly happens in high density, multiplexing panel, also is helpful for the white balance at low grayscale condition. The functionality is as follows: 00b — no enhancement 01b — weak enhancement 10b — medium enhancement 11b — strong enhancement
7	RSV	0b	Reserved data. Don't care.
9-8	LGSE1-G	00b	Low Gray Scale Enhancement for green color, can be used to solve the 1st line issue which commonly happens in high density, multiplexing panel, also is helpful for the white balance at low grayscale condition. The functionality is as follows: 00b — no enhancement 01b — weak enhancement 10b — medium enhancement 11b — strong enhancement
10	RSV	0b	Reserved data. Don't care.
12-11	LGSE1-R	00b	Low Gray Scale Enhancement for red color, can be used to solve the 1st line issue commonly happens in high density, multiplexing panel, also is helpful for the white balance at low grayscale condition. The functionality is as follows: 00b — no enhancement 01b — weak enhancement 10b — medium enhancement 11b — strong enhancement
13	RSV	0b	Reserved data. Don't care.
22 - 14	CCB	1 0000 0000b	Color brightness control data for BLUE color group (Data = 000h-1FFh. See Table 1)
31 - 23	CCG	1 0000 0000b	Color brightness control data for GREEN color group (Data = 000h-1FFh. See Table 1)
40 - 32	CCR	1 0000 0000b	Color brightness control data for RED color group (Data = 000h-1FFh. See Table 1)
43 - 41	BC	100b	Global brightness control data for all output (Data = 0h- 7h. See Table 2)

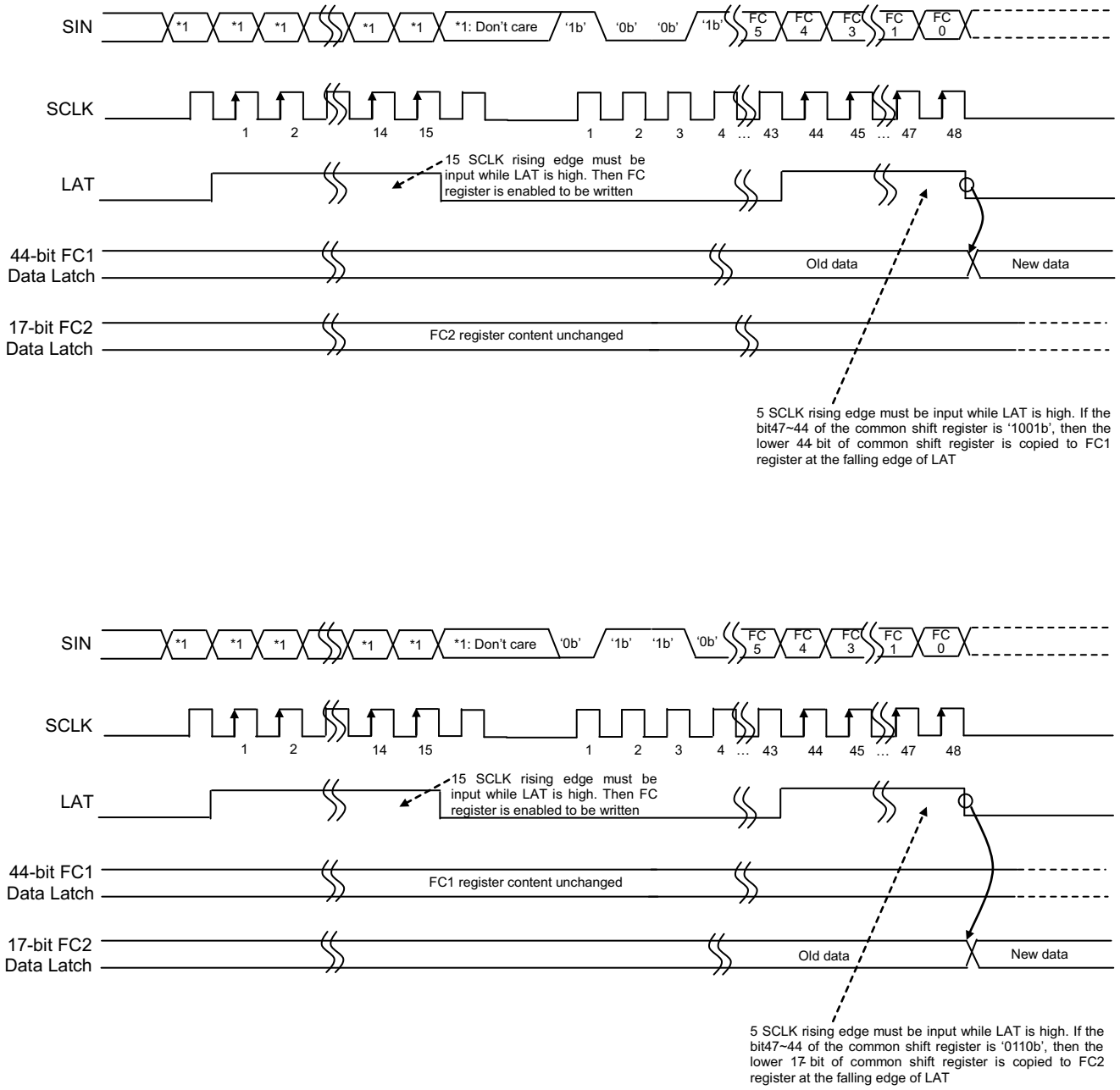


Figure 7. FC Write Enable (FCWRTEN) and FC Data Write (WRTFC) Command

Table 5. LOD Threshold Voltage Truth Table

LODVTH		LED Open Detection (LOD) Threshold Voltage
Bit1	Bit0	
0	0	VLOD0 (0.10 V typ)
0	1	VLOD1 (0.25 V typ, Default value)
1	0	VLOD2 (0.40 V typ)
1	1	VLOD3 (0.50 V typ)

Table 6. TD0 Definition and Selection

SEL_TD0		TD0 Definition and Selection
Bit3	Bit2	
0	0	TD0 is the time from SCLK↑ to SOUT↑↓, typical value 15 ns. Once SCLK↑ is received, with 15 ns delay, SOUT begins to change.
0	1	TD0 is the time from SCLK↑ to SOUT↑↓, typical value 23 ns (default value when power up). Once SCLK↑ is received, with 23 ns delay, SOUT begins to change.
1	0	TD0 is the time from SCLK↑ to SOUT↑↓, typical value 32 ns. Once SCLK↑ is received, with 32 ns delay, SOUT begins to change.
1	1	TD0 is the time from SCLK↓ to SOUT↑↓, typical value 12 ns. Once SCLK↓ is received, with 12 ns delay, SOUT begins to change. One can adjust the hold time from SCLK↑ to SOUT↑↓ by changing duty of SCLK

Table 7. Group Delay When SEL_GDLY = 1

Output Pins	Delay Time From GCLK↑ to Output Channel Turn On/Off (ns)
OUTR0/7/8/15	tD2
OUTG0/7/8/15	tD2 + 1.67
OUTB0/7/8/15	tD2 + 3.34
OUTR1/6/9/14	tD2 + 5
OUTG1/6/9/14	tD2 + 5 + 1.67
OUTB1/6/9/14	tD2 + 5 + 3.34
OUTR2/5/10/13	tD2 + 10
OUTG2/5/10/13	tD2 + 10 + 1.67
OUTB2/5/10/13	tD2 + 10 + 3.34
OUTR3/4/11/12	tD2 + 15
OUTG3/4/11/12	tD2 + 15 + 1.67
OUTB3/4/11/12	tD2 + 15 + 3.34

3.3.4 Function Control (FC) Register FC2

FC2 is used to select ES-PWM mode, pre-charge function, power save mode, and the multiplexing ratio. Table 8 shows the FC2 register bit assignment.

Table 8. FC2 Register Bit Assignment

Bit Number	Bit Name	Default Value (Binary)	Description
4-0	MAX_LINE	0 0000b	Multiplexing ratio select. Based on the multiplexing ratio in real application, correct scan line number should be selected here. Table 9 shows the scan line number vs MAX_LINE setting.
5	PSAVE_ENA	0b	Power Save mode select. When this bit is '0', power save function is disabled. This is the default value when power is on. When this bit is '1', power save function is enabled. The TLC5958 will enter power save mode if all '0' GS data is input. If detect a non '0' GS data input, normal mode will be resumed. Refer to Figure 26 for the timing diagram of enter/exit power save mode.
6	SEL_GCLK_EDGE	0b	GCLK edge select. When this bit is '0', OUTn only turns on/off at the rising edge of GCLK, this is the default setting; When this bit is '1', OUTn turns on/off at both edge (rising and falling) of GCLK. At this condition, the maximum input GCLK is 16.5 MHz.
7	SEL_PCHG	0b	Pre-charge working mode select. When this bit is '1': After power on, Pre-charge FET is enabled. When 1st GCLK input, pre-charge FET is turned off and stays off until this segment finished (257th GCLK in 8+8 mode, or 513th GCLK in 9+7 mode). Once this segment finished, Pre-charge FET is turn on again. This means the Pre-charge FET keep off during whole segment period, and remains on during the dead-time (the time between two adjacent segments). When this bit is '0': After power on, Pre-charge FET is enabled. When 1st GCLK input, the pre-charge FET state will depends on the GS data. If GS = 0, then the pre-charge FET will always keep on. If GS>0, the Pre-charge FET will be turn off, and will be turn on again once the output channel is turn off. This means the Pre-charge FET will only keep off during the period in which the channel is on. See Figure 27 for more detail.
10-8	RSV	All 0b	Reserved data. Don't care.
11	EMI_REDUCE_B	0b	EMI reduce select for blue channels. When this bit is '0', EMI noise contributed by blue channels will be reduced. When this bit is '1', EMI noise contributed by blue channels is at default value. However, low grayscale visual effect will be better.
12	EMI_REDUCE_G	0b	EMI reduce select for green channels. When this bit is '0', EMI noise contributed by green channels will be reduced. When this bit is '1', EMI noise contributed by green channels is at default value. However, low grayscale visual effect will be better.
13	EMI_REDUCE_R	0b	EMI reduce select for red channels. When this bit is '0', EMI noise contributed by red channels will be reduced. When this bit is '1', EMI noise contributed by red channels is at default value. However, low grayscale visual effect will be better.
14	SEL_PWM	0b	ES-PWM mode select. When this bit is '0', 8MSB + 8LSB mode is chosen. The whole 65536 GCLK display period is divided into 256 segments. Each segment include 257 GCLK. LED turn on time is scattered in these 256 segments. When this bit is '1', 9MSB + 7LSB mode is chosen. The whole 65536 GCLK display period is divided into 128 segments. Each segment include 513 GCLK. LED turn on time is scattered in these 128 segments. See Section 3.6.2 "Multiplexed Enhanced Spectrum(ES) PWM Control" for more detail.
16 - 15	LGSE2	00b	Besides LGSE1-R/G/B in FC1, these two bits will also improve the first line issue at low grayscale condition. 00b — no improvement 01b — weak improvement 10b — medium improvement 11b — strong improvement

Table 9. Scan Line Number vs MAX_LINE Setting

MAX_LINE (Bit4–Bit0)	Scan Line Number
0 0000b	1
0 0001b	2
0 0010b	3
—	—
0 1111b	16
—	—
1 1101b	30
1 1110b	31
1 1111b	32

3.4 Step 3 — Write GS Data into one Memory BANK

3.4.1 Overview of the Memory Structure

The bottleneck for a traditional PWM LED driver to realize a high visual refresh rate is the GS data transmission limitation. To remove this limitation, the TLC5958 has 48K bit display memory implemented. With this memory size, a multiplexing LED display system with from 1 up to 32 duty ratio (that is, 32 multiplexing) is supported.

The memory is divided into two BANKs: BANK A and BANK B. One is read for current display image, the other one is written with GS data of next display image. This BANK selection is decided by BANK_SEL bit which is an internal flag bit. At power on, BANK_SEL = 0, thus BANK A is selected to be written with GS data for next frame, while the GS data in BANK B is read out for current frame display. When the time of one frame elapsed, Vsync command (see Section 3.4.2 for detail) should be input, and the usage of these two BANKs will be exchanged. By this method, TLC5958 can display the image of current frame at a very high refresh rate, without the limitation of GS data transmission. See Figure 8 for this BANK select mode change.

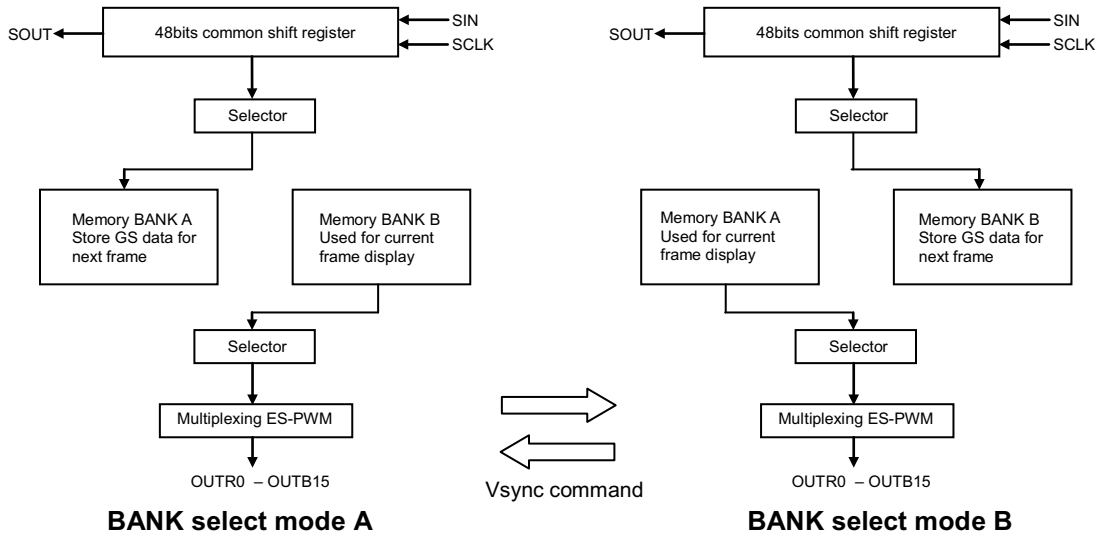


Figure 8. BANK Select Mode Change

3.4.2 What's Vsync Command?

Vsync is the Vertical Frame Synchronization command. When the period of one frame ends, this command should be input to exchange the usage of the two memory BANKs, then the new image in the other BANK is displayed in the coming frame period.

If 3 SCLK rising edges are detected during LAT high period, then TLC5958 considers this as a Vsync command.

Table 10. Vsync Commands Description

Command Name	SCLK Rising Edges While LAT is High	Description
Vsync (Vertical Synchronization)	3	Vertical Synchronization signal. When this command is received, BANK_SEL bit will be toggled, and all counters will be reset to 0. New frame images will be displayed in coming frame period. Refer to Figure 9 for a timing diagram of this command operation.

All the internal counters are initiated once the Vsync command is received. Figure 9 shows the timing of Vsync command.

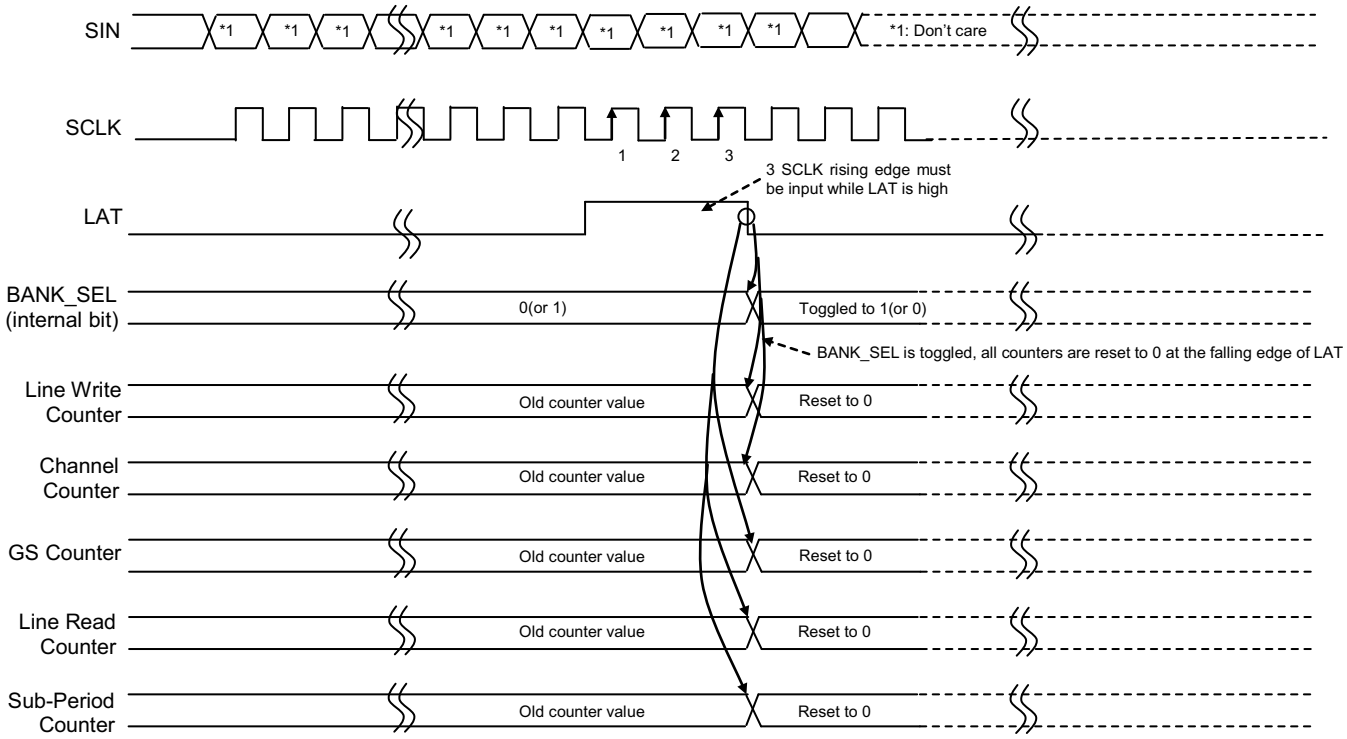


Figure 9. Vertical Synchronization (Vsync) Command

3.4.3 Detail of the Memory BANK

Each BANK contains all the GS data of 32 scan lines. Each line is comprised of sixteen 48 bits-width memory units. Each unit contains the R/G/B grayscale(GS) data of one channel. For example, the memory unit for channel 0 contains 16-bit GS data for OUTR0, 16-bit GS data for OUTG0, and 16-bit GS data for OUTB0. Figure 10 shows the bit arrangement of this memory unit. In this example, bit 32–47 contains the 16-bit GS data for OUTB0 (Pin10 of IC) for line x.

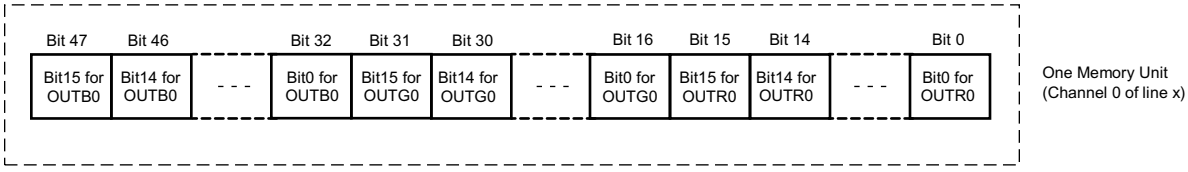


Figure 10. Bit Arrangement of One Memory Unit

Depending on the scan line number selected in the FC2 register (bit4–0), the total memory units to be written in one BANK is: 16 x scan_line_number. For example, if 32 multiplexing is chosen, then 512 (32 × 16 = 512) memory units should be written during one frame period. Figure 12 shows the memory structure detail.

3.4.4 Write GS Data to one Memory Unit (48 Bits-Width) With WRTGS Command

If TLC5958 detected one SCLK rising edge during LAT high period, it considers this as WRTGS command, and will latch the data of common shift register into one memory unit (48-bits width) at the falling edge of LAT.

The data of common shift register is latched into memory unit according to Figure 11 bit sequence. When GS data is shifted into the common shift register, bit 15 of OUTBn (Blue color) should be input first.

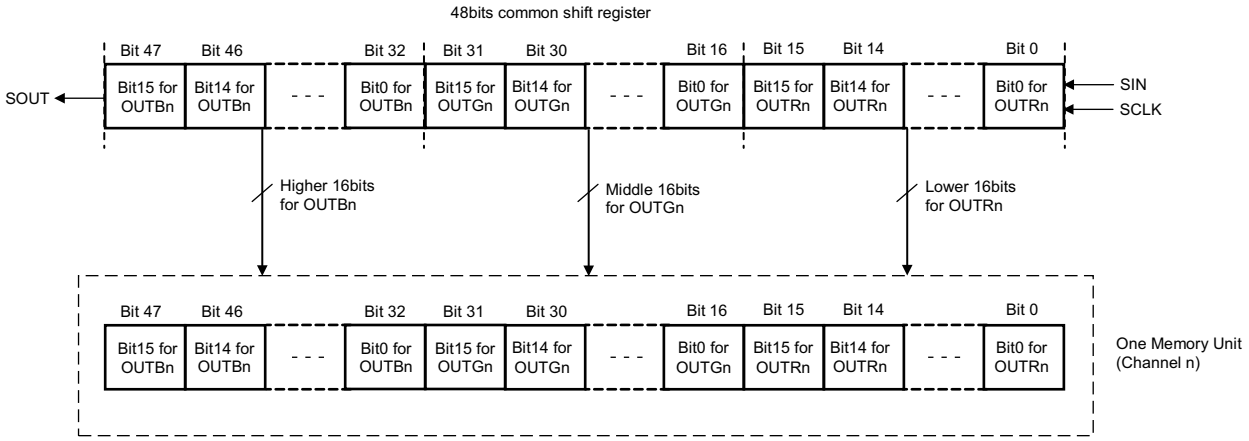


Figure 11. Latch Common Shift Register Data into One Memory Unit

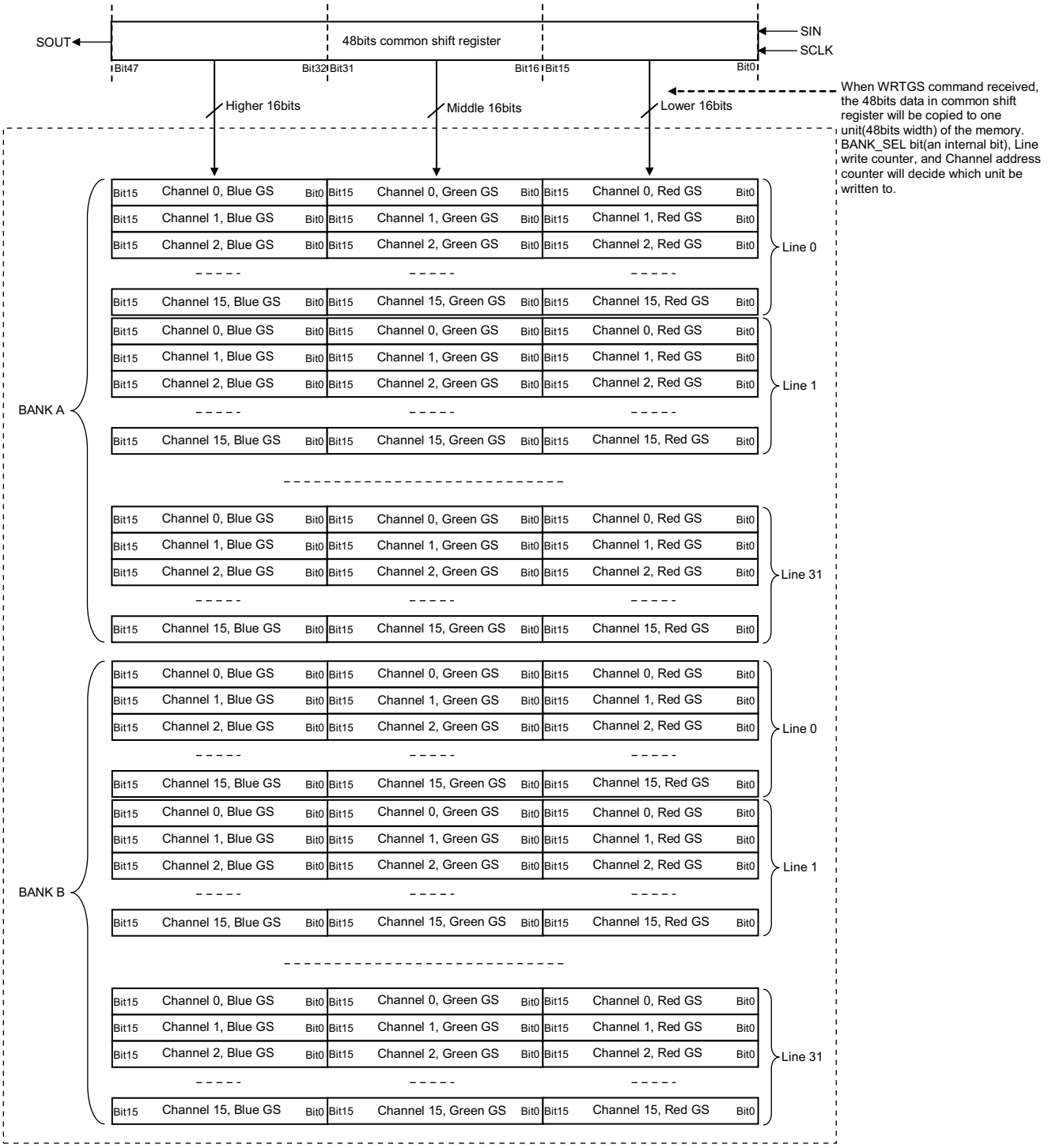


Figure 12. Memory Structure

BANK_SEL bit(an internal bit), Line write address counter, and channel address counter will decide which unit to be written.

Figure 13 shows the timing of this command.

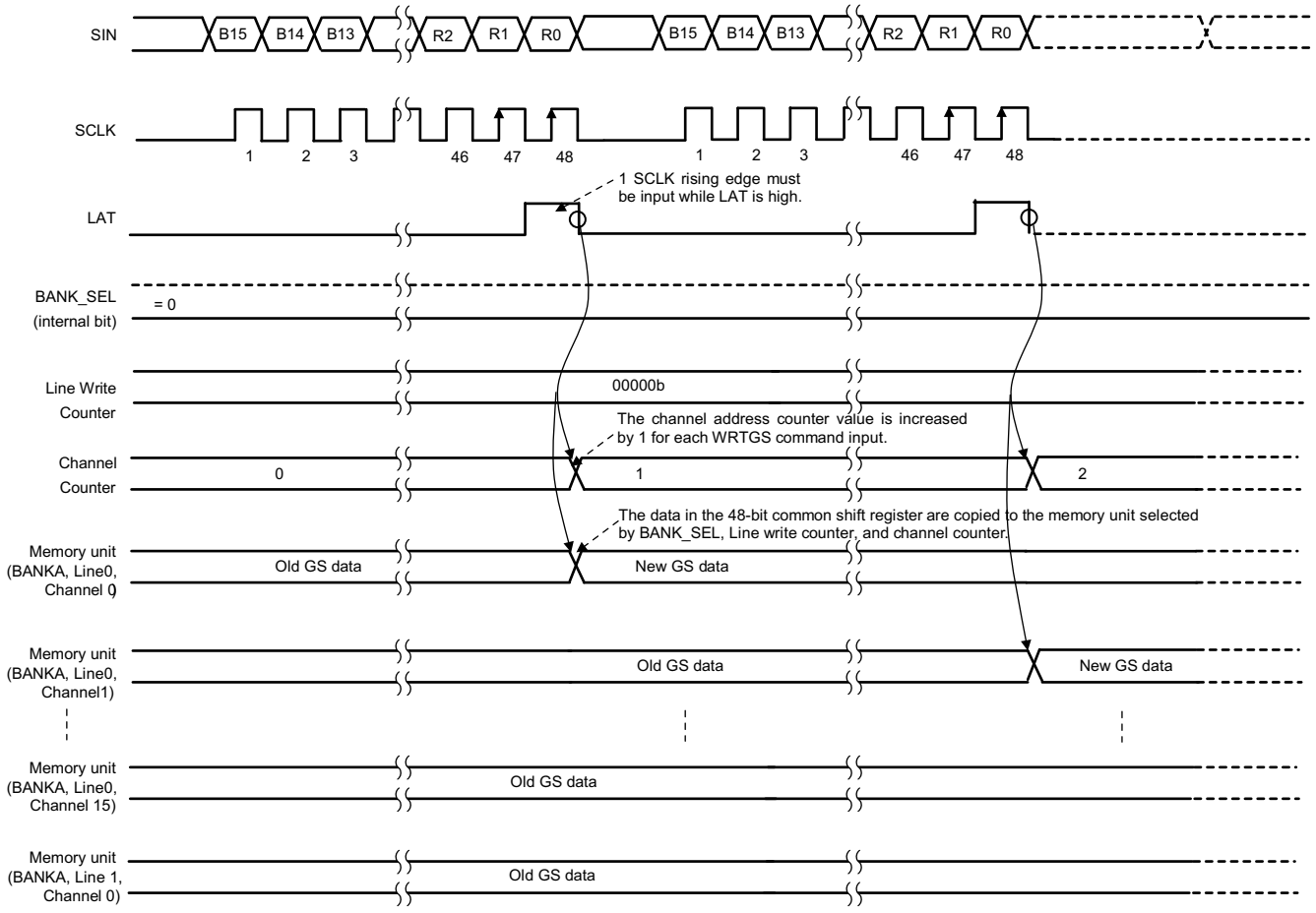


Figure 13. 48-Bit GS Data Write (WRTGS) Command

3.4.5 Write GS Data to one Memory BANK

One BANK contains maximum memory units (48 bits-width) number is: 32 lines x 16 channels = 512.

Depending on the multiplexing ratio selected in the FC2 register (bit4–0), the total memory units needed to be written in one BANK is: 16 x scan_line_number. Users should write to these memory units one by one sequentially. A detailed description follows:

After power on, BANK_SEL bit, line write counter, and channel counter are reset to 0. Thus, the memory unit of BANK A, Line 0, Channel 0 are selected to be written with the 48-bits GS data in common shift register when WRTGS command received.

After that, the channel counter increments (+1), then the memory unit of BANK A, Line 0, and channel 1 will be copied with the 48-bit data in common shift register when next WRTGS command input.

In this sequence, when all sixteen channel's memory unit of line 0 have been written, the channel counter will be higher than 15. At this moment, the channel counter will be reset to 0, and line counter will +1.

Next, the sixteen channel's memory unit of line 1 is written one by one in same method. When line1 is finished, line counter increments (+1), and the sixteen channels of line 2 are written.

In this manner, when the line counter is higher than MAX_LINE (see Table 9), it means all scan lines had been updated with new GS data, then the line counter is reset to 0.

See Figure 14 for this timing diagram.

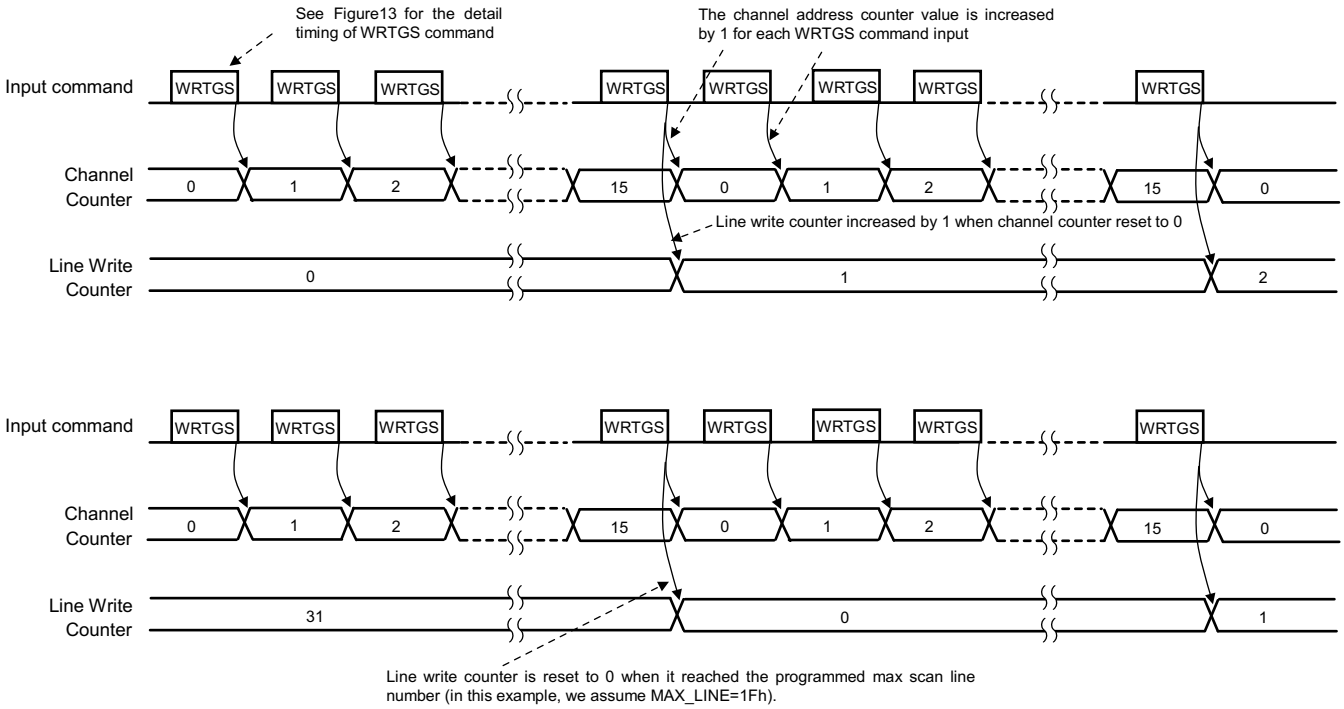


Figure 14. Memory Write Sequence

3.5 Step 4 — Send Vsync Command to Switch the BANK Purpose

Send Vsync command, then the BANK to which the GS data had been written in previous step will be displayed in the coming frame period. See Figure 9 to learn how to send Vsync command.

3.6 Step 5 — Input GCLK to Begin Display the Image of one new Frame

Input GCLK continuously, 257GCLK (or 513GCLK) as a segment. Between the interval of two segments, LED supply voltage should be switched from one line to next line accordingly. Since TLC5958 needs some time to prepare GS data for the 1st line of a new frame, after sending Vsync command (falling edge of LAT pulse), some wait time (2.5µS) is needed before sending the 1st GCLK .

3.6.1 Basic Knowledge: What's PWM CONTROL?

PWM Control means pulse width modulation (PWM) control scheme, which control the OUTx pin turn on ratio during one display period proportional to the GrayScale (GS) data of this channel. The use of 16-bits GS data per channel results in 65536 brightness steps, from 0% up to 100% brightness.

For example:

- If GS = 0, then OUTx will not turn on during one display period (65536 GCLK period totally), the brightness is 0%
- If GS = 500, then during one display period, OUTx will turn on 500 GCLK period, then the brightness ratio will be 500/65535 = 0.763% (Assume 100% brightness if 65535 GCLK period is turn on during one display period)
- If GS = 65534, then during one display period, OUTx will turn on 65534 GCLK period, then the brightness ratio will be 65534/65535 = 99.9985%

3.6.2 Multiplexed Enhanced Spectrum (ES) PWM Control

TLC5958 is designed mainly for multiplexed display system. It uses an innovative Multiplexed ES PWM method to improve the visual refresh rate while maintain the best grayscale performance.

Two PWM modes can be selected: 8-bit MSB + 8-bit LSB (8+8) mode, and 9-bit MSB + 7-bit LSB (9+7) mode. This is decided by SEL_PWM (bit 14 of FC2 register).

3.6.2.1 8+8 mode ES PWM Control

When SEL_PWM (bit 14 of FC2 register) = 0, ES-PWM is in 8MSB + 8LSB mode.

In the conventional 8MSB + 8LSB ES-PWM control, one total display period (include 65536 GCLK period) is divided to 256 display segments. Each segment has 256 GCLK periods. The OUTx total on-time during one display period is distributed evenly in these 256 segments. By this mean, the visual refresh rate is increased by 256 times.

This is a good method for static display system, but not good for multiplexed (dynamic) display system. If one finished all the 256 segments of one scan line, then change to display another scan line, the refresh rate will be very low.

In TLC5958's multiplexed ES PWM control, one display period is divided into 256 sub-periods, which corresponding to the 256 segments of the conventional ES-PWM. During one sub-period, all scan lines will display their corresponding segment sequentially. When all scan lines finished their segment, this sub-period ends, and next sub-period will start. Because each scan line has a chance to display in one sub-period, thus the visual refresh rate is 256 time higher than that of the conventional ES-PWM control.

The time of one sub-period will determine the visual refresh rate, as Equation 3 shows:

$$f_{Refresh} = 1/t_{Sub\text{-}period} \quad (3)$$

Where:

$f_{Refresh}$ is the visual refresh rate
$t_{Sub\text{-}period}$ is the time of one sub-period needed.

Figure 15 shows the timing of multiplexed ES PWM operation in 8+8 mode.

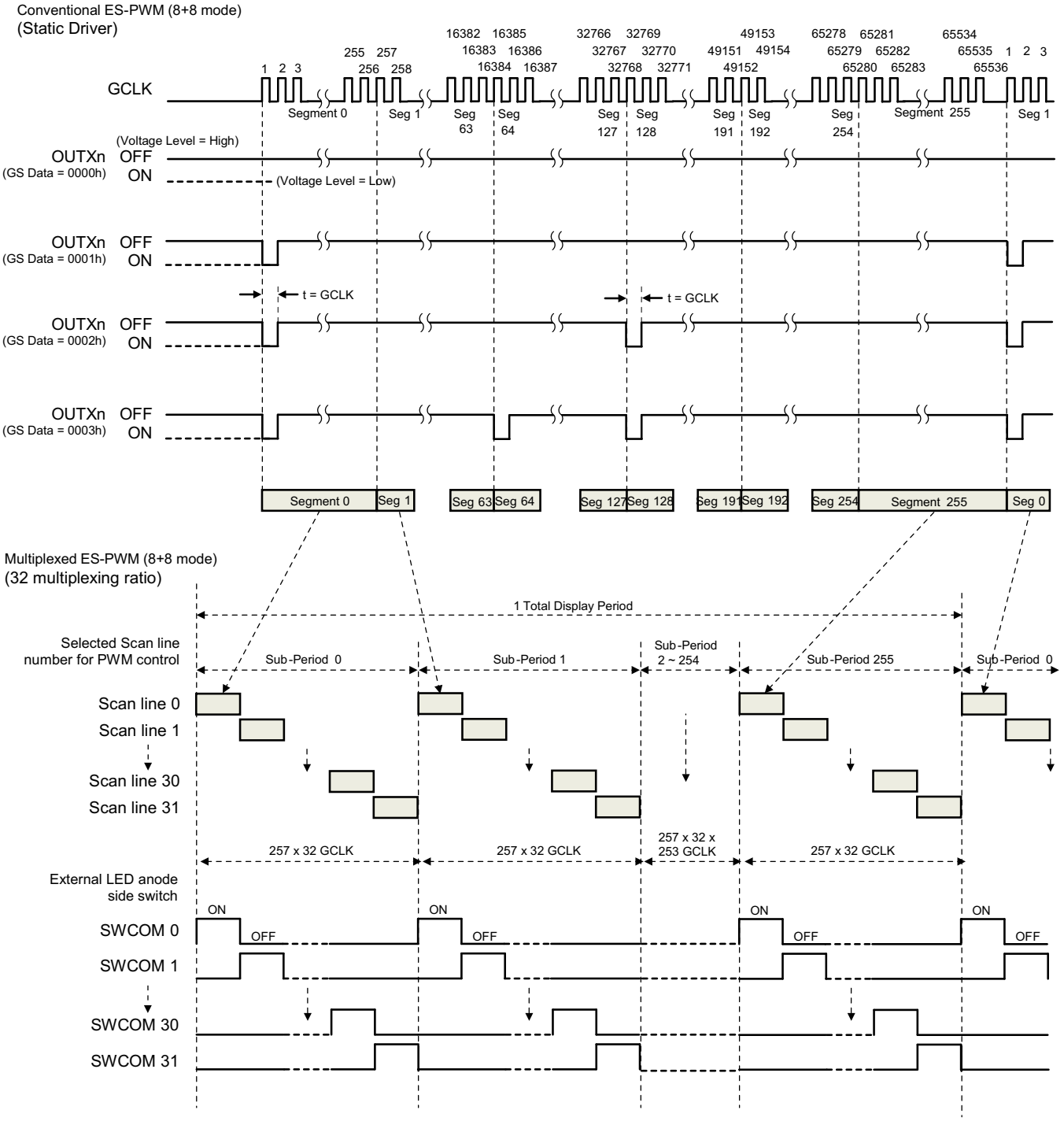


Figure 15. Multiplexed ES-PWM Operation (8+8 mode)

3.6.2.2 9+7 Mode ES PWM Control

When SEL_PWM (bit 14 of FC2 register) = 1, ES-PWM is in 9MSB + 7LSB mode.

In the conventional 9MSB +7LSB ES-PWM control, one total display period (include 65536 GCLK period) is divided to 128 display segments. Each segment has 512 GCLK periods. The OUTx total on-time during one display period is distributed evenly in these 128 segments. By this mean, the visual refresh rate is increased by 128 times.

This is a good method for static display system, but not good for multiplexed (dynamic) display system. If one finished all the 128 segments of one scan line, then change to display another scan line, the refresh rate will be very low.

In TLC5958's multiplexed ES PWM control, one display period is divided into 128 sub-periods, which corresponding to the 128 segments of the conventional ES-PWM. During one sub-period, all scan lines will display their corresponding segment sequentially. When all scan lines finished their segment, this sub-period ends, and next sub-period will start. Because each scan line has a chance to display in one sub-period, thus the visual refresh rate is 128 times higher than that of the conventional ES-PWM control.

Figure 17 shows the timing of multiplexed ES PWM operation in 9+7 mode.

3.6.3 How to input GCLK and Address of Lines for Multiplexing

3.6.3.1 Example: 8+8 Mode, Multiplexing Ratio 1/32

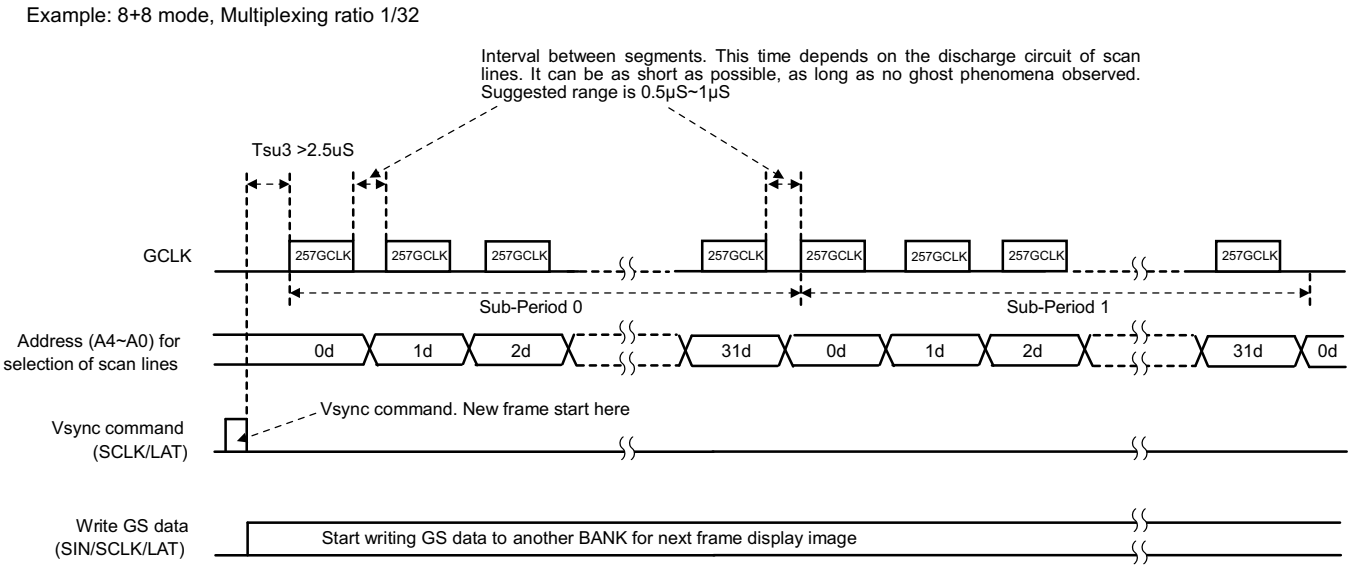


Figure 16. Controller Timing Sequence, 8+8 Mode, 32 Multiplexing

3.6.3.2 Example: 9+7 Mode

Same timing sequence as 8+8 mode, except 513GCLK per segment instead of 257GCLK per segment.

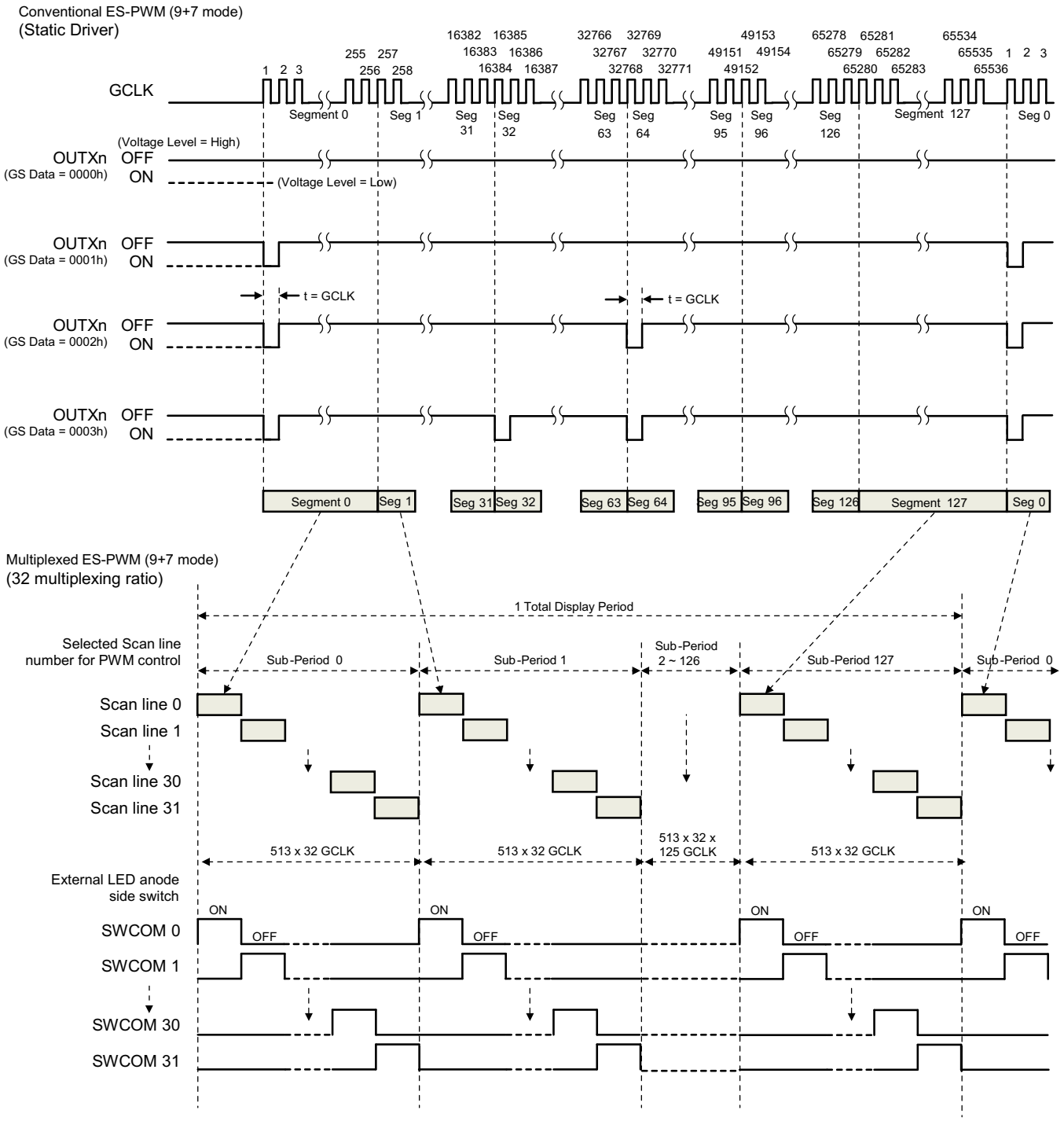


Figure 17. Multiplexed ES-PWM Operation (9+7 mode)

3.7 Finish the Last Two Steps to Operate TLC5958

3.7.1 Step 6 — During the same period of step5, GS data for next frame should be written into another BANK

See Figure 16 for detail.

3.7.2 Step 7 — When the time of one frame ends, Vsync command should be input to swap the purpose of the two BANKs

Example: A big picture of the timing sequence, 9+7 mode

Example: A big picture of the timing sequence, 9+7 mode

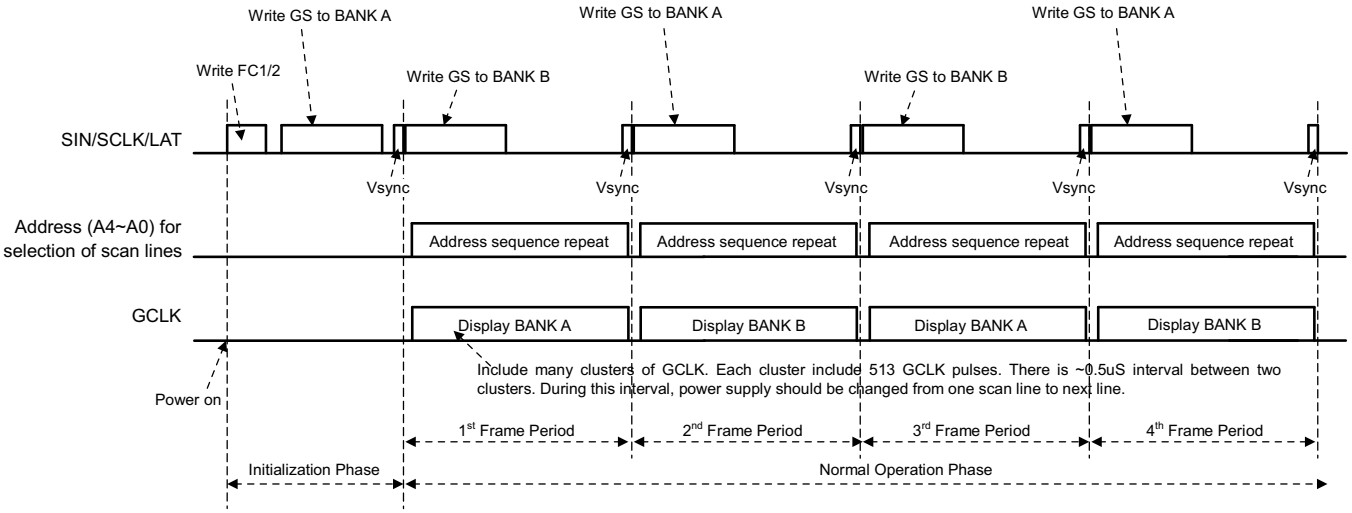


Figure 18. Timing Sequence, 9+7 mode

3.8 Led Open Detection (LOD)

3.8.1 How does LOD Operate?

LOD function detect a fault caused by an open circuit in any LED string, or a short from OUTXn to ground with low impedance, by comparing the OUTX*n* voltage to the LOD detection threshold voltage level set by LODVLT in the FC1 register (see Table 5). If the OUTX*n* voltage is lower than the programmed voltage, the corresponding output LOD bit will be set to '1' to indicate a opened LED. Otherwise, the output of that LOD bit is '0' (see Figure 19). LOD data output by detect circuit are valid only during the ‘on’ period of that OUTX*n* output channel. LOD data are always ‘0’ for outputs that are turned off.

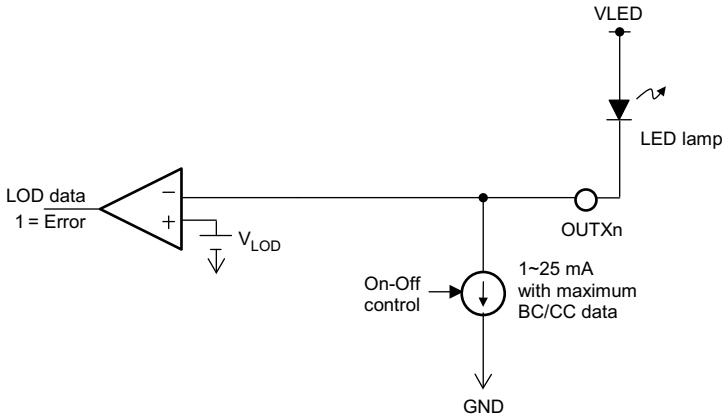


Figure 19. LOD Detect Circuit of One Channel

The output of LOD detect circuit are loaded into the 48-bit register called SID holder (Figure 20 shows the bit arrangement of this SID holder) at the rising edge of the thirty-third GCLK in each segment. To get a correct detecting result, it’s necessary to make sure OUTXn kept ‘on’ in the thirty-third GCLK period in one segment. See Figure 21 for the timing diagram.

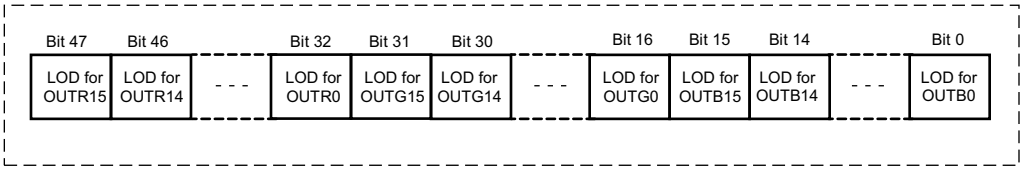


Figure 20. Bit Arrangement of SID Holder

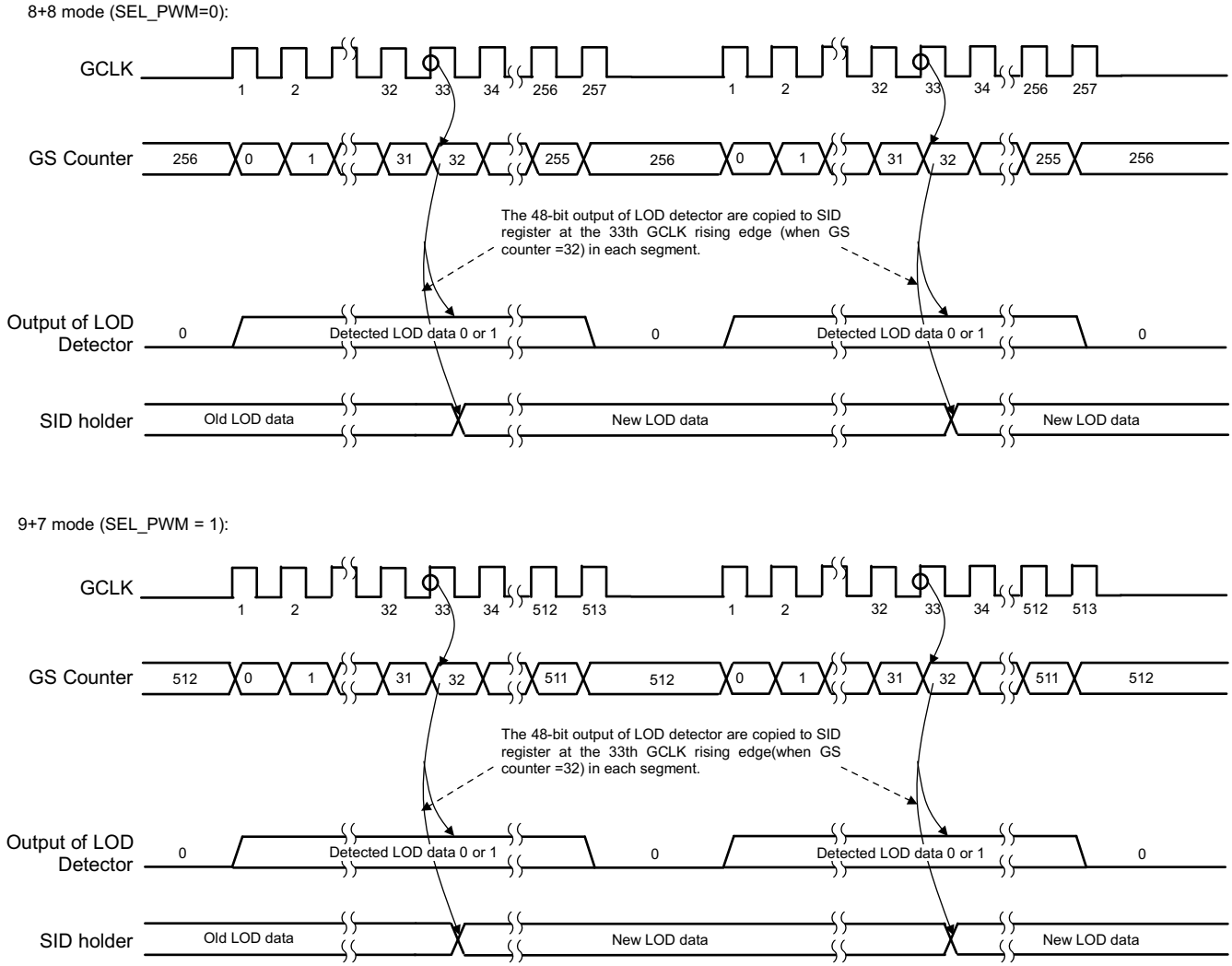


Figure 21. LOD Information Latch Into SID Holder

3.8.2 Read LOD Information With READSID Command

Once TLC5958 detected 7 rising edges of SCLK during LAT high period, it consider this as a READSID command. The 48bit data in SID holder will be latched into common shift register at the falling edge of LAT signal. After that, 48 SCLK pulse should be input to shift out the LOD data at the SOUT pin. Figure 22 shows this timing diagram.

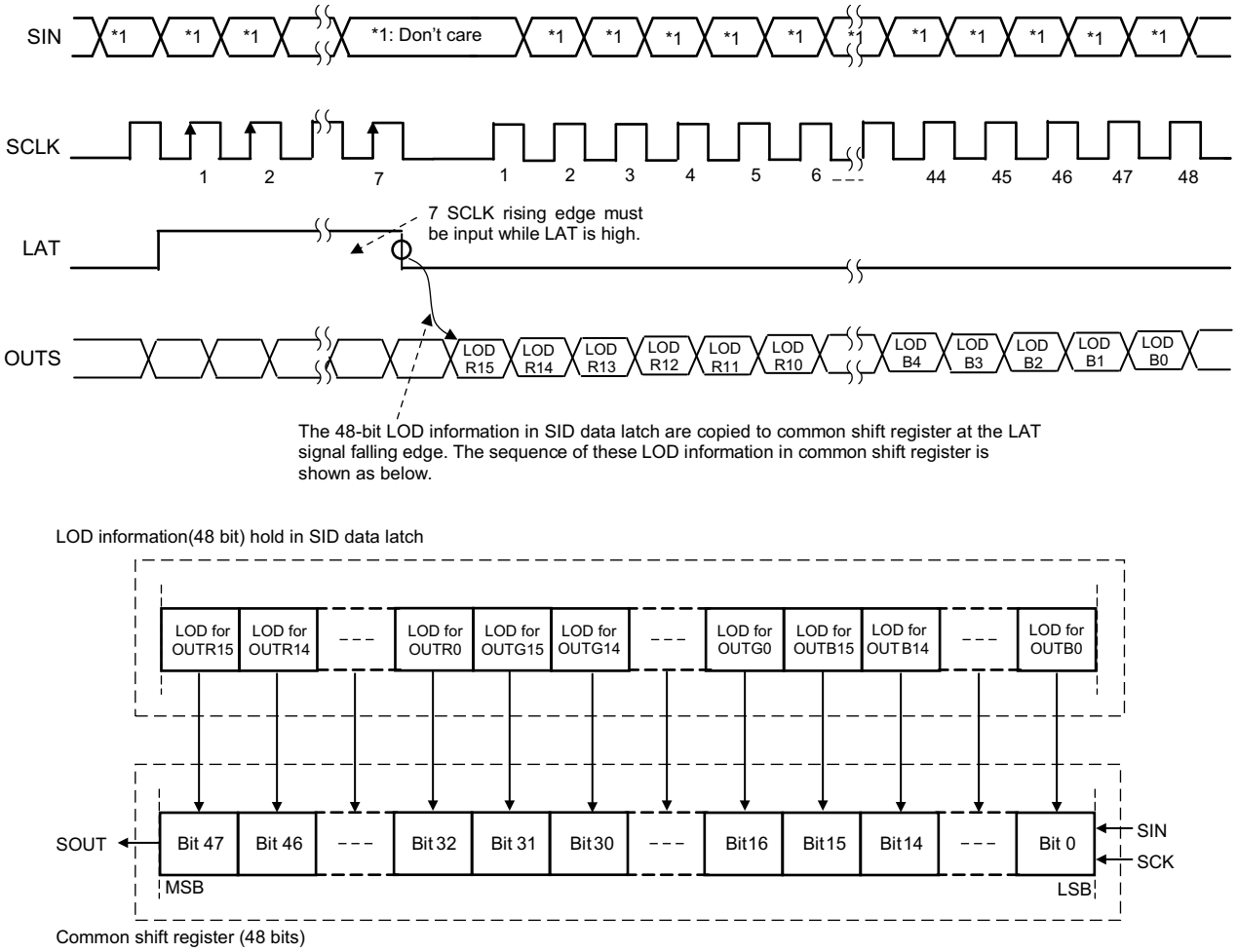


Figure 22. LOD Information Read (READSID) Timing

3.8.3 Suggested LED Open Detection Process

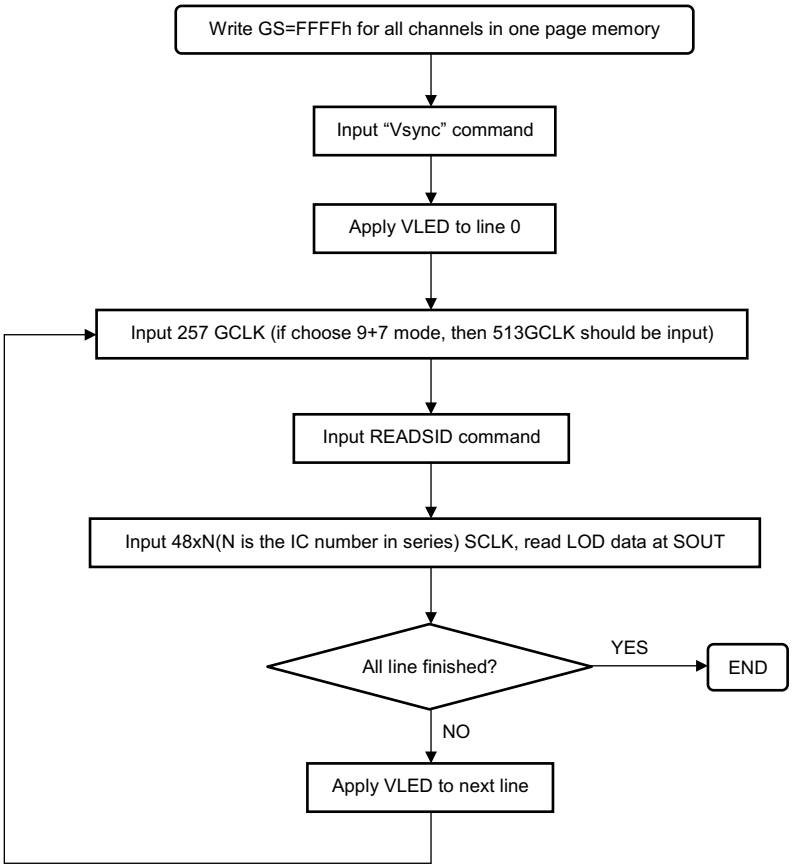


Figure 23. Example of LOD Detection Process (8+8 mode)

3.9 How to Read Function Control Register

Once TLC5958 detected 10 rising edges of SCLK during LAT high period, it consider this as a READFC1 command. The 44 bit data in FC1 register will be latched into the lower 44bit of common shift register at the falling edge of LAT signal. Other bits in the common shift register will be reset to 0.

Once TLC5958 detected 11 rising edges of SCLK during LAT high period, it consider this as a READFC2 command. The 17 bit data in FC2 register will be latched into the lower 17 bit of common shift register at the falling edge of LAT signal. Other bits in the common shift register will be reset to 0.

Then the loaded data can be read out from SOUT synchronized with the SCLK rising edge.

Refer to Figure 24 and Figure 25 for the timing diagram of these two commands.

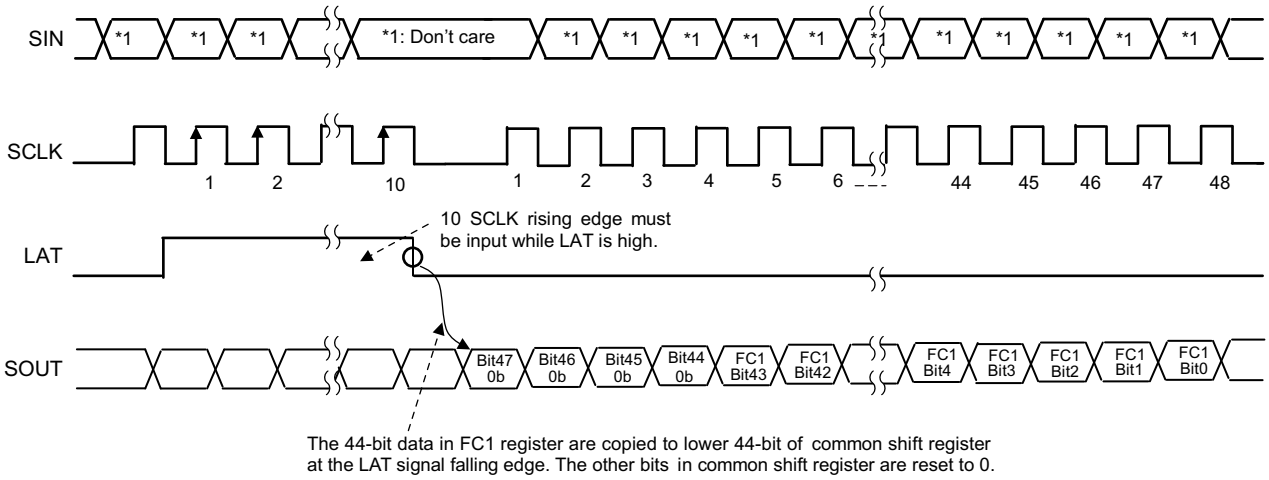


Figure 24. FC1 Data Read (READFC1) Command

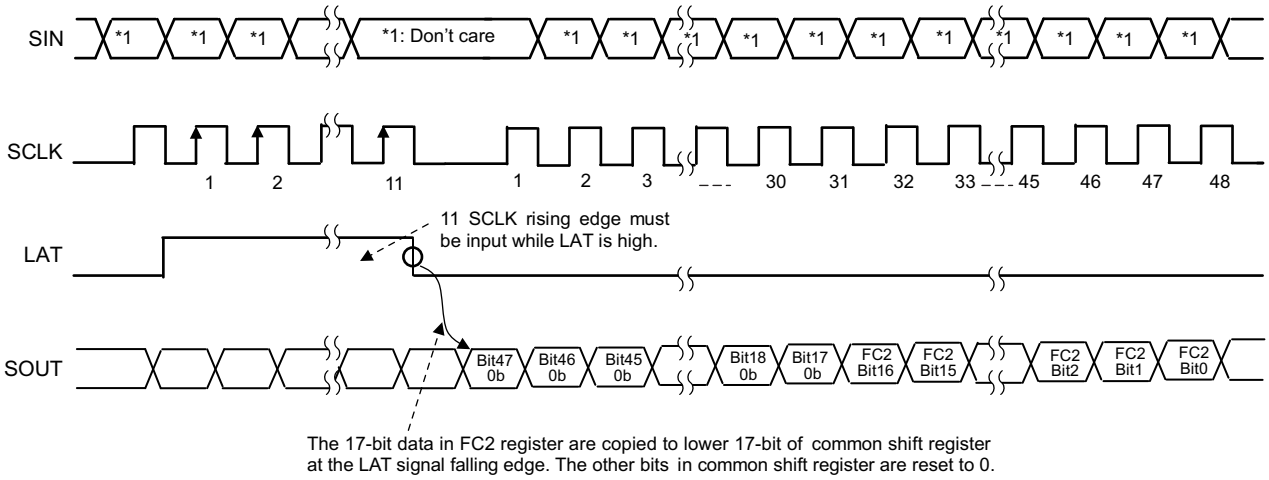


Figure 25. FC2 Data Read (READFC2) Command

3.10 Function Commands Summary

In Table 11 is a summary of all the seven commands that can be input with SCLK and LAT signals: WRTGS, VSYNC, WRTFC, READSID, READFC1, READFC2, and FCWRTEN.

Table 11. Function Commands Summary

Command Name	SCLK Rising Edges While LAT is High	Description
WRTGS (48-bit GS data write)	1	The 48-bit data in common shift register are copied to the memory unit selected by Channel address counter, Line write counter, and BANK_SEL bit. Refer to Figure 13 for a timing diagram of this command operation.
Vsync (Vertical Synchronization)	3	Vertical Synchronization signal. When receive this command, BANK_SEL bit will be toggled, and all counters will be reset to 0. New frame image will be displayed in coming frame period. Refer to Figure 9 for a timing diagram of this command operation.

Table 11. Function Commands Summary (continued)

Command Name	SCLK Rising Edges While LAT is High	Description
WRTFC (FC data write)	5	The lower 44-bit data or the lower 17-bit data in common shift register are copied to the FC1 or FC2 register. Bit47–44 of the common shift register will be used to choose which FC register be written to. If '1001b' received for bit47–44 of common shift register, then the lower 44-bit in common shift register will be copied to FC1 register. If '0110b' received for bit47–44 of common shift register, then the lower 17-bit in common shift register will be copied to FC2 register. Refer to Figure 7 for a timing diagram of this command operation.
READSID (SID data read)	7	The 48-bit LOD data in the SID data latch are copied to the 48-bit shift register. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 22 for a timing diagram of this command operation.
READFC1 (FC1 data read)	10	The 44-bit data in the FC1 register are copied to the lower 44-bit of shift register. Other bits in the shift register will be reset to 0. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 24 for a timing diagram of this command operation.
READFC2 (FC2 data read)	11	The 17-bit data in the FC2 register are copied to the lower 17-bit of shift register. Other bits in the shift register will be reset to 0. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 25 for a timing diagram of this command operation.
FCWRTEN (FC write enable)	15	FC writes are enabled by this command. This command must always be input before the FC data write occurs. Refer to Figure 7 for a timing diagram of this command operation.

3.11 Power-Save Mode (PSM)

The power-save mode (PSM) is enabled by setting PSAVE_ENA (bit5 of FC2 register) to '1'. When power on, this bit default is '0'.

When this function is enabled, if all the GS data received for next frame are '0', IC will enter power-save mode at the moment Vsync command input.

In power-save mode, IC will detect if non-zero GS data is input for next frame. Among all the GS data for next frame, if anyone is non-zero, it will start to resume normal mode once finish the whole GS input for next frame.

See Figure 26 for the timing diagram.

In power-save mode, all analog circuits like constant current output, LOD circuit, and so forth, do not work, the device total current consumption Icc is below 1 mA.

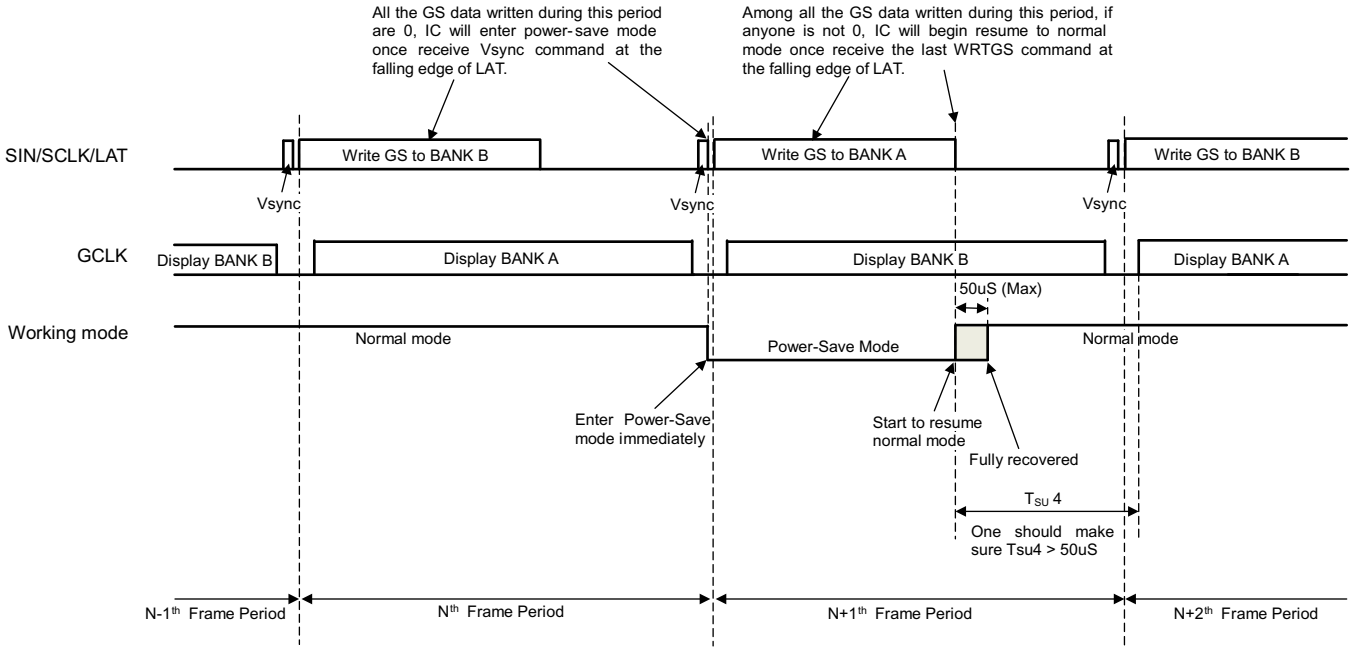


Figure 26. Enter/Exit Power-Save Mode

3.12 Ghost Removal

The internal pre-charge FET is implemented to remove ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current for parasitic capacitance of OUTXn through the LED when the supply voltage switches from one common line to next common line.

To prevent this unwanted charging current, TLC5958 uses an internal FET to pull OUTXn up to VCC-1.4 V, during the common line switching period. Thus, no charging current is flowing through the LED anymore and the ghosting is eliminated.

Two working modes of pre-charge can be selected with SEL_PCHG, bit 7 of FC2.

When this bit is ‘0’, which is the default setting, the pre-charge FET only remains off during the period in which the channel is on.

When this bit is ‘1’, the pre-charge FET remains off during the whole segment period (257 GCLK period), and only keep on during the dead-time (the time between two adjacent segments).

Figure 27 shows this difference (take 8+8 mode as example).

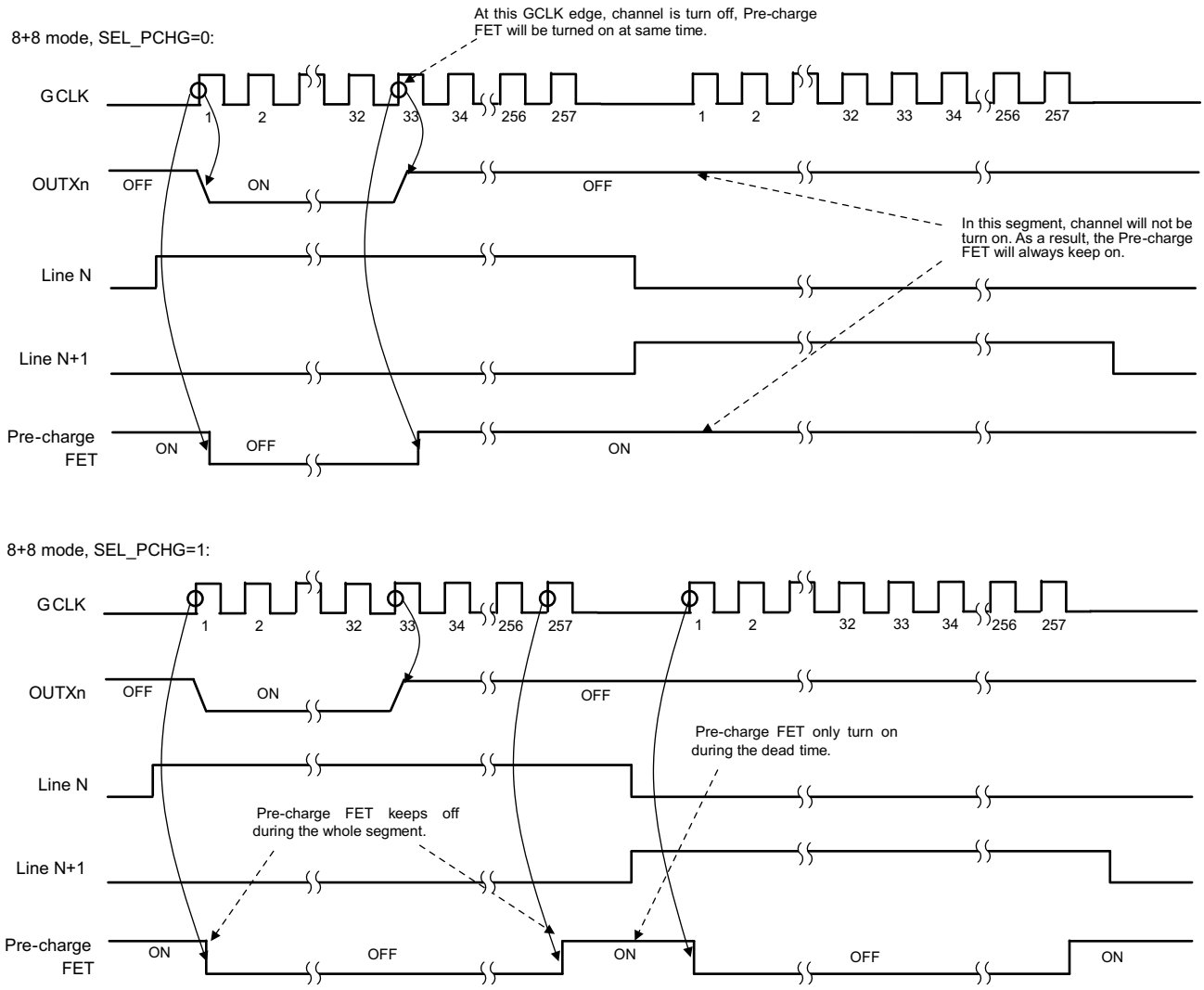


Figure 27. Pre-charge FET Working Mode

3.13 Protection

3.13.1 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs of the IC when the junction temperature (T_J) exceeds the 170°C (typ). It resume normal work once T_J lower than 160°C(typ).

3.13.2 IREF Resistor Short Protection (ISP)

The Iref resistor short protection (ISP) function prevent the unwanted large current from flowing though the constant-current output when Iref resistor is shorted accidently. TLC5958 will turn off all output channels when Iref pin voltage lower than 0.125 V(typ). When Iref pin voltage higher than 0.35 V(typ), the TLC5958 will resume normal work again.

3.14 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 48 LED channels turned on simultaneously at the 1st GCLK rising edge. This large surge current could induce detrimental noise and electromagnetic interference (EMI) into other circuits.

The TLC5958 separate the LED channels into 12 groups. Each group include 4 output channels. It turns on these groups sequentially with a 1.67 ns (typ) delay between one group and the next group. By this means, a soft-start feature is provided. See Table 7 for the detail turn on delay sequence.

The turn-off of LED channels is implemented with a same delay scheme.

This group delay function is enabled by default at power on. However, it can be disabled by setting SEL_GDLY (bit4 of FC1 register) to '0'.

3.15 Low Gray Scale Enhancement (LGSETM)

First (1st) line issue is a common phenomena in multiplexing application, especially in high density, high refresh rate panel. This issue can be solved by choosing different setting of LGSE1-R, LGSE1-G, LGSE1-B in FC1 register. Adjust these control bits will also help improve the white balance at low grayscale condition.

Table 12. LGSE1-R/G/B Effect Summary

LGSE1-R (FC1)		Low Grayscale Enhancement Effect
Bit12	Bit11	
0	0	No
0	1	Weak
1	0	Medium
1	1	Strong
LGSE1-G(FC1)		Low Grayscale Enhancement Effect
Bit9	Bit8	
0	0	No
0	1	Weak
1	0	Medium
1	1	Strong
LGSE1-B(FC1)		Low Grayscale Enhancement Effect
Bit6	Bit5	
0	0	No
0	1	Weak
1	0	Medium
1	1	Strong

Different multiplexing ratio needs different setting:

1. The higher multiplexing ratio is, the higher enhancement needed.
2. The enhancement of G/B should be higher than that of Red color.

For example, one suggested setting for a 1/32 multiplexing panel is:
LGSE1-R = 01b, LGSE1-G = LGSE1-B = 11b

Besides the above counter measures, choose setting of LGSE2, bit15-16 of FC2 register, will also help improve the 1st line issue at low gray scale condition.

Table 13. LGSE2 Effect Summary

LGSE2(FC2)		Low Grayscale Enhancement Effect
Bit16	Bit15	
0	0	No
0	1	Weak
1	0	Medium
1	1	Strong

A third method to improve low grayscale performance is to set EMI_REDUCE_R(G/B), bit 11-13 of FC2. When set some of these bits to 1, the white balance and 1st line issue at low grayscale may be improved; While, keep these bits at 0 will be helpful for EMI performance. A trade-off need be made based on the test result of the specific application.

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