Tony Calabria

TI Precision Designs: Verified Design

Hardware Pace using Slope Detection

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Circuit Description

This hardware pace detection circuit is designed to monitor for occurrences of a pace maker signal in an electrocardiogram (ECG) application by providing an alert to a GPIO. The circuit combines three individual circuits: a differentiator circuit used for slope detection, a window comparator to monitor for an event and SR latch to indicate an event has occurred. A pacemaker signal at the input will latch a digital I/O pin high to indicate the signal is present in the waveform.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
ADS1298	Product Folder
OPA348	Product Folder
TLV3401	Product Folder
SN74LVC2G00DCTR	Product Folder

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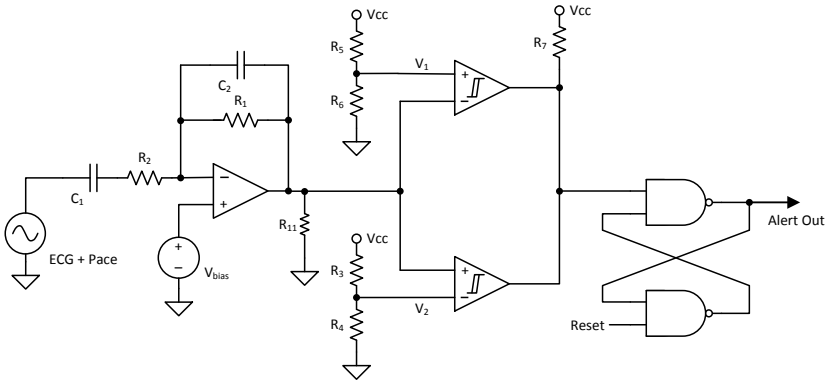

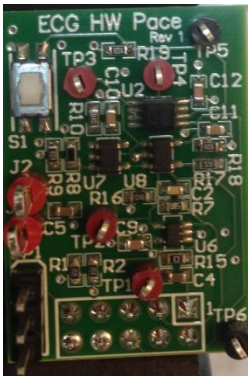

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5V dc
- Minimum pace signal width: 100µs
- Minimum pace signal amplitude: 2mV
- Monitor for slope of pacemaker signal while ignoring ECG signal
- Set GPIO to indicate pacemaker signal is present

The design functionality is displayed below showing a pulse when the slope of the pace maker signal is present. The Differentiator Out signal triggers a falling edge on the window comparator thereby setting the SR latch.

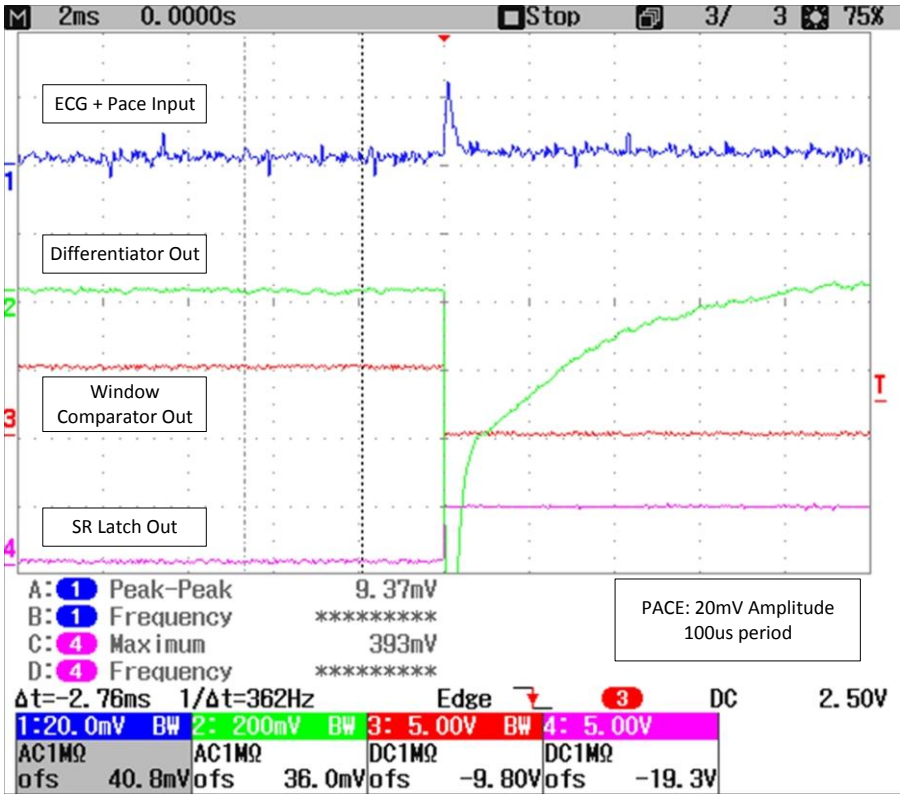

Figure 1: Hardware Pace Results

2 Theory of Operation

To understand the design approach discussed in this TI Design note, basic pacemaker functionality must first be discussed. The primary role of the pacemaker is to apply a small surge of voltage to the heart, prior to the QRS pulse, to assist with blood flow through the body. The signal can take on a variety of form factors which can be broken down to a specific amplitude and signal width. Figure 2 is used to model a typical QRS pulse with an example of a Ventricle pacemaker signal shown prior.

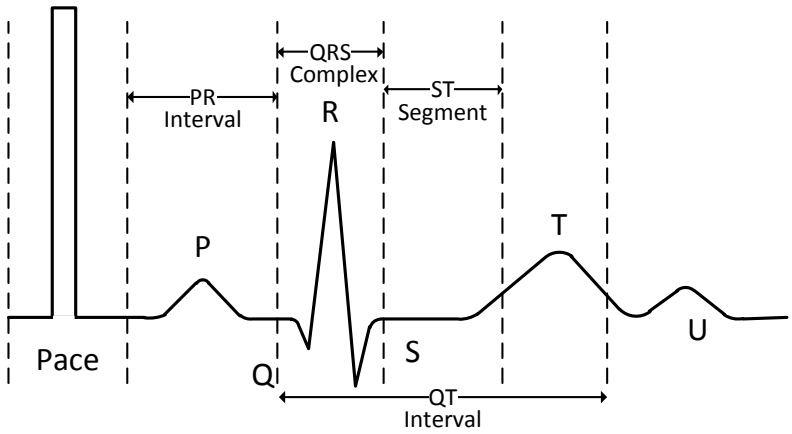

Figure 2: ECG Signal with Pace

The height and width of the pacemaker signal can range anywhere from 2mV to over 500mV in amplitude and 0.1ms to 500ms in width while possibly sharing similar signal characteristics of the ECG pulse. The shape of the signal will differ depending on how the pacemaker is positioned to assist the heart and the type of pacemaker installed. A common characteristic of pacing pulses is to have a very steep rising edge transition which can be used to distinguish from the QRS complex. Using the higher frequency components associated with this steep rising edge can determine if a pacemaker is present. Taking a Fast Fourier Transfer (FFT) of an ECG signal with a pacemaker, the characteristics show that the ECG components lie within the 150Hz and lower range while the pace signal resides in the higher bandwidths, at times 1kHz and greater.

Determining if the pace signal is present in an ECG system can be done in a variety of ways. Wide bandwidth ADCs are commonly used to digitize the ECG signal, where post processing can determine if a pace signal appears before the QT interval shown in Figure 2. There are also hardware methods which can be used focused around analog design to determine if the pacemaker signal is present.

This TI Design is a hardware pace detection method designed around using slope detection. A complete schematic for this design is shown in Figure 3. The circuit is designed to be specifically used with the ADS1298 which includes an internal differential to single ended converter for the ECG lead. Once routed from the ADC, a differentiator circuit is used for slope detection of the pacemaker signal. A reference voltage, V_{bias}, is used to add DC bias to the window comparator circuit to allow the circuit to be powered off of a single supply. Resistors set the threshold values for the window comparator prior to the latch stage to indicate an event. The design can be segmented into three stages: Slope Detection, Alert Stage, and Latch to GPIO.

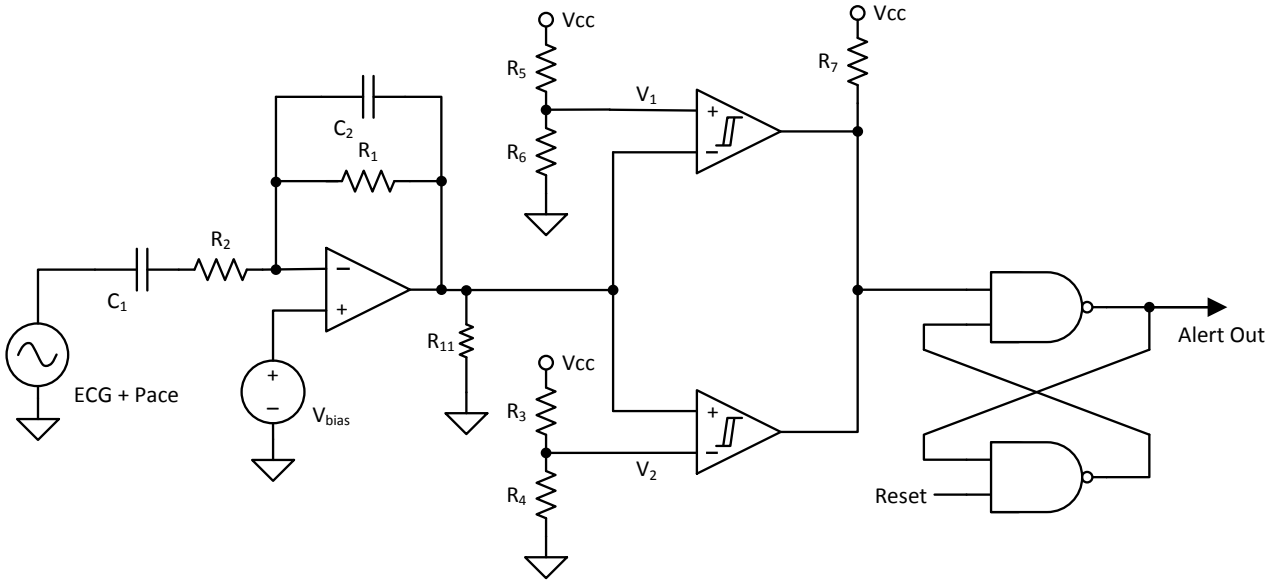

Figure 3: Complete Circuit Schematic

2.1 Slope Detection

The first stage monitors for the leading edge of the pace signal while attenuating the QRS complex. A differentiator circuit is selected to monitor for the steep leading edge of the pacemaker signal. This circuit takes advantage of the characteristic of current across a capacitor and uses the op amp feedback resistor to develop a proportional voltage. The output from the circuit will reflect a signal relative to the slope, dV/dt, of the input, shown in Figure 4.

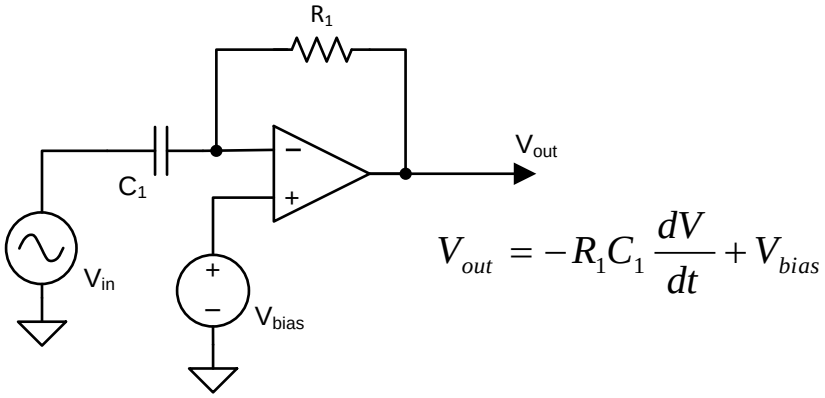

Figure 4: Typical Differentiator Circuit

The resistor and capacitor used in this circuit form a high pass filter which is set to monitor for the higher frequency components from the pacemaker signal. Thus, the output will be proportional to the slope amplitude and duration while ignoring the QT interval and being offset by the V_{bias} voltage.

2.1.1 Circuit Compensation

The passive components will set the poles and zeroes for the transfer function and must be selected to ensure stability. A second capacitor, C_2, may be placed in parallel with the resistor in the feedback loop to help stabilize the circuit, along with a second resistor, R_2, in the input path. The procedure for selecting the stability network is beyond the scope of this design note; please see reference [1] for a detailed explanation of stability.

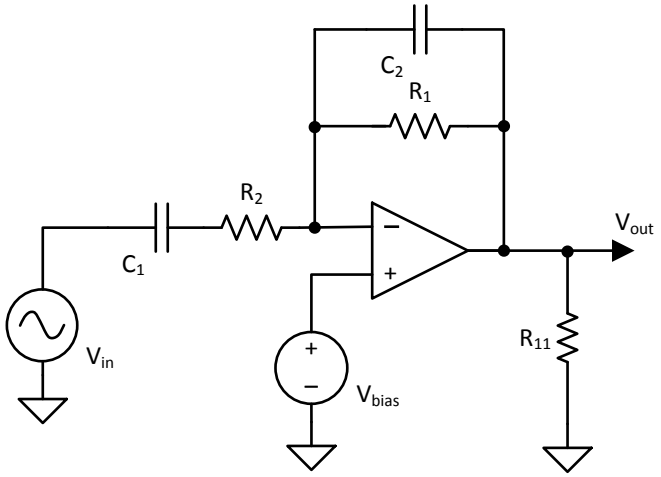

Figure 5: Differentiator Circuit with Compensation

In order to ensure 40dB gain before compensating for stability, the first order high pass filter for the circuit must begin at around 1Hz. C_1 is chosen to be 1µF to set the HPF cut off of the differentiator circuit to attenuate the unwanted QRS complex. Setting R_1 to 392kΩ and C_2 to 10nF help maximize the gain while keeping the circuit stable. R_2 is short circuited to 0Ω but included for design flexibility. R_{11} is in place as a 1MΩ load resistor for the output. The V_{bias} voltage is set to 2.5V, the midpoint of the power supplies, to allow the differentiator output maximum swing in either the positive or negative direction allowing design flexibility if the pace maker pulse is of opposite polarity. The V_{bias} voltage is generated by dividing the 5V supply using two 2MΩ resistors to help conserve power. As mentioned in the modifications section later, a second order high pass filter would help improve gain before compensating for stability.

2.2 Alert Stage

The output of the differentiator circuit, discussed above, will produce a pulse when a pace event occurs which must then be recognized to register an alert. By design, this pulse from the output of the differentiator can range anywhere from a few hundred mVs to a couple volts depending on the pacemaker signal characteristics. Capturing the signal is done using a window comparator circuit designed to output a logic low signal when the comparator input pulse exceeds either a high or low threshold voltage. The open drain output window comparator circuit used in the design is shown in Figure 6.

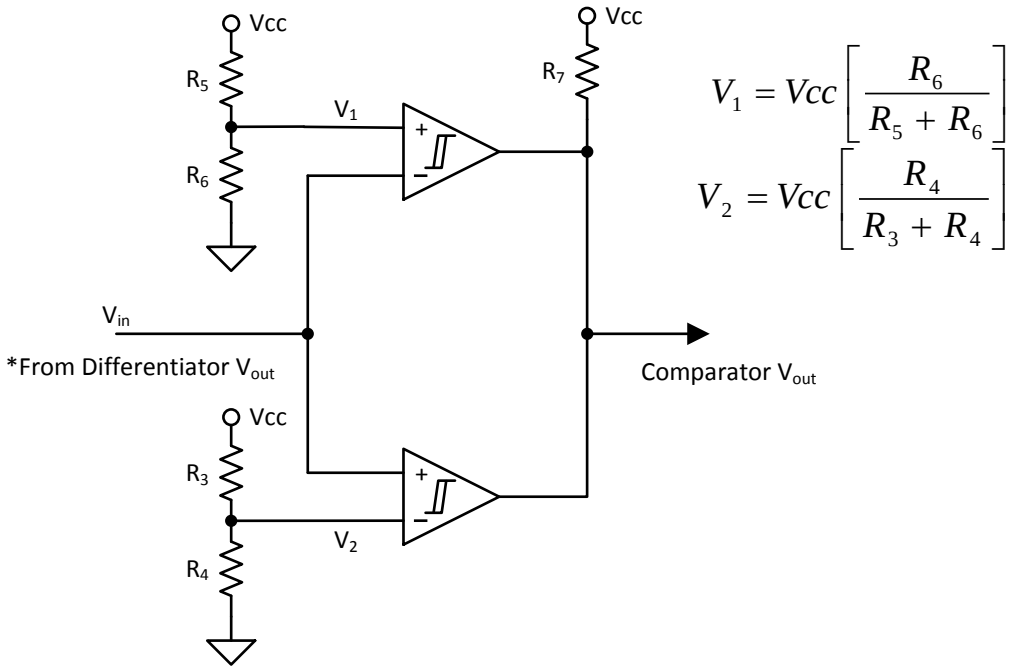

Figure 6: Window Comparator Circuit

The threshold limits, listed as V_1 and V_2 in Figure 6, are set as a fraction of the power supply determined by the R_3, R_4, R_5, R_6 resistor values. When the output from the differentiator circuit, listed as V_{in}, exceeds the set limits V_1 or V_2, the comparator output will trigger by pulling the comparator V_{out} line low.

Selection of component values is not as straightforward as it is for the differentiator circuit. The boundary limits for the window comparator are dependent on the amplitude of the differentiator amplifier output under the worst case condition, 2mV amplitude and 100µs width pacemaker pulse. Through simulation (shown later) we can estimate a value for the differentiator output amplitude to set the threshold limits of the window comparator, and then make modifications in the verification process. The values chosen are setting V_1 to 2.77V and V_2 to 2.48V, requiring R_3 set to 10.2kΩ, R_4 set to 10kΩ, R_5 set to 8.06kΩ, and R_6 set to 10kΩ. R_7 is a weak pull up resistor for the open drain output and will be set to 10kΩ. V_{cc} is the 5V supply used to power the system.

2.3 Latch to GPIO

The width of the comparator output pulse is determined by the time that V_{in} (from Figure 6) exceeds the window comparator boundaries. This duration can be as small as a few milliseconds and may be missed if not latched. Placing a SR-latch circuit after the window comparator will latch the signal in a steady state to be read back by a microcontroller or DSP until a reset is performed. The SR latch will perform two functions: latching the window comparator out signal, and serving as an inverter to create an active high alert out signal. The design of the SR-latch using two NAND gates is shown in Figure 7.

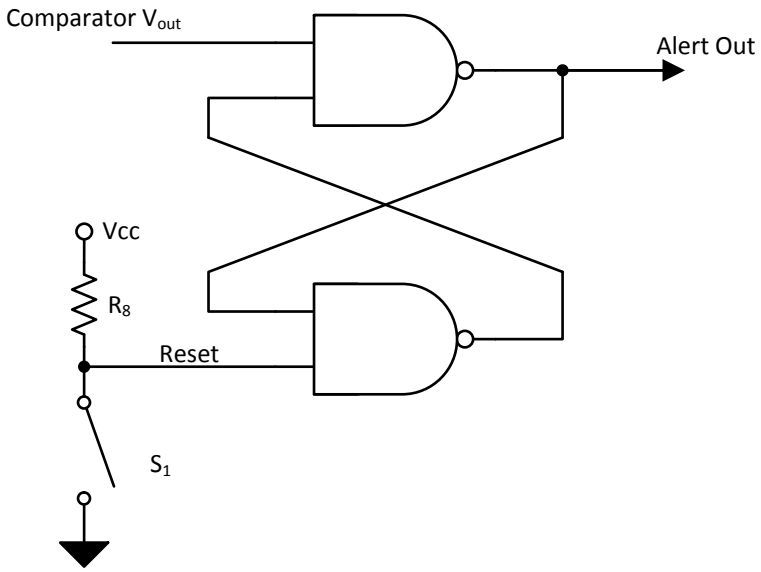

Figure 7: SR Latch

The alert out signal can be routed to a GPIO and the state monitored for a pace event. The R_8 resistor and S_1 switch are used to reset the latch. R_8 is a weak pull up resistor and will be set to 10kΩ, and S_1 is a single pull, single throw (SPST) push button switch.

3 Component Selection

3.1 Differentiator Circuit Amplifier Selection

The slope detection circuit has a few requirements on the amplifier selection. The op amp must have adequate bandwidth to respond to the pace signal change on the input before compensation. Earlier it was specified that the minimum pace signal we would like to detect is 100µs in width, therefore, an amplifier of, at least, a decade greater bandwidth is preferred. Depending on the duration of the pace pulse slope, the output may swing close to the power rails, requiring a rail to rail out op amp. The OPA348 was chosen because it has 1MHz bandwidth, is capable of reaching within 25mV of the rail, and maintains adequate bandwidth, while staying cost effective in the TI value line of devices. A wider bandwidth op amp can be selected to provide more flexibility on the high pass filter design prior to compensation for stability.

3.2 Differentiator V_{bias} Voltage Selection

The role of the V_{bias} voltage is to set the dc operating point to the window comparator input when a pace pulse is not detected. This becomes the idle voltage state of the window comparator input used to set the high and low threshold values of the individual comparators. By setting V_{bias} to 2.5V, the midpoint of the system power supplies, the swing of individual comparators is maximized in either the positive or negative direction. Adjusting the V_{bias} value would require that the window comparator threshold voltages are properly set.

3.3 Comparator Device Selection

The window comparator circuit design requires two comparators sharing a common output that each has the ability to control. Open drain output comparators allow for either device to pull the line low when the window comparator input voltage exceeds set voltage values. The TLV3401 was chosen for its open drain output and small package option. The TLV3402 is a secondary option as it includes two devices per package.

3.4 NAND Gates for SR Latch Selection

Two NAND gates are required for the SR latch design with adequate propagation delay. The SN74LVC2G00 was chosen for its two devices per package and t_{pd} max of under 5ns. A simple push button switch will work for the reset.

3.5 Passive Component Selection

The differentiator circuit design and window comparator threshold design are the two paths for which the passive component selection values are critical for this design. To meet the design goal of the differentiator circuit responding to the pace signal, the resistor tolerance values of the passive components setting the high pass filter were chosen to be 1%.

Resistors R_3, R_4, R_5, and R_6 in Figure 6 set the threshold values for the window comparator. These threshold voltage values may be set very close to the dc operating point set in the differentiator stage, in order to meet the specification of responding to a 2mV amplitude, 100µs period pace signal. Therefore, resistor tolerances of 0.1% were chosen to set the voltages as accurate as possible. When this was not possible due to reasonable cost or availability, the tolerance of the resistor was chosen to be 1%. The values, themselves, were obtained experimentally during TINA-TI™ simulation and then modified based on lab testing.

Other passive components in this design may be selected for 1% or greater as they will not directly affect the transfer function of this design.

4 Simulation

The TINA-TI™ schematic shown in Figure 8 includes the circuit values obtained in the design process. The first OPA348 in a unity gain buffer configuration is used to model the internal buffer of the ADS1298 prior to the V_PACE_OUT pin.

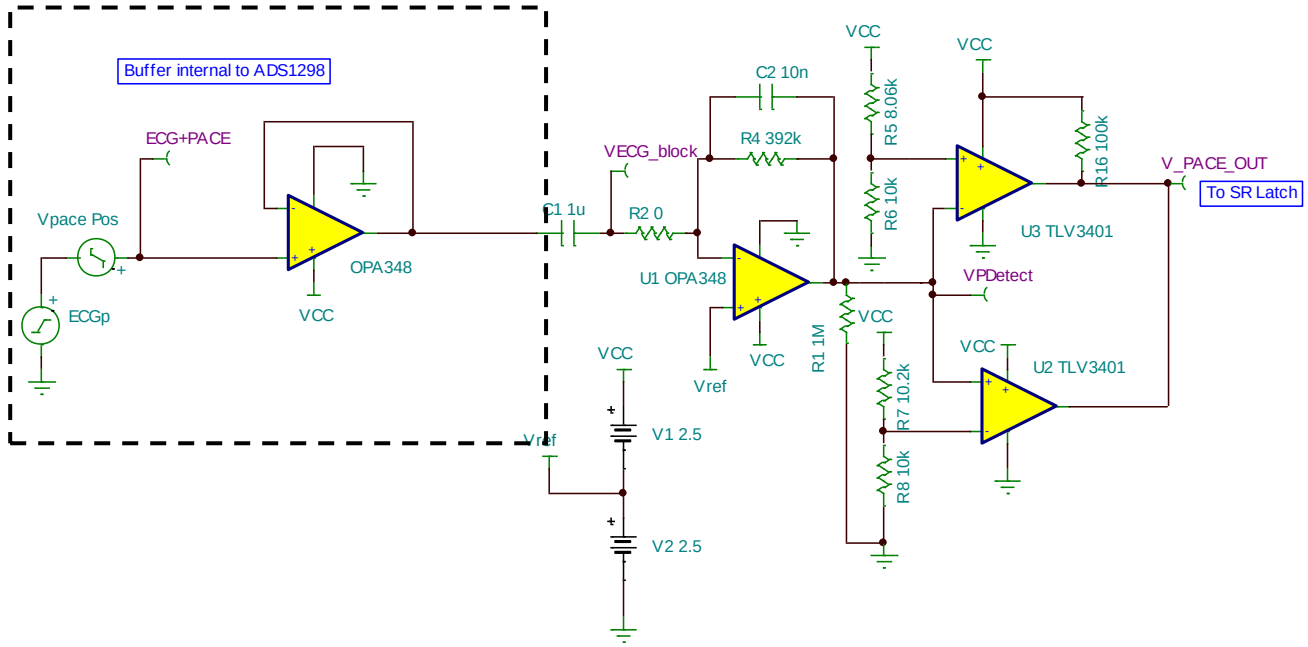

Figure 8: TINA-TI™ Schematic

4.1 Time Domain Analysis

The transient analysis is first performed to get an understanding of the events at each stage of the circuit. ECGp and Vpace Pos are arbitrary waveforms used to model a typical ECG pulse with a 2mV, 100µs pace signal beforehand, similar to what is shown in Figure 2. VPDetect is the output from the differentiator which is used to get an understanding of where to set the voltage threshold levels for the window comparator. V_PACE_OUT is the output from the window comparator which will get pulled low when VPDetect appears outside of the set boundaries. The time domain response is shown in Figure 9.

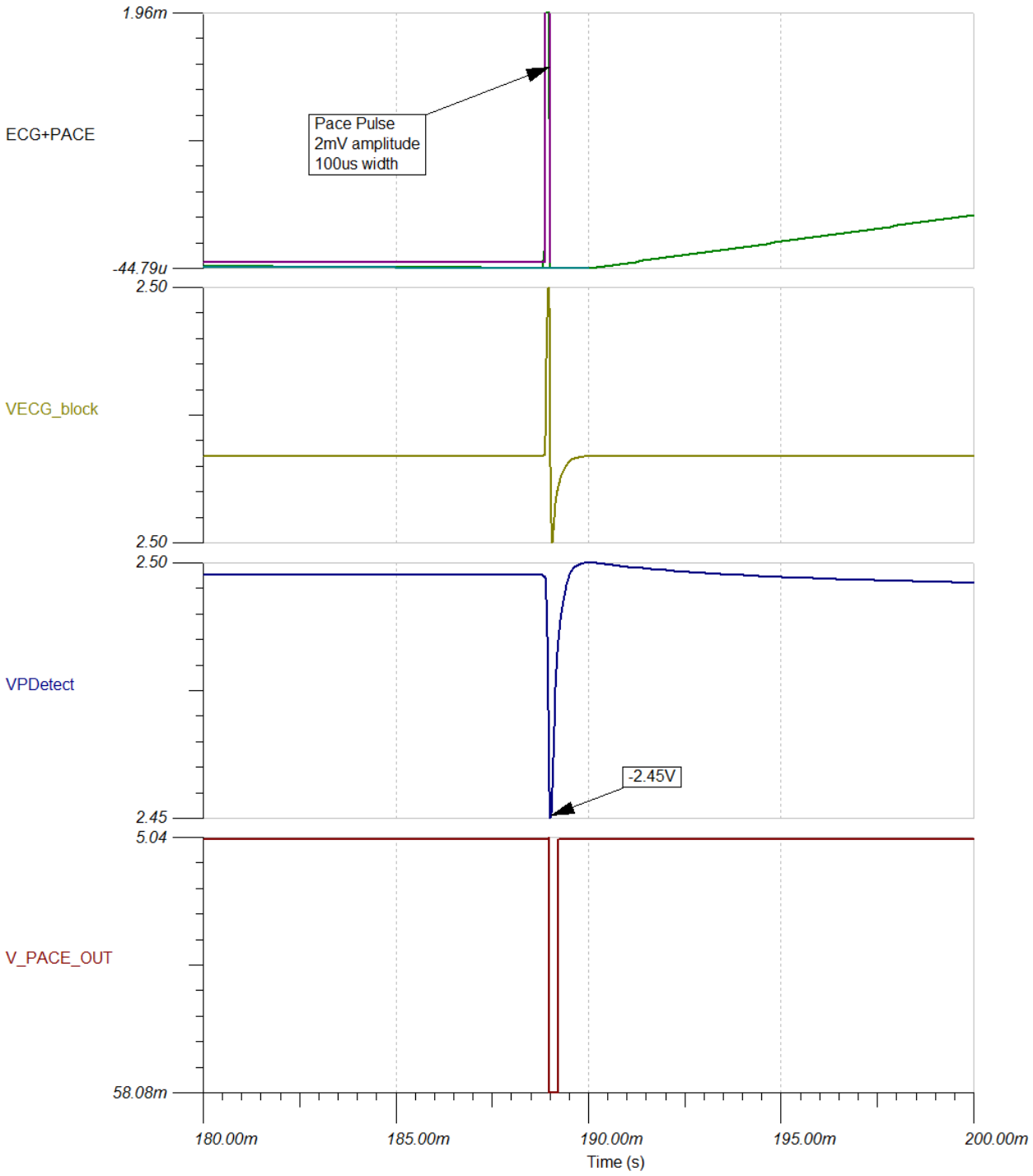

Figure 9: TINA-TI™ - Transient Response

The simulation results in Figure 9 are used to make any adjustments to the window comparator levels if a latch does not take place. VPDetect reaches a value of 2.45V when the target of a 2mV, 100µs pace signal is applied to the input. Giving a little room for error, a level of 2.48V is used for the lower limit.

4.2 Step Response

The time domain step response of the differentiator stage can be seen in Figure 10 to verify stability.

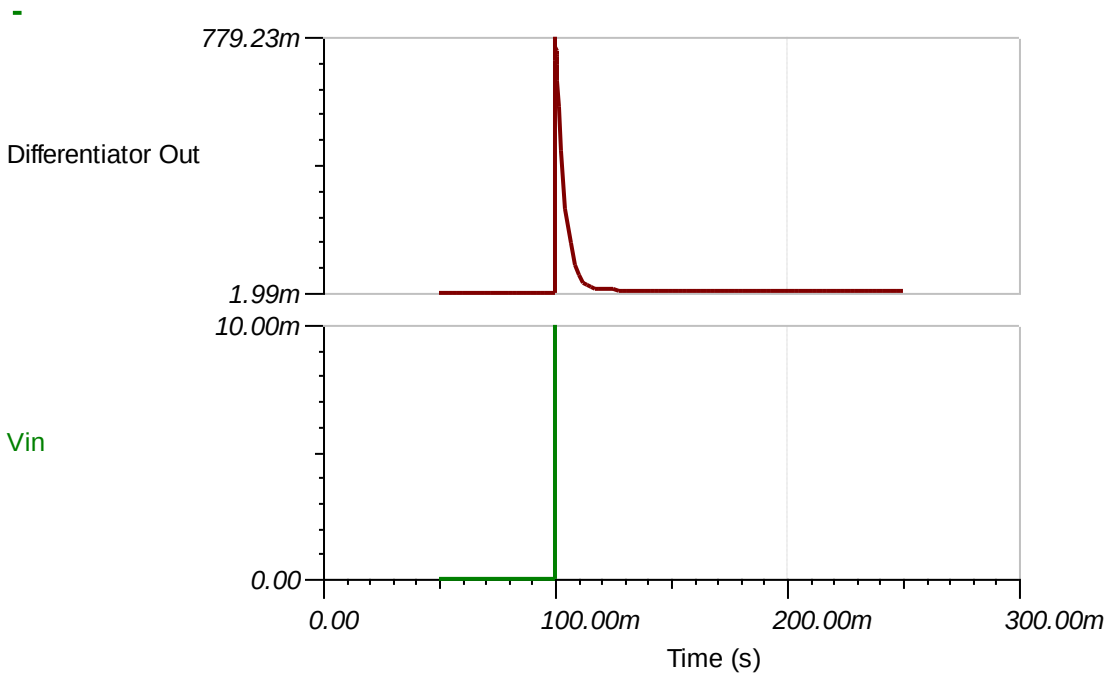

Figure 10: TINA-TI™ - Step Response

At the moment of the step input, there is a large spike on the Differentiator Out (VPDetect) relative to the slope before stabilizing to a steady DC value. This is the expected behavior of the differentiator circuit without ringing or oscillations verifying that we have a stable design.

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The layout of the ECG hardware pace board was designed to pair with the ADS1298ECG-FE board requiring minor modifications to the connecting headers. General layout practices based on the general PCB Layout Guidelines document found on the e2e Wiki were followed. The PCB layout for this design is shown in Figure 11.

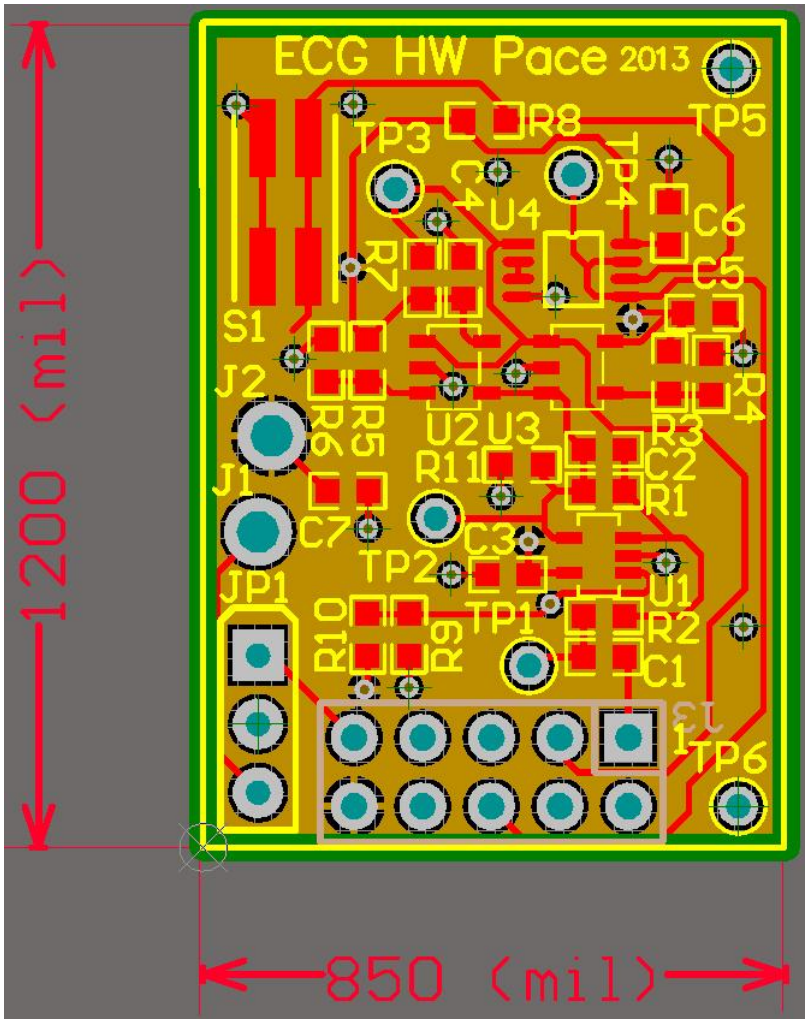

Figure 11: PCB Layout

6 Verification & Measured Performance

6.1 Time Domain Analysis

This circuit is required to pass functionality tests comparing the real-world circuit performance to expectations from the TINA-TI™ simulation and the requirements laid out in the Design Summary. Test points were included in the board design at the VPDetect, V_PACE_OUT, and the SR Latch points out to monitor signal progress through the circuit. Figure 12 displays the transient analysis results when a 20mV amplitude, 100µs period pacemaker pulse is applied prior to the QRS interval. The Fluke Medsim 300B was used to simulate a pacemaker pulse and ECG signal.

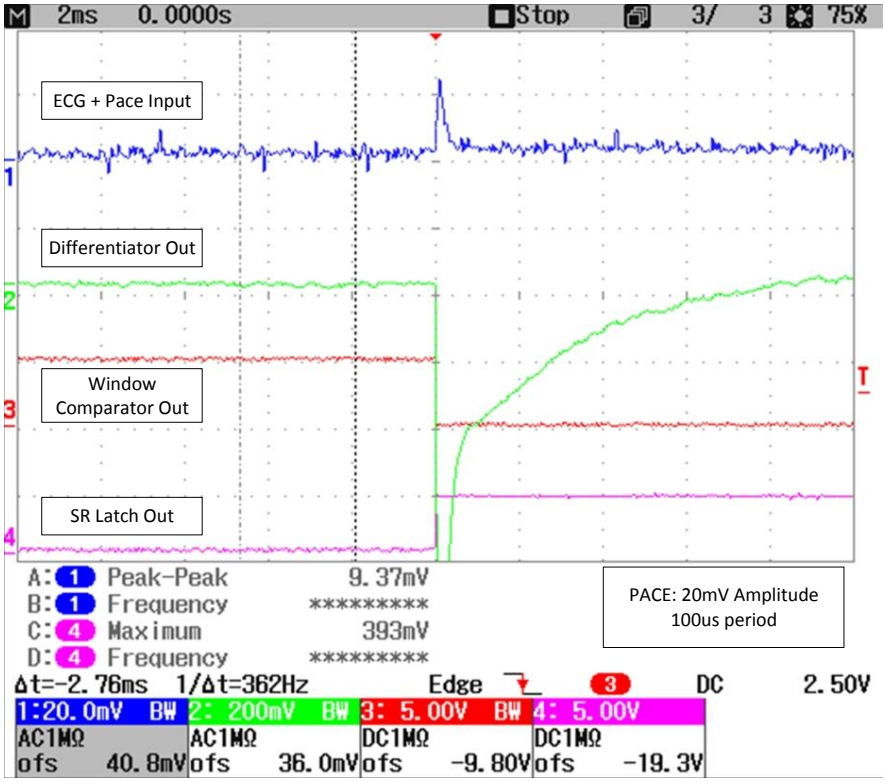

Figure 12: Time Domain Results (20mV amplitude)

A 20mV pace signal amplitude was first selected to show a visual demonstration of how a pace signal (shown on channel 1) will cause the SR latch to change to a high state (shown on channel 4).

Once functionality has been proven in Figure 12, a second test is required to demonstrate circuit response to a 2mV amplitude and 100µs period pulse width pace signal. Figure 13 displays the transient analysis for these conditions which can be compared to the Figure 9 simulation results.

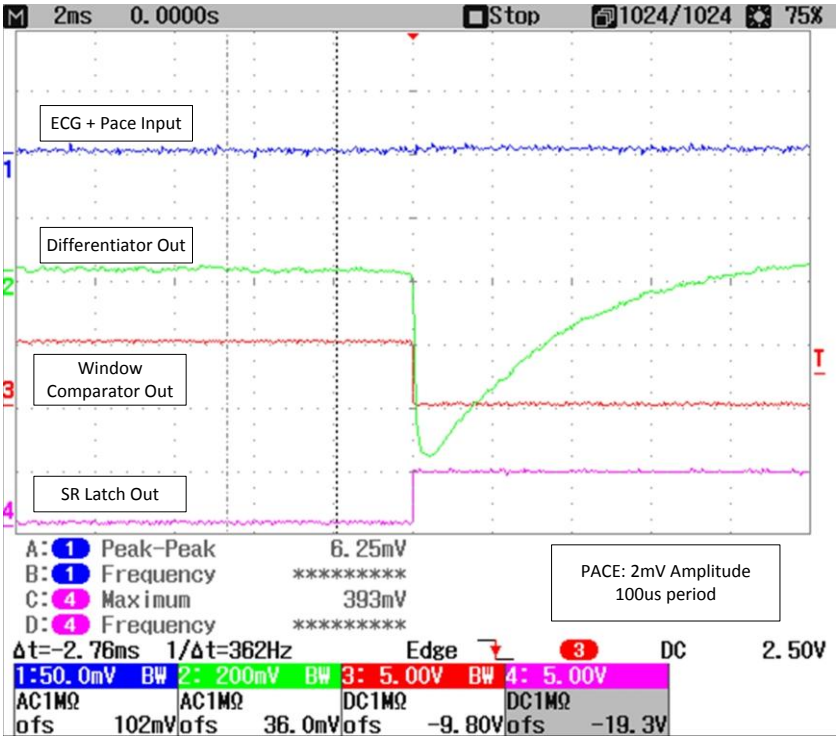

Figure 13: Time Domain Results (2mV Amplitude)

The 2mV amplitude pacemaker signal does successfully trigger the window comparator and SR latch indicating an event. Figure 12 and Figure 13 also show how the amplitude of the differentiator out circuit is dependent on the duration of the input pacemaker slope. This concludes testing verification of the hardware pace detection circuit.

7 Modifications

The components selected for this design were based on the design goals and outlined at the beginning of the design process. Those goals are focused on monitoring for a 2mV positive polarity pacemaker pulse that can be as small as 100µs in signal width. In reality, a pacemaker can be positioned in the body a variety of ways, where the monitored pacemaker signal could either read back with positive or negative polarity. Following the design method described above, R_5 and R_6 can be selected for the circuit to respond to a negative polarity pace signal in addition to the positive pulse.

The first order high pass filter and slope detection circuit is designed to demonstrate how manipulation of frequency components can alert a user when a pace maker signal is present prior to the ECG signal. All tests in this document were performed with a Fluke patient simulator, not taking into account any motion artifacts which would be present in a commercial medical system. This circuit is not designed to be used directly with a patient without proper IEC certification.

When designed to be used in a patient monitoring system, additional design effort is required to help filter motion artifacts which will cause false positive triggers. The poles and zeroes on the differentiator may need to be manipulated to further attenuate the lower frequency components avoiding unwanted triggers on the window comparator. Additional gain may be required on the differentiator circuit to allow a wider range on the window comparator threshold limits to help with motion artifacts. Adding gain to the differentiator circuit will allow the threshold limits to be pushed further away from the idling voltage, set by V_{bias}. Designing a second order high pass filter may be required to help attenuate the lower frequency components while providing enough gain at the higher frequencies to help with motion artifacts. A wider bandwidth op amp in the differentiator stage can also help improve the gain before stability compensation.

Moving forward, software detection methods are becoming a more accurate way to monitor for a pace maker. Using a wide bandwidth SAR ADC, the ECG and pace signal can be digitized and then processed to remove unwanted signal components. The Q-T interval can be removed, along with electromyography (EMG) signals from muscle movement and any other motion artifacts leaving solely the pace maker signal components. Further algorithms can be put in place to not only alert the user if a pacemaker is present, but also provide details about the pace device.

8 About the Author

Tony Calabria is a Systems Engineer and Product Definer in the Delta Sigma ADC group at Texas Instruments where he supports medium to wide bandwidth Delta Sigma ADCs. Tony received his BSEE from the University of Arizona.

9 References

1. *Green, T., Operational Amplifier Stability, Parts 1 – 11, November 2008, http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712*

Appendix A.

A.1 Electrical Schematic

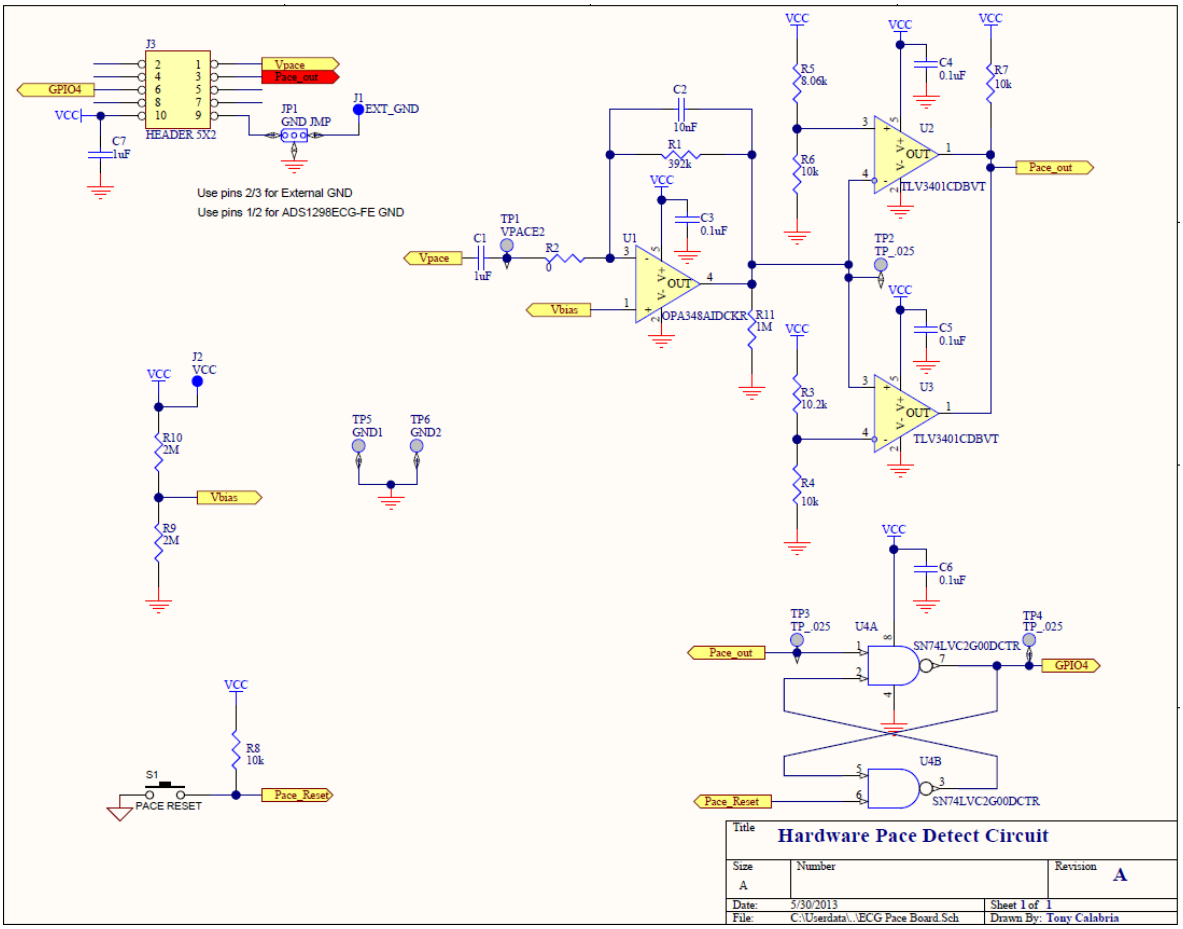

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	Qty	Value	Designator	Description	Manufacturer	Part Number	Supplier Part Number
1	2	1uF	C1, C7	CAP CER 1UF 25V 10% X7R 0603	Taiyo Yuden	TMK107B7105KA-T	587-2984-1-ND
2	1	10000pF	C2	CAP CER 10000PF 50V 5% X7R 0603	AVX	06035C103JAT2A	478-5007-1-ND
3	4	0.1uF	C3, C4, C5, C6	CAP CER 0.1UF 50V 10% X7R 0603	TDK	C1608X7R1H104K	445-1314-1-ND
4	2	Red	J1, J2	TEST POINT PC MULTI PURPOSE RED	Keystone	5010	5010K-ND
5	1		J3	CONN RCPT .100" 10POS DUAL TIN	Samtec	SSW-105-01-T-D	SAM1212-05-ND
6	1		JP1	3 Position Jumper _ .1" spacing	Samtec	TSW-103-07-T-S	SAM1035-03-ND
7	1	392k	R1	RES 392K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-07392KL	311-392KHRCT-ND
8	1	0	R2	RES 0.0 OHM 1/10W 0603 SMD	Yageo	RC0603JR-070RL	311-0.0GRCT-ND
9	1	10.2k	R3	RES 10.2K OHM 1/10W 0.1% 0603 SMD	Panasonic	ERA-3AEB1022V	P10.2KDBCT-ND
10	4	10k	R4, R6, R7, R8	RES 10K OHM 1/10W 0.1% 0603 SMD	Panasonic	ERA-3AEB103V	P10KDBCT-ND
11	1	8.06k	R5	RES 8.06K OHM 1/10W 0.1% 0603 SMD	Panasonic	ERA-3AEB8061V	P8.06KDBCT-ND
12	1	1M	R11	RES 1.00M OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-071ML	311-1.00MHRCT-ND
13	2	2M	R9, R10	RES 2.00M OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-072ML	311-2.00MHRCT-ND
14	1		S1	SWITCH TACTILE SPST-NO 0.02A 15V	Panasonic	EVQ-P2002M	P12296SCT-ND
15	4	Red	TP1, TP2, TP3, TP4	TEST POINT PC MINI .040"D RED	Keystone	5000	5000K-ND
16	2	Black	TP5, TP6	TEST POINT PC MINI .040"D BLACK	Keystone	5001	5001K-ND
17	1		U1	IC OPAMP GP R-R 1MHZ SGL SC70-5	TI	OPA348AIDCKT	296-27989-1-ND
18	2		U2, U3	IC COMPARATOR SGL OD OUT SOT23-5	TI	TLV3401IDBVR	296-13376-1-ND
19	1		U4	IC DUAL 2-IN POS-NAND GATE SM8	TI	SN74LVC2G00DCTR	296-13257-1-ND

Figure A-2: Bill of Materials

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