User's Guide

ADC366xEVM Evaluation Module

Abstract

This user's guide describes the characteristics, operation, and use of the ADC366x evaluation module (EVM). This user's guide discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADC366xEVM. In the following sections of this document, the ADC366x evaluation board is referred to as the EVM and the ADC366x devices are referred to as the ADC devices, respectively. This document applies only to the ADC3663EVM and ADC3662EVM.

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1 Introduction

The ADC366xEVM is an evaluation board used to evaluate the ADC366x analog-to-digital converters (ADC) from Texas Instruments. The ADC366x uses a serial LVDS interface to output the digital data. The serialized LVDS interface supports output rates to 1 Gbps. The ADC366x can be operated in 'oversampling + decimating' mode using the internal decimation filter in order to improve the dynamic range and relax external anti-aliasing filter.

The ADC366xEVM is equipped with the following features:

- Transformer and FDA coupled analog inputs
- CDCE6214 clocking solution for on-board clocking
- Transformer coupled or single-ended clock inputs
- INA226 current shunt monitors for evaluating power consumption
- Power over mini-USB
- FMC connector

By default, the EVM is configured to receive external inputs for the sampling clock and analog input via AC-coupled, transformer (balun) inputs. These transformers perform single-ended to differential conversion, and provide a low noise/distortion passive input.

To exercise the full performance capabilities of this high performance SAR ADC, it is recommended to evaluate the ADC in the default configuration, and then evaluate in other configurations (like onboard clocking or FDA input), as required.

2 Equipment

This hardware setup procedure is written with the intent to use external clocking (sample clock and DCLKIN) and transformer coupled analog inputs. Using onboard clocking and FDA driven analog inputs is an option, and instructions are provided toward the end of this document to make the required hardware/software modifications.

2.1 ADC366xEVM Functionality

The ADC366xEVM receives power from the USB 2.0, +5 V rail, and is then converted to +3.3 VDC and +1.8 VDC. The ADC receives +1.8 VDC from the TPS62231 DC-DC converter. The power consumption of the 1.8 V rail can be monitored (using the INA226) in the ADC35xxEVM GUI. USB-to-SPI communication is established using the FTDI (FT4234H). The ADC clocks can be supplied externally or from the onboard PLL/Distributor CDCE6214 (high quality external clocks are used to acheive best AC performance). The analog input can be AC coupled through the Balun (ADT1-6T+) input, or DC (or AC) coupled with the onboard FDA (THS4541). The analog input is 3.2 Vpp, and is driven a -1 dBFS (~2.8 Vpp) in all examples in this user's guide.

The ADC366x family has a +1.6 V voltage reference (VREF), and can be supplied internally or externally. By default, the EVM is configured to supply an external voltage reference using the REF3318 (divided down to +1.6 V) and the OPA837 high speed amplifier to drive the voltage reference. At any time, the VREF can be changed to internal reference by SPI write.

The ADC366x family uses an unbuffered analog input, so a glitch filter is required to attenuate the ADC sampling glitch from when the sampling capacitors switch (sample/hold). The glitch filter acts as a low pass filter with an corner frequency (Fc) at 30 MHz (accepts DC to 30 MHz).

The ADC366xEVM LVDS output data is routed to an FMC connector, and then connected to the LVDS Interposer card. This interposer card then maps to the TSW1400EVM HSMC connector in order to capture the ADC366xEVM SLVDS clock and data signals.

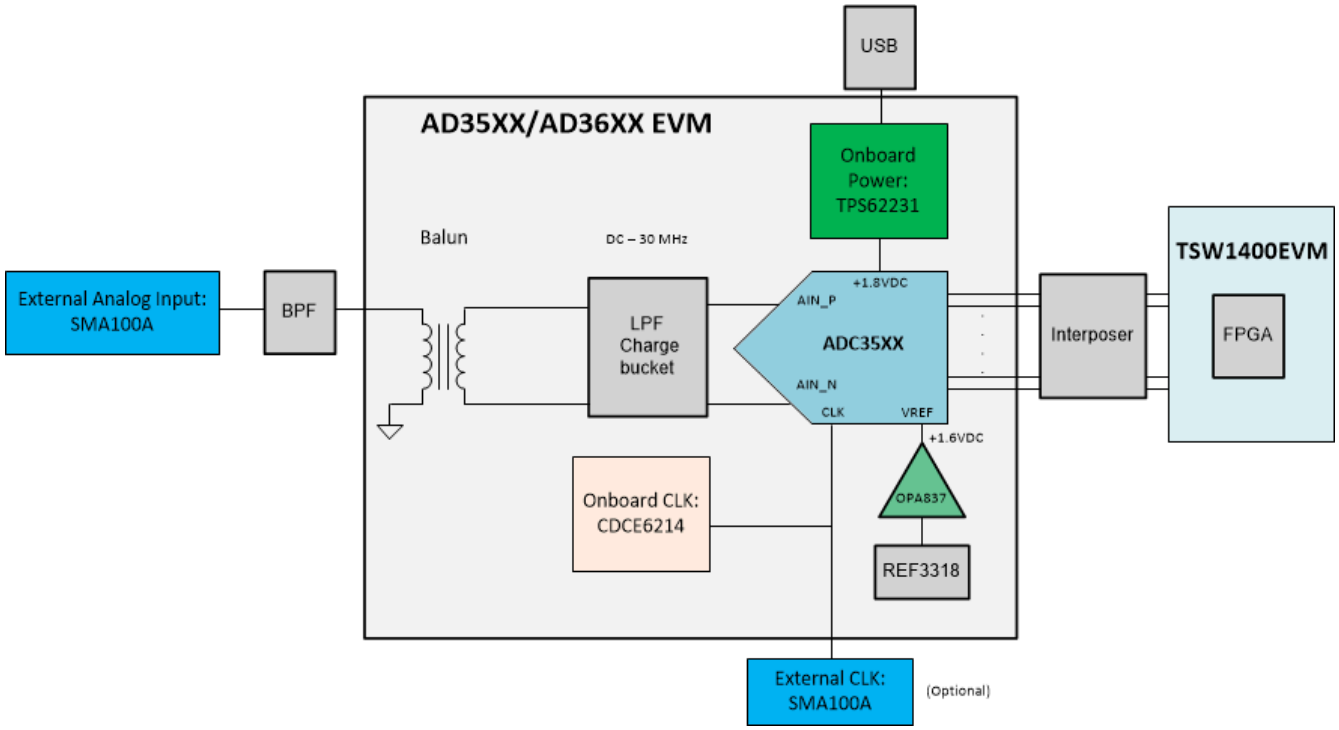


Figure 2-1. ADC36xxEVM block diagram: Balun input

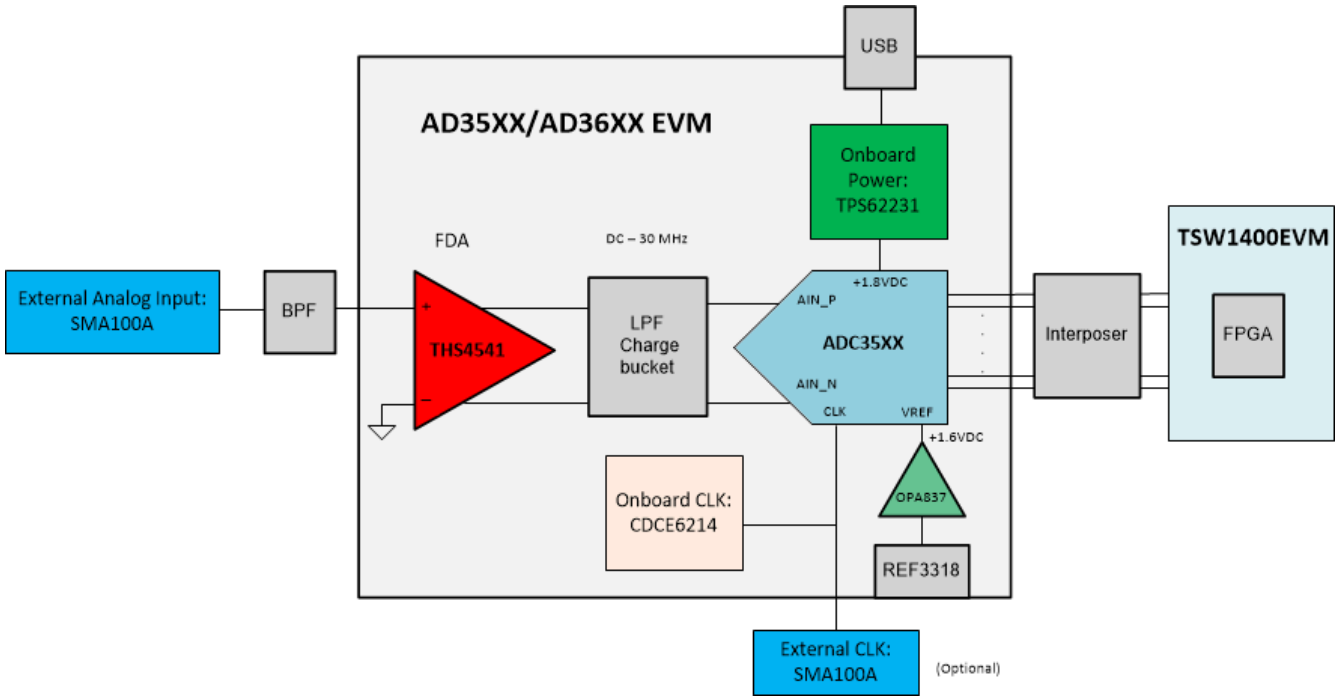


Figure 2-2. ADC36xxEVM block diagram: FDA input

2.2 Evaluation Board Feature Identification Summary

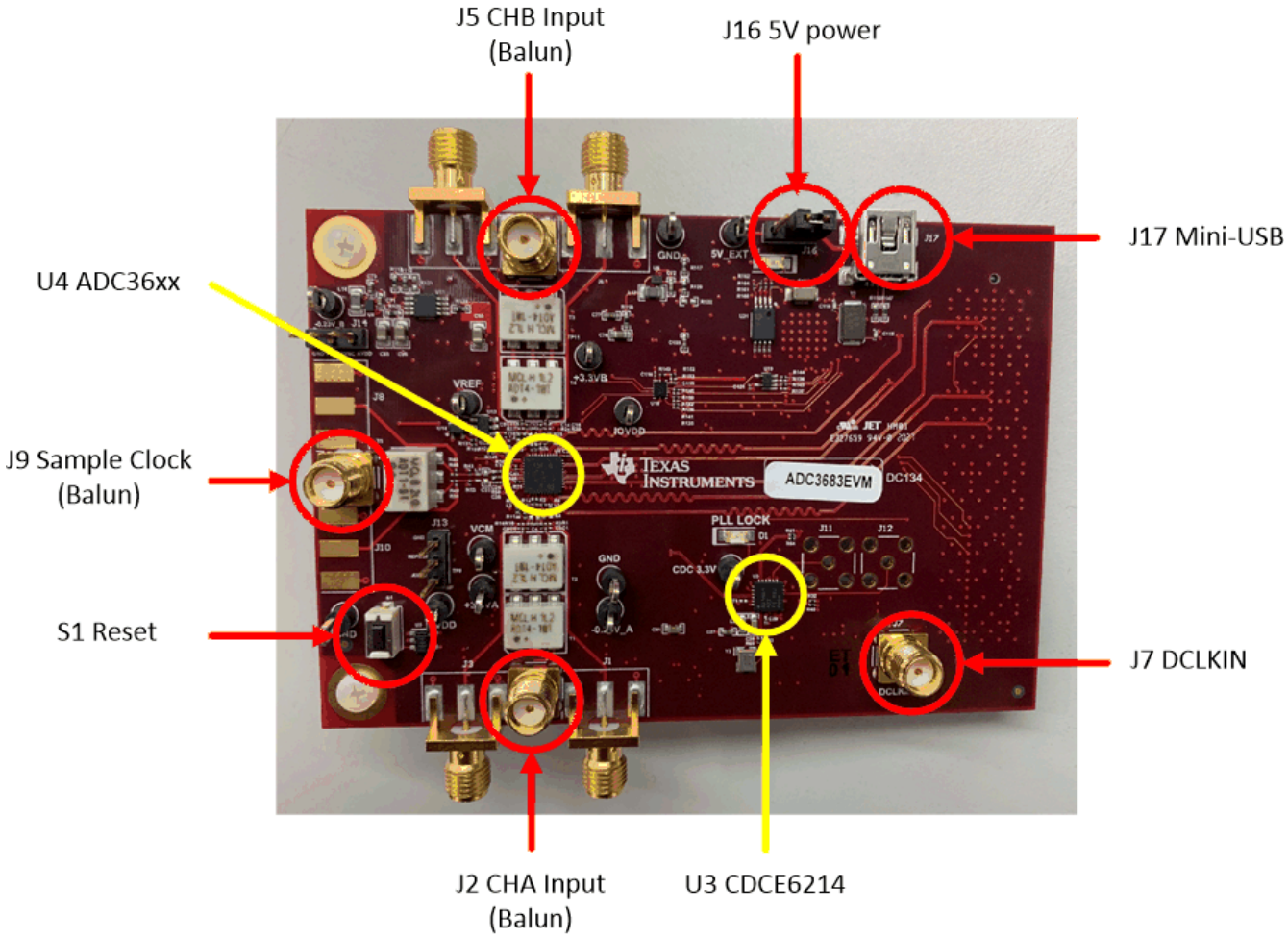


Figure 2-3. ADC366xEVM Feature Identification

Ensure that jumper J16 is shunted in the 2-3 position. This allows 5 V to be supplied to the ADC366xEVM through the mini-USB connector.

If an external 5-V supply is desired, J16 must be shunted in the 1-2 position, and the external 5 V can be connected to the test point labeled "+5 EXT". The USB data connection is still connected for SPI communications.

J13 is tied to the REFBUF pin. It can be left floating, or can be tied to 1.8 V (shunt pins 2-3) for normal operation.

J14 is tied to the PDN/SYNC pin. It can be left floating for tied to ground (shunt pins 1-2) for normal operation. To power down the ADC, tied to 1.8 V (shunt pins 2-3). The ADC may also be powered down via SPI.

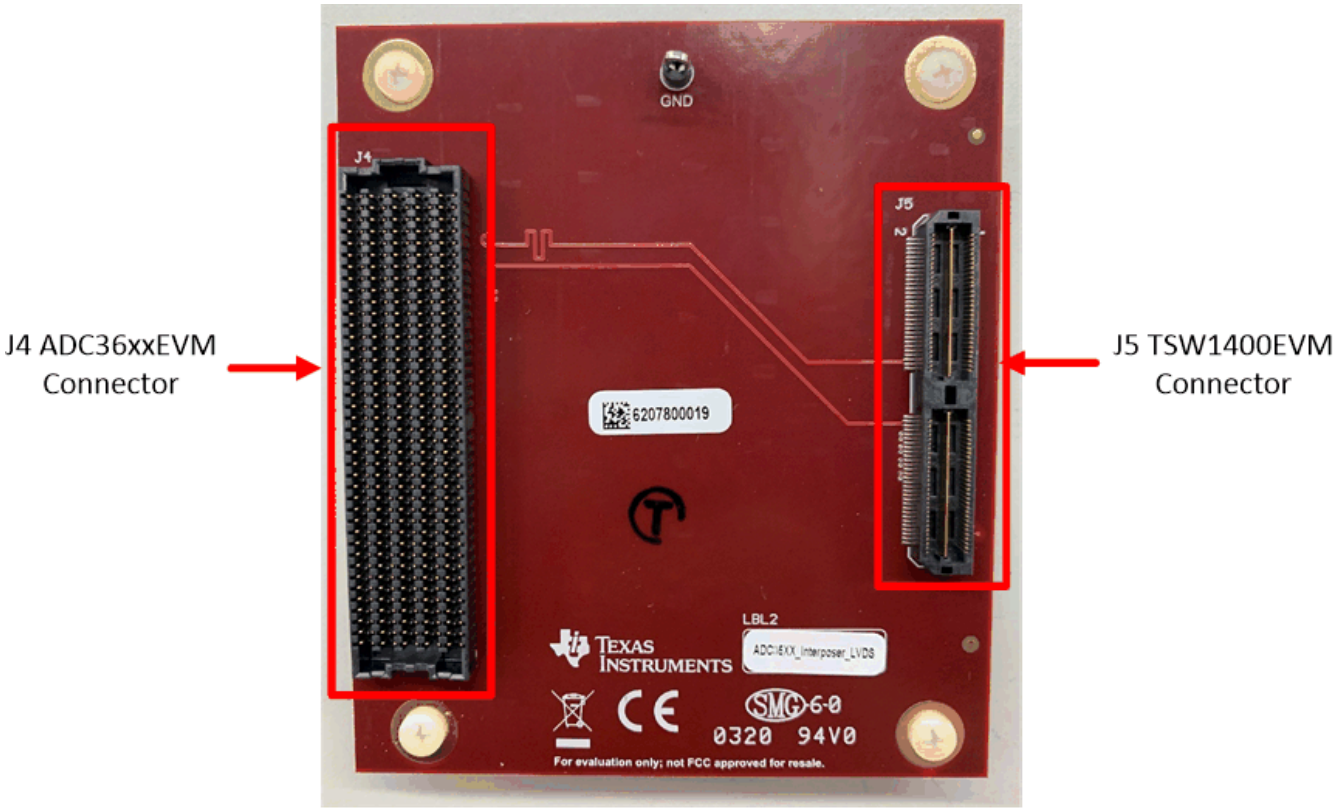


Figure 2-4. LVDS Interposer

2.3 Required Equipment

- The following equipment is included in the EVM evaluation kit:
  - ADC366xEVM Evaluation board (EVM)
  - LVDS FPGA Interposer Card
  - Mini-USB cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this EVM:

- TSW1400EVM data capture board and related items
- HSDC Pro software
- PC running Microsoft® Windows® 7, or 10
- One low-noise signal generator for the analog input (If using onboard clock option, no additiona signal generators are required).
- Two low-noise signal generators for the sample clock and DCLKIN. (These two signal generators must share the same reference frequency).

TI recommends the following generators:

- Rohde & Schwarz SMA100A
- Rohde & Schwarz SMA100B

A bandpass filter is required for the analog input signal due to most signal generators addition of phase noise or spurious components. A bandpass filter should also be used for the sample clock input. The DCLKIN input does not require a bandpass filter. If bandpass filters are not used, then the true performance of the ADC may not be seen clearly, and is limited by the performance of the signal generators being used.

The following recommended bandpass filter have:

- Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
- Signal-path cables, SMA

3 Setup Procedure

This Setup Procedure will detail how to setup the ADC366xEVM hardware and software GUI required for evaluation using external sample and DCLKIN clocks. The clock rates in the following steps apply specifically to the ADC3663EVM, but example clock rates are provided for other EVM variants.

3.1 Install High-Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software. Launch the executable, and accept the default installation options.

3.2 Install ADC35XXEVM GUI 1.0 Software

Download the ADC35XXEVM GUI 1.0 software from the EVM tool folder at ADC3663EVM.

Extract and run the executable file, and accept the default installation options.

3.3 Connect the ADC366xEVM and TSW1400EVM

Connect the ADC366xEVM FMC connector to J4 of the LVDS Interposer Card.

Connect J5 of the LVDS Interposer Card to J1 of the TSW1400EVM.

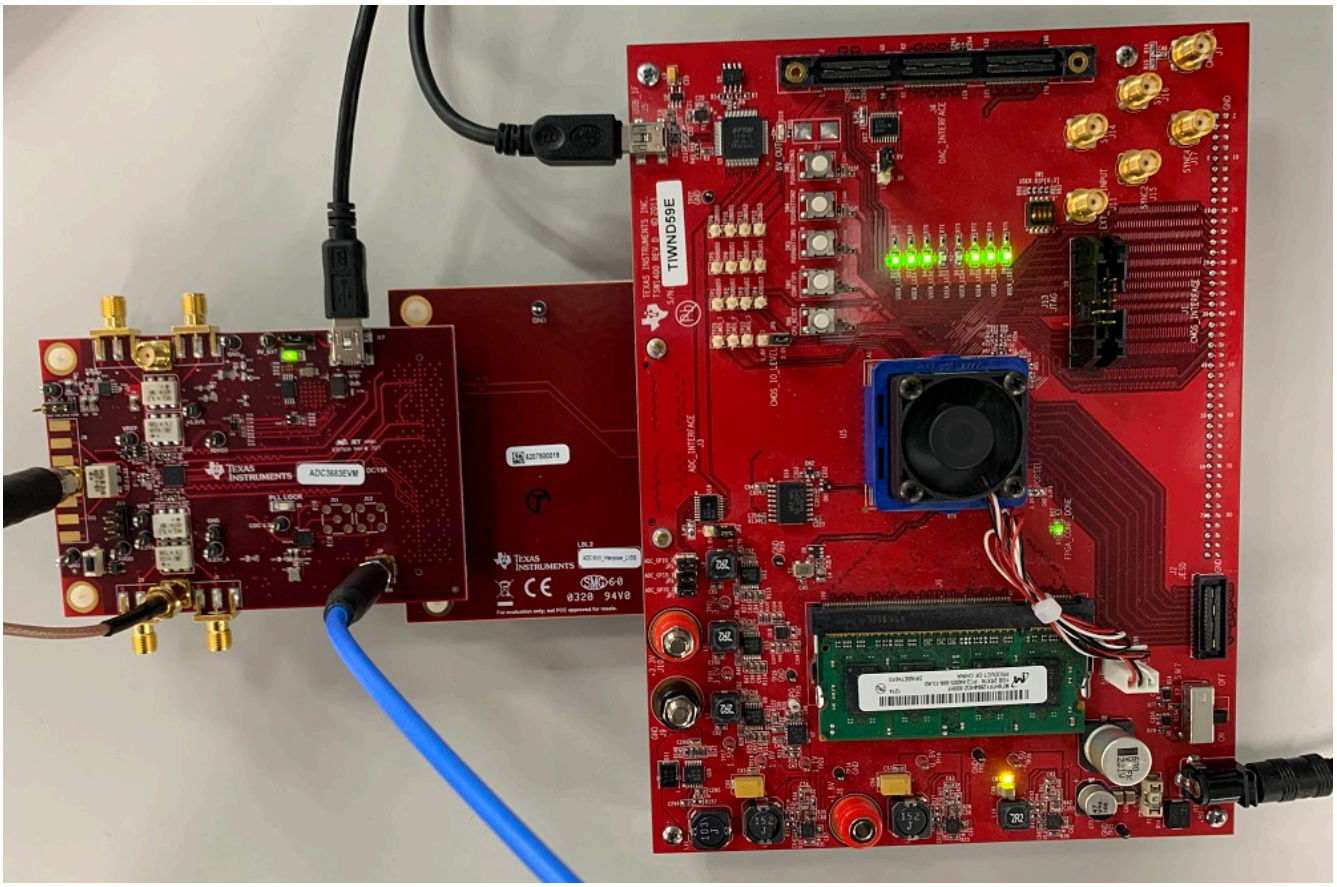


Figure 3-1. ADC366xEVM Complete Setup (external clocks)

3.4 Connect the Power Supply and Mini-USB Connections

Use the following steps to connect the power supply and mini-USB connections:

1. Connect the power cable to the TSW1400EVM at 5-V (minimum 3 A) power supply. Place the power switch (SW7) to the "On" position.
2. Connect the mini-USB cable to the TSW1400EVM (J2).
3. Connect the mini-USB cable to the ADC366xEVM (J16).

3.5 Connect the Clocks and Analog Input

Use the following steps to connect the external ADC clocks and analog input. If onboard clocking is to be used, follow the instructions in the section Onboard Clocking Hardware Setup.

The clock frequencies shown below are for the power on/default settings (bypass mode/non-decimation) for the ADC3663EVM, but the physical connections and signal power levels will remain the same for all ADC modes.

- For the sample clock (ADC3663EVM), set a signal generator to 65 MHz at a power level of +10 dBm. Connect to the SMA connector J4. A bandpass filter for the sample clock is recommended for best AC performance of the ADC366xEVM.
- For the DCLKIN clock (ADC3663EVM), set a signal generator to 260 MHz at a power level of +10 dBm. A bandpass filter is not required for the DCLKIN clock.

  External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

- For the analog input, set a signal generator to 5 MHz at a power level of ~ +15 dBm. A bandpass filter is required to reduce harmonic and phase noise effects of the signal generator.

4 ADC GUI Configuration

A hardware reset should be performed before programming the ADC by toggling the push button switch S1. Also, a software reset may be performed at any time to reset the ADC registers to their default state.

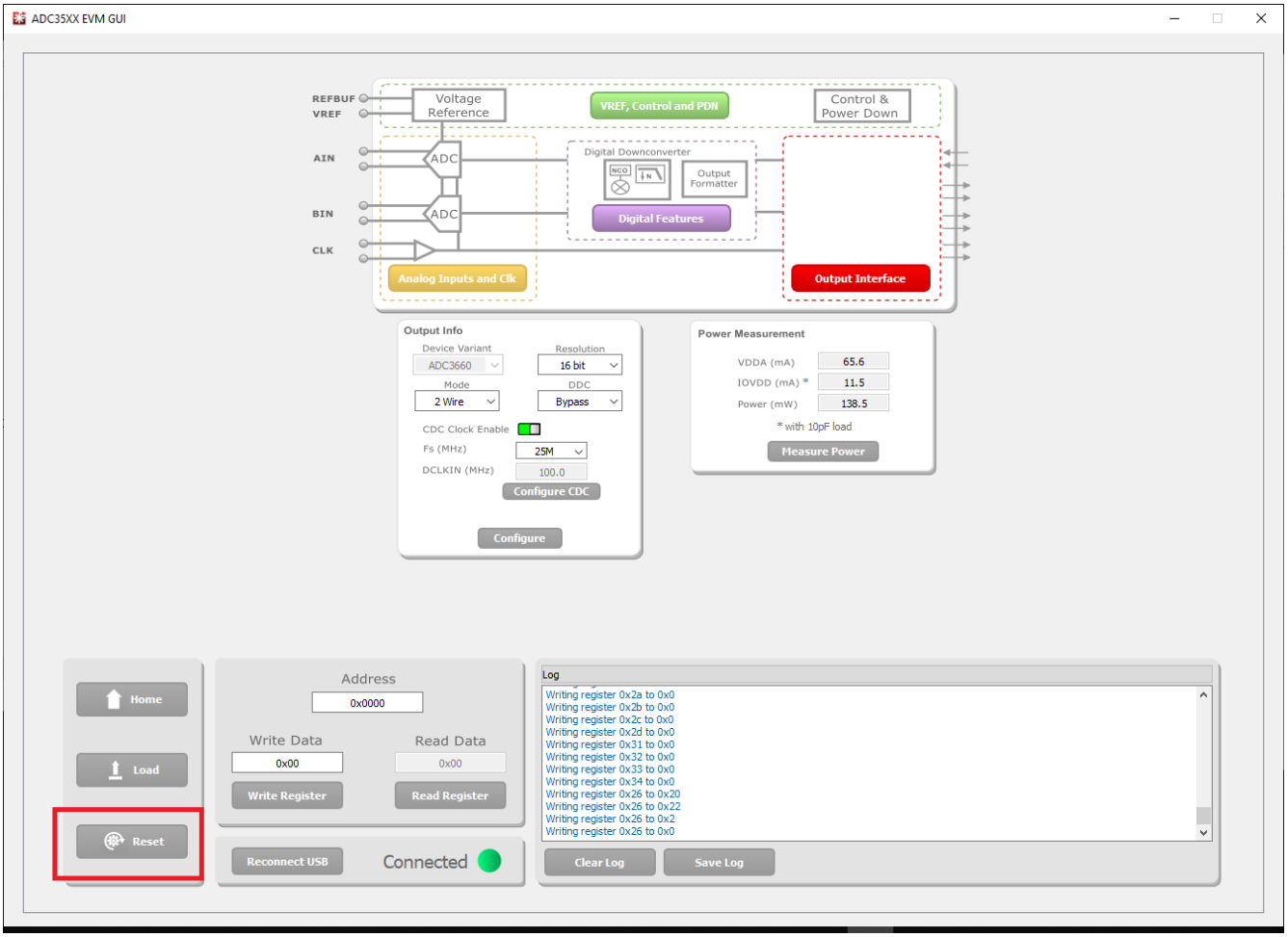


Figure 4-1. ADC35xx Software Reset

4.1 Bypass Mode

The following steps show how to configure the ADC366xEVM in Bypass mode with external sample clock and DCLKIN. These instructions show how to configure the ADC3663EVM, but apply to other EVM variants as well.

4.1.1 ADC35XXEVM GUI: Bypass Mode (2W) Configuration

The following steps for Bypass (No Decimation)mode also apply to ADC3662EVM, but requires modification to the sample/DCLKIN clocks in accordance with the desired sample rate and bit resolution. For example, at 25 MSPS, the DCLKIN rate is 25 MHz x 4 = 100 MHz.

For different sampling rates and bit resolutions, see Table 4-1 for calculating the correct DCLKIN frequency for the desired sample rate and bit resolution.

Table 4-1. 16-bit, Bypass Mode, Sample rate and DCLKIN examples (ADC3663EVM, ADC3662EVM).

Interface Mode	DCLKIN multiplier	Example Sample Clock	Required DCLKIN Frequency
2 Wire	4	65 MSPS	260 MHz
1 Wire	8	32 MSPS	256 MHz
1/2 Wire	16	10 MSPS	160 MHz

For this example, ensure that the sampling clock (J9) and DCLKIN (J7) are connected before launching the ADC35XX EVM GUI. In this example, for the ADC3663EVM, the sampling clock is 65 MHz, and the DCLKIN is 292.5 MHz.

External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data appears scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

After launching the ADC35xx GUI perform the following steps:

- Under Resolution, select "16 bit".
- Under Mode, select "2 Wire".
- Ensure that "CDC Enable" is red (disabled).
- To calculate the DCLKIN frequency, enter "65" in the Fs(MHz) field, and click calculate. This is informational only.
- Click "Configure" button.

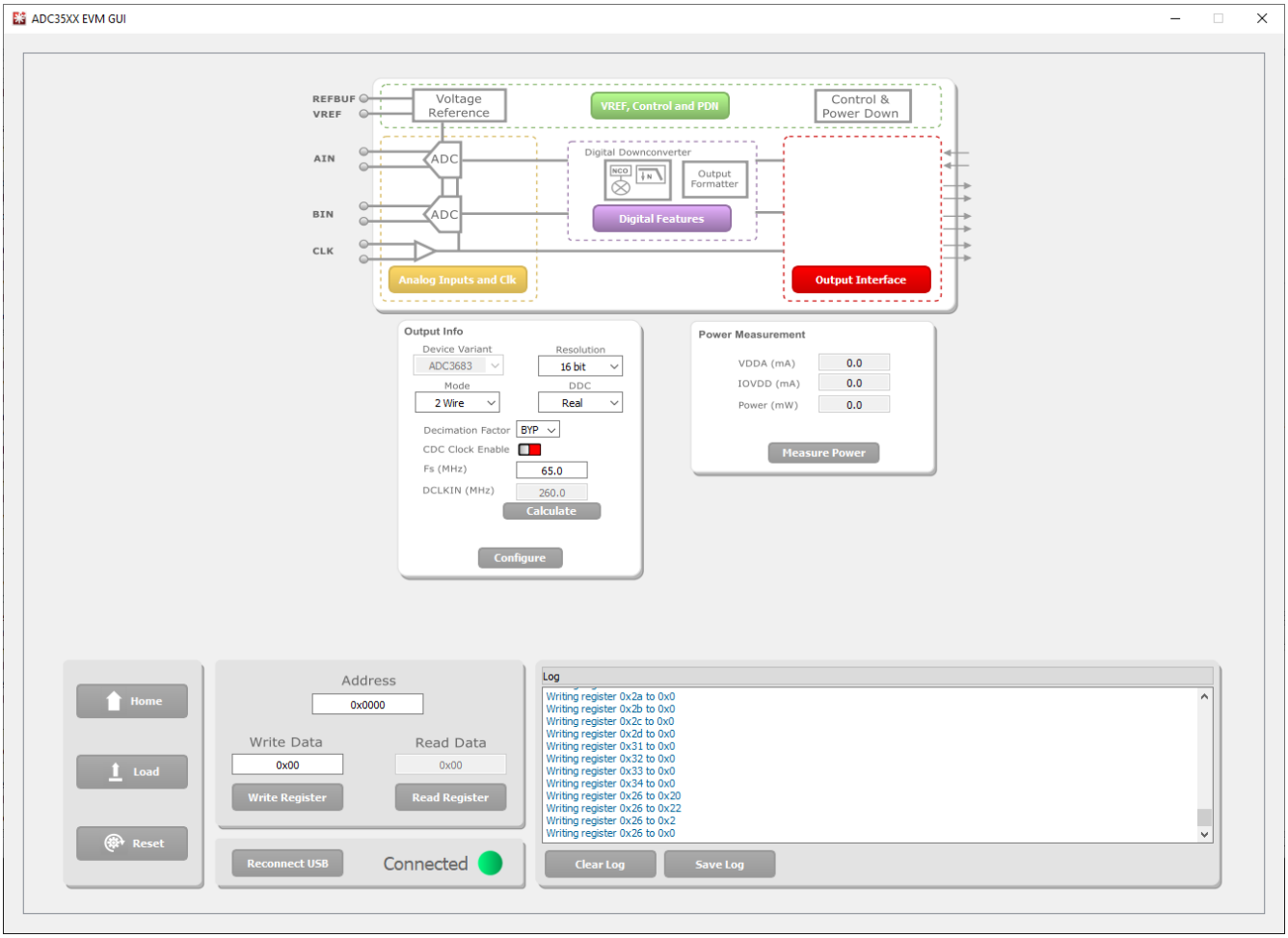


Figure 4-2. ADC35XXEVM GUI: ADC3663 Bypass Mode

4.1.2 HSDC Pro: Bypass Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro
- Select the TSW1400 and click OK

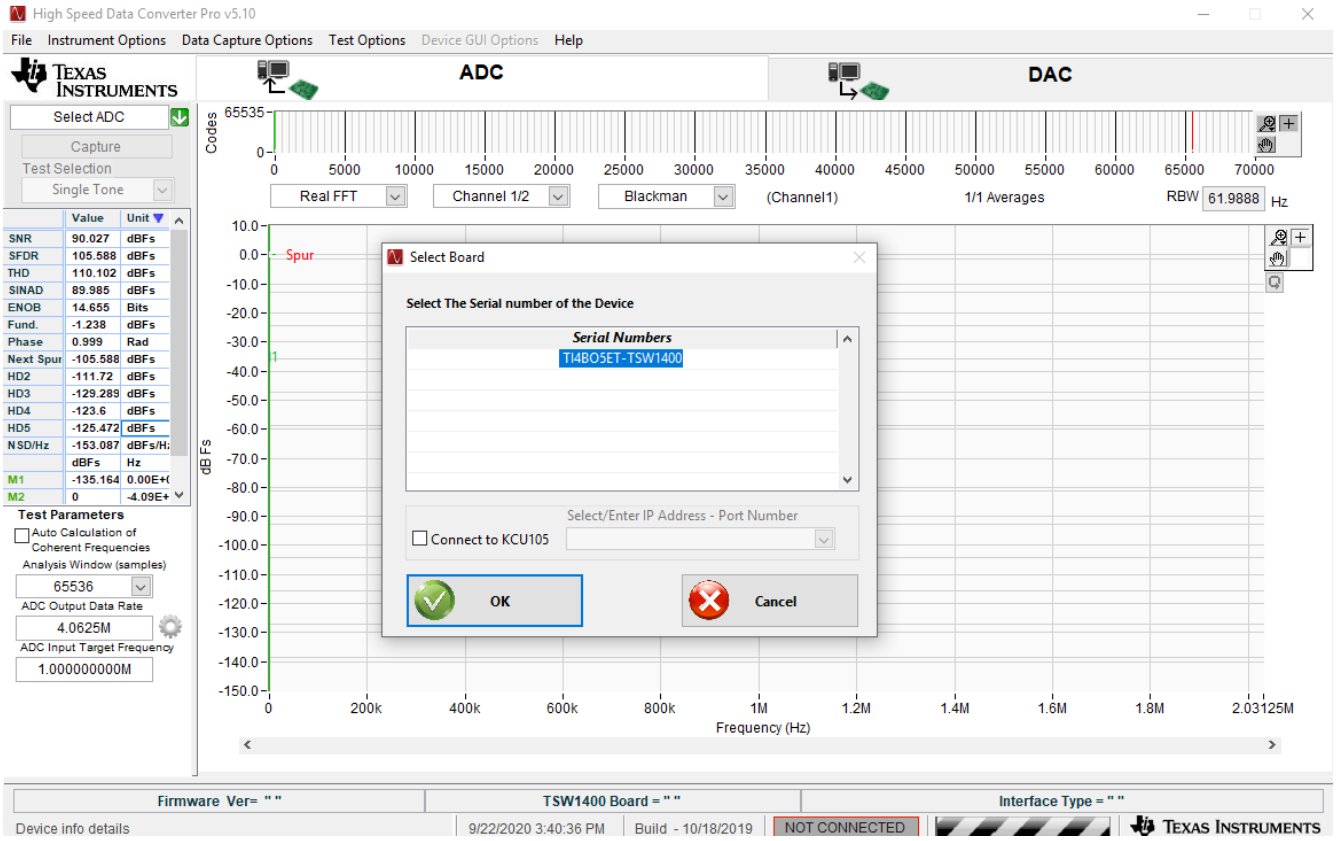
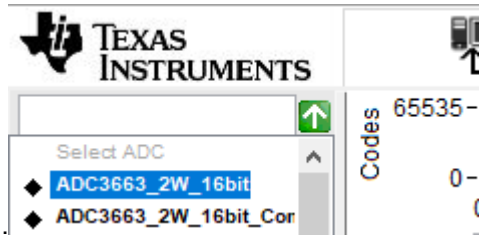
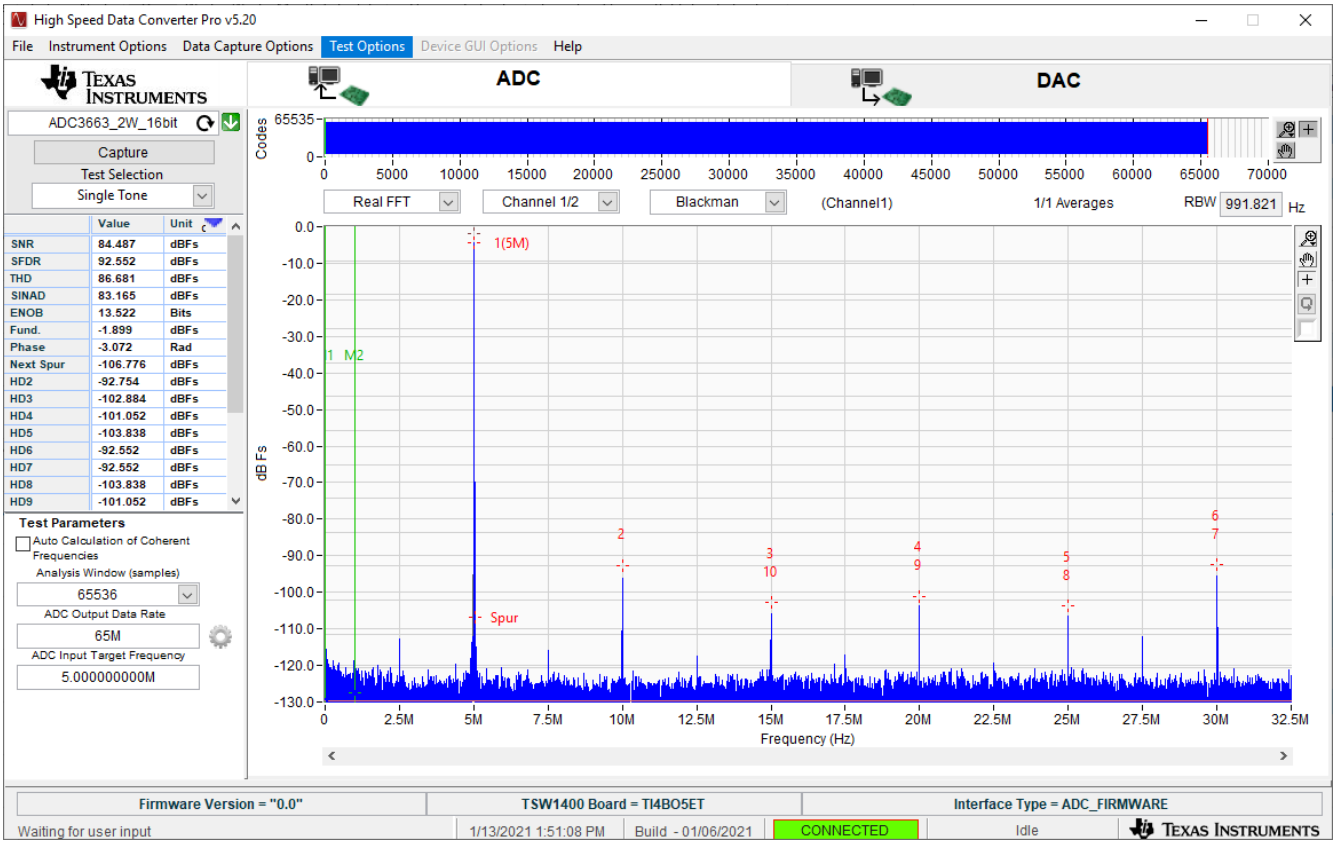


Figure 4-3. HSDC Pro: Connect to TSW1400

- Click OK for the no firmware loaded prompt.
- Select “ADC3663_2W_16bit" to load firmware, and click "Yes".



- Enter "65M" in the box that says “ADC Output Data Rate” since the ADC is sampling at 65 MSPS.
- Enter the input frequency of the input signal in the box that says "ADC Input Target Frequency" (5 MHz used in this example).
- Click "Capture" .



- The analog input signal power may need to be adjusted to reach -1 dBFS.

4.2 Real Decimation Mode

The following software configuration steps will program the ADC366xEVM in 16x Real Decimation mode.

4.2.1 ADC35XX GUI: Real Decimation Mode Configuration (2W, 16bit)

This procedure applies specifically to the ADC3663EVM, but can be applied to other sampling rates and bit resolutions. See Table 4-2 for examples for clock rates in Real Decimation mode.

Table 4-2. 16-bit, Real Decimation Sample rate and DCLKIN examples

Interface Mode	DCLKIN multiplier	Example Sample Clock	Real Decimation Factor	Required DCLKIN Frequency
2 Wire	4	65 MSPS	2	130 MHz
1 Wire	8	32 MSPS	8	32 MHz
1/2 Wire	16	10 MSPS	32	5 MHz

For this 16x Real Decimation example, apply a 65 MHz signal to J9 (sample clock) and a 16.25 MHz signal to J7 (DCLKIN).

> External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

Apply a 1 MHz signal to J2 (ensure bandpass filter is used to reduce harmonics and noise of signal generator).

After launching the ADC35xx GUI perform the following steps:

- Under Resolution, select 16 bit.
- Under DDC, Select Real.
- For Decimation Factor, select 16.
- To calculate the DCLKIN frequency, enter "65" in the Fs(MHz) field, and click calculate. This is informational only.
- Ensure that "CDC Enable" is red (disabled).
- Click "Configure"

4.2.2 HSDC Pro: Real Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro
- Select the TSW1400 and click OK
- Click OK for the no firmware loaded prompt.
- Select “ADC3663_2W_16bit” to load firmware, and click Yes.

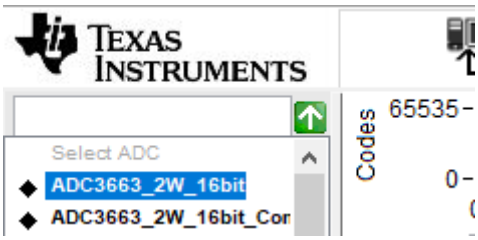


Figure 4-4. Real Decimation HSDC Pro INI File (2W, 16bit)

- Click on the cog next to "ADC Output Data Rate".
- In the new dialogue box, enter "65M" in "ADC Sampling Rate"
- Enter "1M" in "ADC Input Frequency"
- Enter "16" in "Decimation"
- Click "OK"
- Click "Capture"

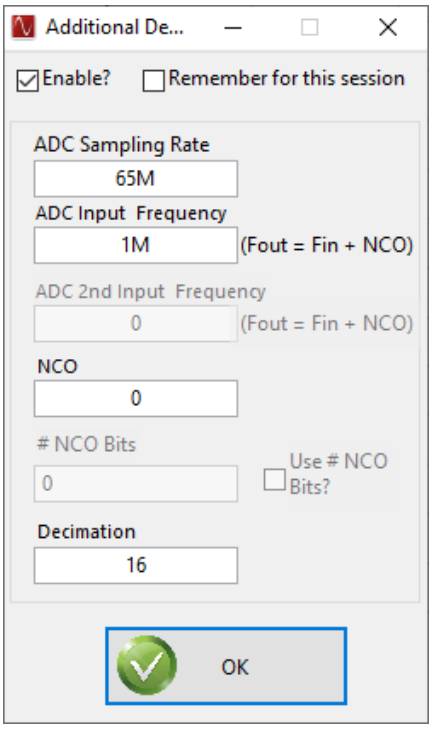


Figure 4-5. HSDC Pro Cog Wheel (Real Decimation)

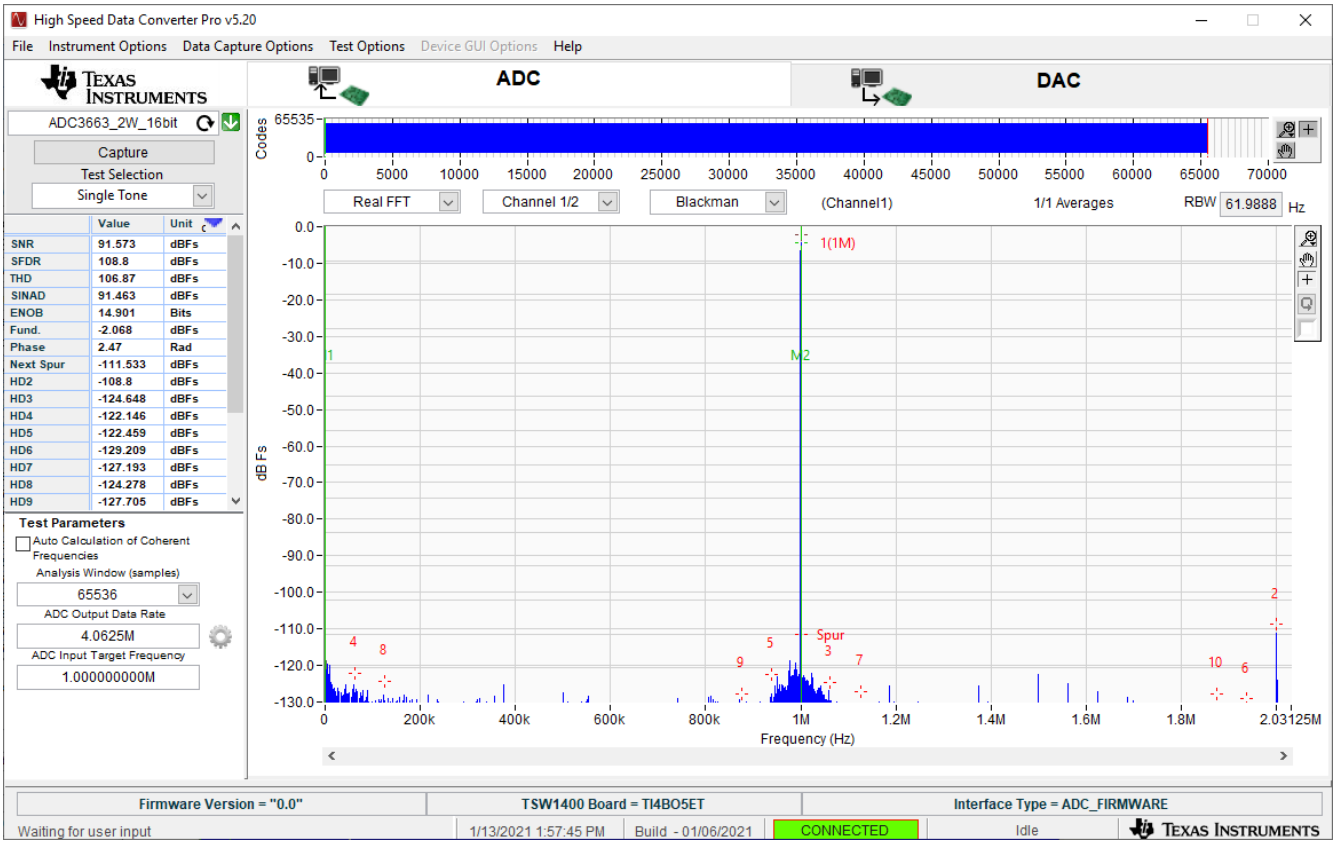


Figure 4-6. HSDC Pro 16x Real Decimation FFT (2W, 16 bit)

4.3 Complex Decimation Mode

The following software configuration steps will program the ADC366xEVM in Complex Decimation mode (32x) with a 10 MHz analog input and 9.9 MHz NCO.

4.3.1 ADC35XX GUI: Complex Decimation Configuration

This procedure applies specifically to the ADC3663EVM, but can be applied to other sampling rates and bit resolutions.

Table 4-3. 16-bit, Complex Decimation, Sample rate and DCLKIN examples

Interface Mode	DCLKIN multiplier (Serialization Factor)	Example Sample Clock	Complex Decimation Factor	Required DCLKIN Frequency
2 Wire	4	65 MSPS	2	260 MHz
1 Wire	8	32 MSPS	8	64 MHz
1/2 Wire	16	10 MSPS	32	10 MHz

For this 32x Complex Decimation example, apply a 65 MHz signal to J9 (sample clock) and a 16.25 MHZ signal to J7 (DCLKIN).

> External ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled. If using the onboard clocking option, the sampling clock and DCLKIN are frequency locked.

Apply a 10 MHz signal to J2 (ensure bandpass filter is used to reduce harmonics and noise of signal generator). An NCO of 9.9 MHz are used to shift the 10 MHz input signal to -100 kHz.

After launching the ADC35xxEVM GUI perform the following steps:

- Under "Resolution", select "16 bit".
- Under "Mode", select "2 Wire"
- Under "DDC", Select "Complex".
- For "Decimation Factor", select "32".
- Ensure that "CDC Enable" is red (disabled).
- To calculate the DCLKIN frequency, enter "65" in the Fs(MHz) field, and click calculate. This is informational only.
- Under "FNCO A (MHz)" and "FNCO B (MHz)", enter "9.9" in the field. This field then calculates to the nearest valid NCO value, and auto-calculates the correct register values in the field next to it.
- Click "Configure".

4.3.2 HSDC PRO: Complex Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro.
- Select the TSW1400 and click "OK".
- Click OK for the "no firmware loaded"prompt.
- Select “ADC3663_2W_16bit_Complex” to load firmware, and click Yes.

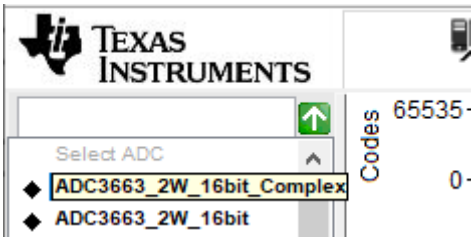


Figure 4-7. Complex Decimation HSDC Pro INI file

- Click on the cog next to “ADC Output Data Rate”.
- In the new dialogue box, check the "Enable?" box.
- Under “ADC Sampling Rate”, enter "65M"
- Under “ADC Input Frequency”, enter "10M"
- Under "NCO", enter "9.9M"
- Under “Decimation”, enter "32".
- Click "OK".

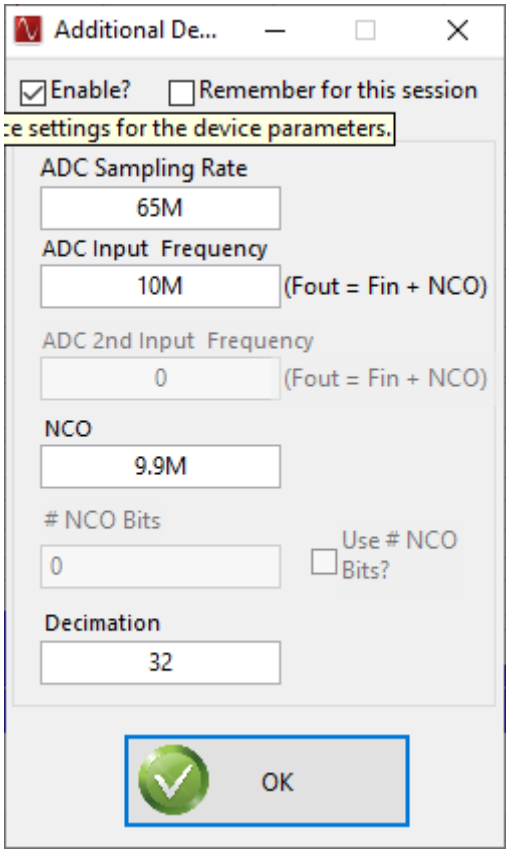


Figure 4-8. HSDC Pro Cog Parameters: 32x Complex Decimation Mode

- Select "Complex FFT"
- Press "Capture"

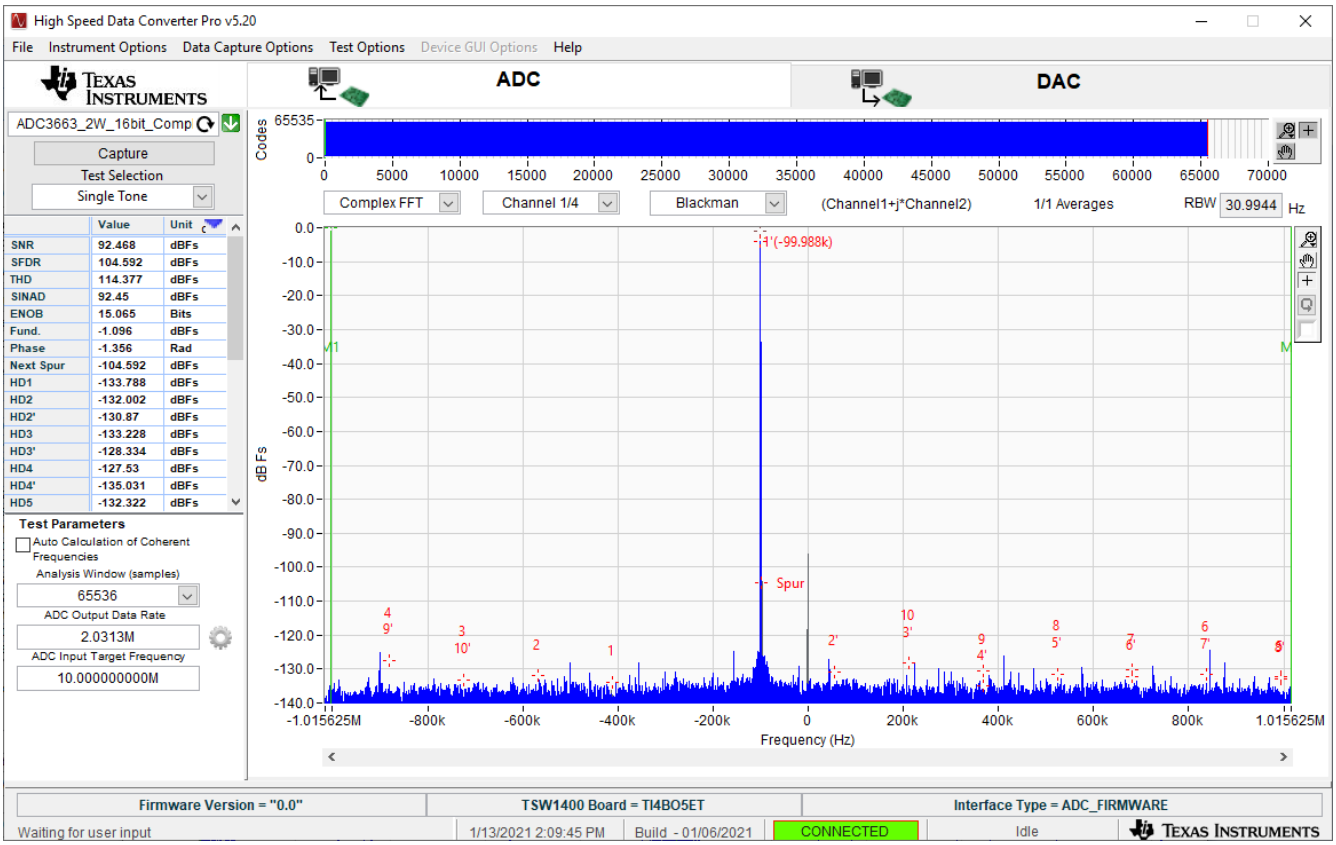


Figure 4-9. HSDC Pro 32x Complex Decimation (2W, 16 bit)

5 Onboard Clocking Hardware Setup

The onboard CDC is useful for general evaluation and relieves the user requirment of needing additional signal generators. However, the clock spurs and jitter of the CDCE6214 (due to 4.5 sample clock/DCLKIN relationship) begin to effect the optimal ADC AC performance.

Looking at the image below, we can see that SNR/SFDR performance does degrade by several dBFS for the ADC3663EVM, however, using the onboard CDCE6214 relieves the user of providing the external sample clock and DCLKIN, and may be useful for verifying the SLVDS interface to an FPGA development kit. In practice, an appropriate filter may be used to reduce the effects of clock spurs and broad band phase noise in order to acheive full ADC performance.

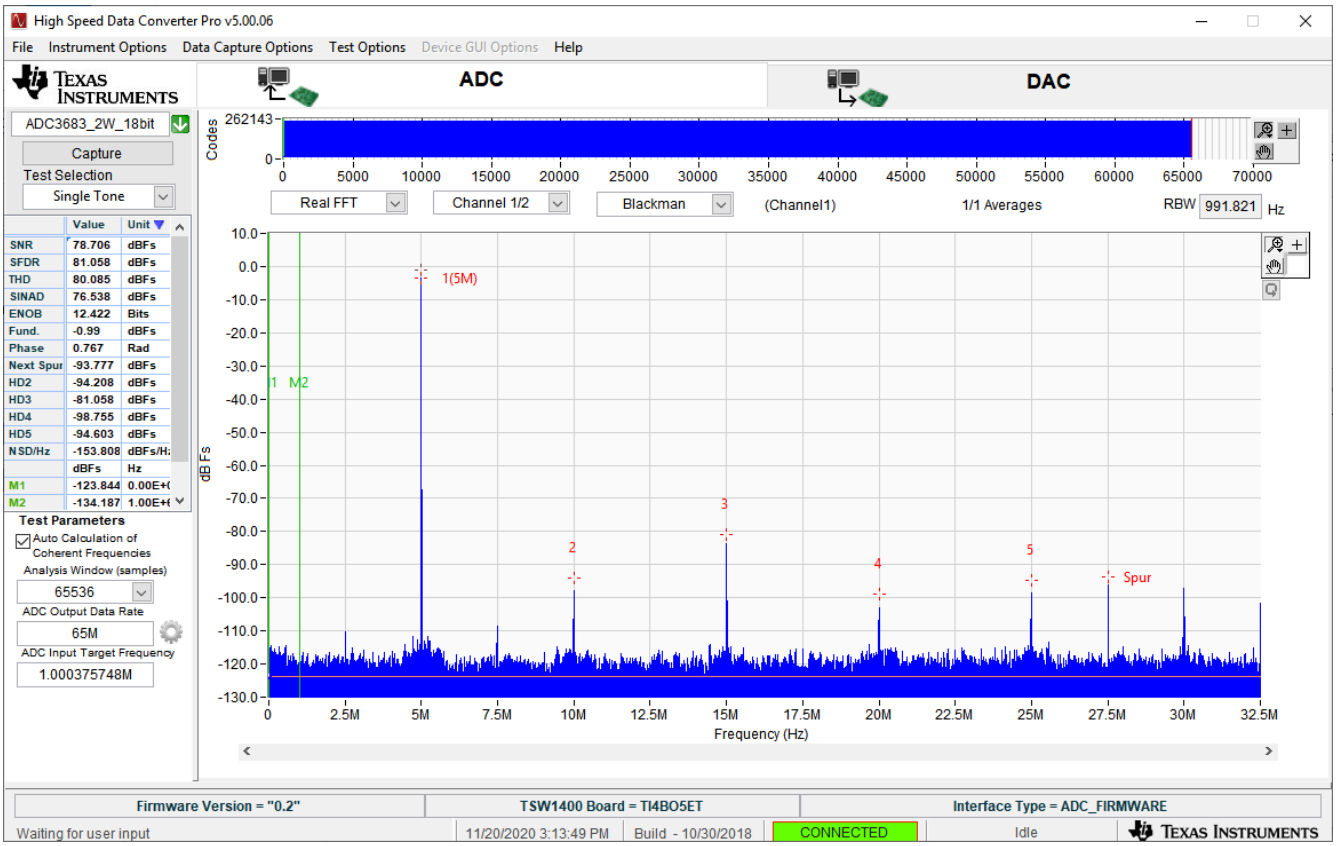


Figure 5-1. ADC3663EVM onboard clocking (CDCE6214: 65 MHz sample clock, 260 MHz DCLKIN)

The following section shows how to configure and program the ADC366xEVM for onboard clock operation for Real Decimation Mode. Onboard clocking can be used for Bypass and Complex Decimation modes as well, and uses similar procedures that have been outlined in this document.

When using onboard clocking, there are several different sampling rates to choose from (65MSPS, 25 MSPS and 10 MSPS) in Bypass and Decimation modes. The ADC35XX GUI does not support configuring the CDCE6214 to frequencies outside of these preset selections at this time.

5.1 Onboard Clocking: Hardware Modfications

The following hardware modifications must be made in order to operate the ADC36xxEVM using an onboard sample and DCLKIN clocks.

Onboard Sample Clock Modification:

- DNI R46, R47
- Install R41, R51 (0-Ω resistor)

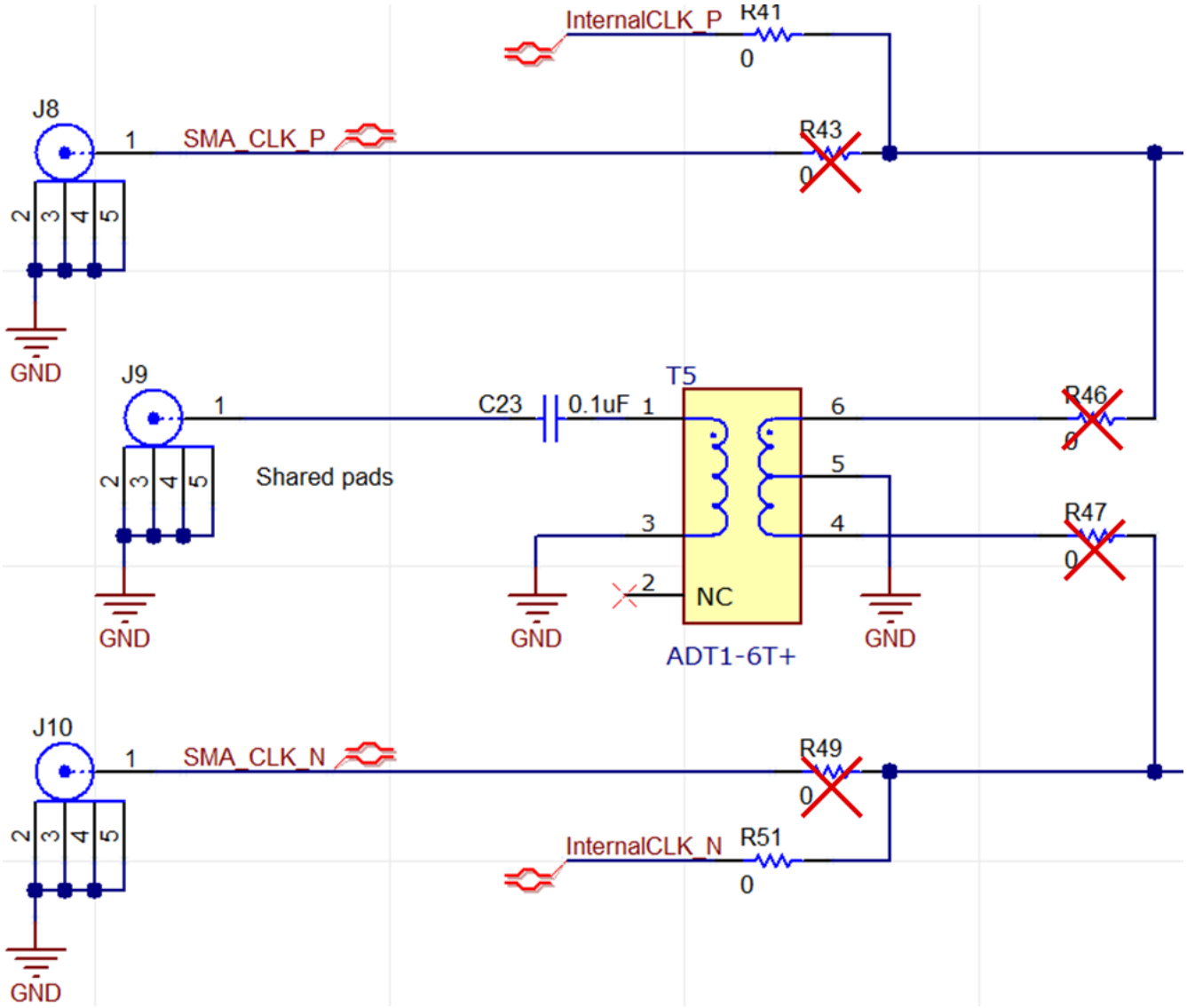


Figure 5-2. ADC36xxEVM Onboard Sample clock modifications

Onboard DCLKIN Modification:

- Install R60 and R62 (0-Ω resistor)
- DNI R35 and R36

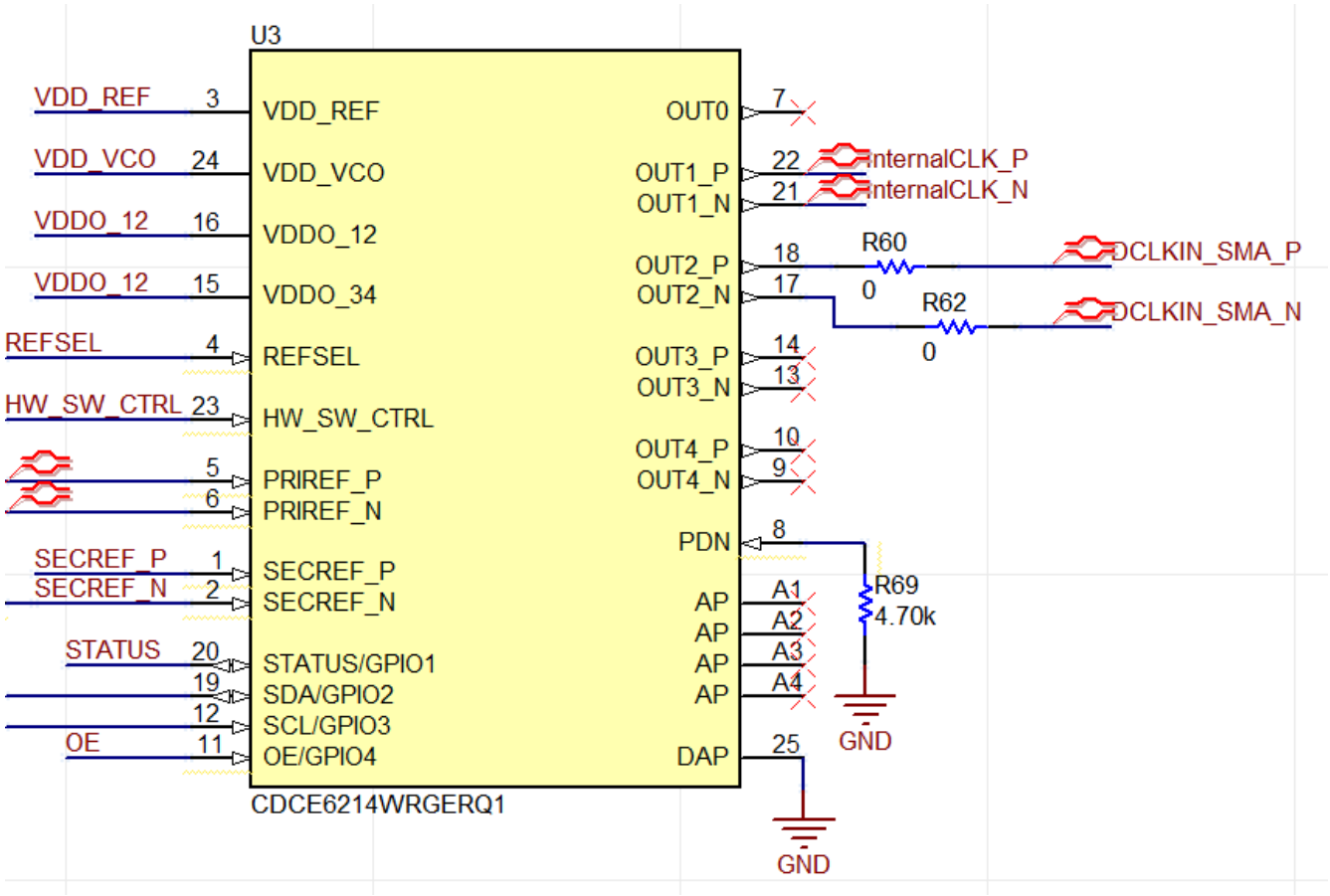


Figure 5-3. ADC36xxEVM Onboard DCLKIN modifications

5.2 Onboard Clock: ADC35XX GUI Real Decimation Mode

Ensure that the steps in Onboard Clocking: Hardware Modifications have been performed before proceeding. To program the ADC36xxEVM with Onboard clocking, follow the steps written in the previous section titled "ADC35xx GUI: Real Decimation Configuration". The only differences that must be observed in the GUI is the "CDC Clock Enable" button must be enabled (Green), and the "Configure CDC" button must be clicked.

The PLL_LOCK LED (D1) also illuminates to ensure CDCE6214 has been configured correctly.

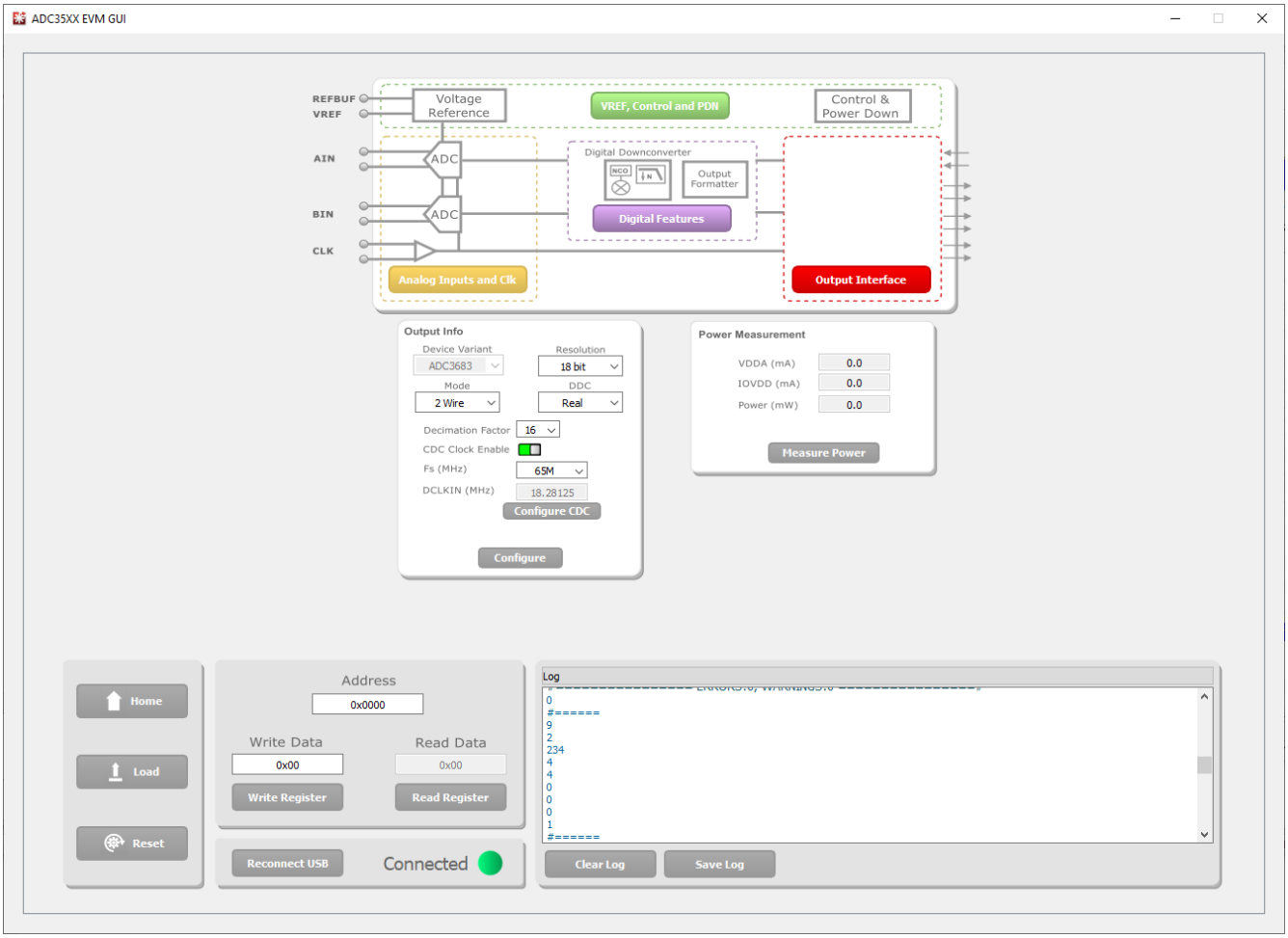


Figure 5-4. AD35xx EVM GUI: Onboard Clock 16x Real Decimation

6 FDA Configuration

By default, the analog input is configured to use the balun input (AD1T-6T+) for both analog input channels, but can be modified to utilize the onboard FDA (THS4541).

In terms of performance as compared with the balun input, SFDR is improves, but SNR performance degrades by a few dBFS.

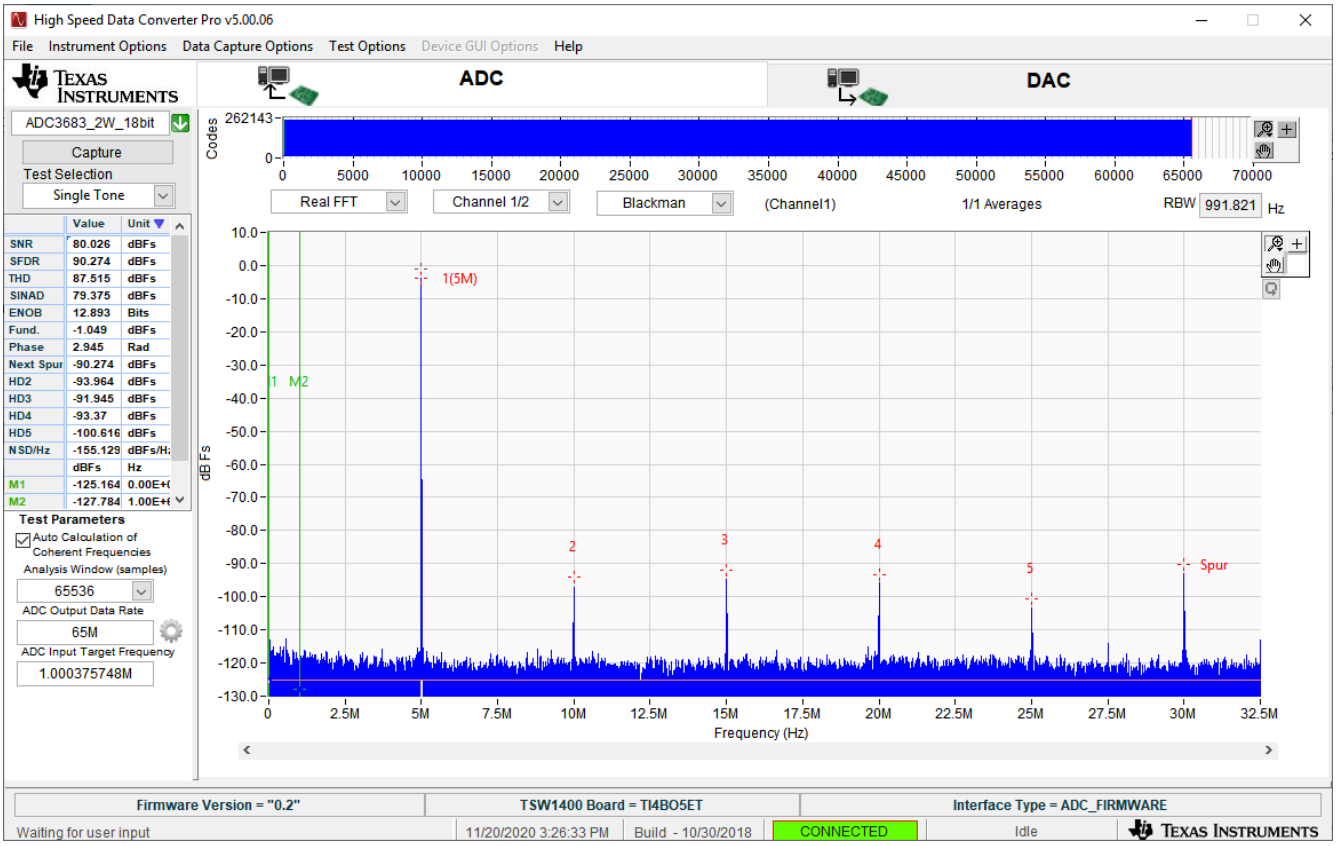


Figure 6-1. ADC3663EVM FDA Analog input (External Clocks, 65 MSPS)

This procedure shows how to configure the FDA single-ended to diferential conversion for CHA. The same procedure can be performed for CHB (with the respective component designators).

The edge launched SMA connector J1 receives the single-ended analog input signal. R1 can be replaced with a capacitor for AC coupling to FDA.

Modify the following components to complete path to FDA (located on top of EVM).

- Install: R1, R2, R14 (o ohm)

- Remove (DNI): C3, C6, R7, R8

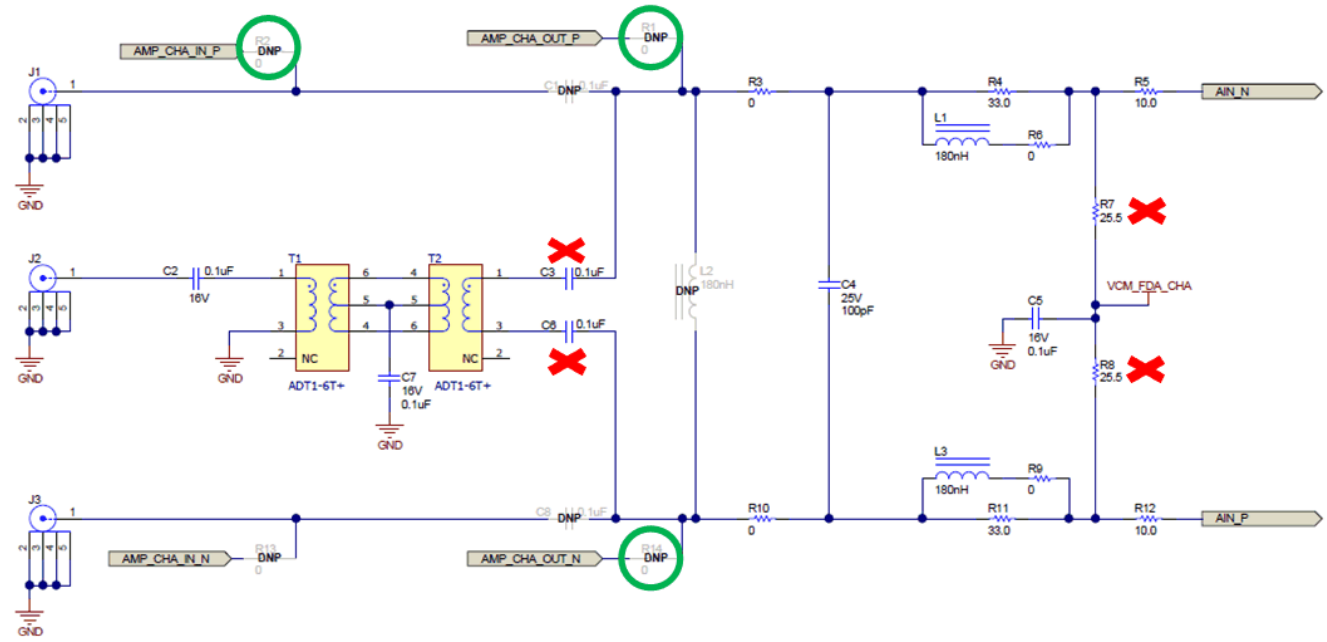


Figure 6-2. CHA FDA Component modification

The FDA is setup with a gain of 2.5, and can be adjusted (R78, R84, R86 and R94) as the application requires. There is a 20 MHz LPF on the output of the FDA, and these components (C52, L11,L12 and C53) can be adjusted as the application requires. The termination resistors (R80, R81, R89 and R90) can be adjusted according to the source impedance.

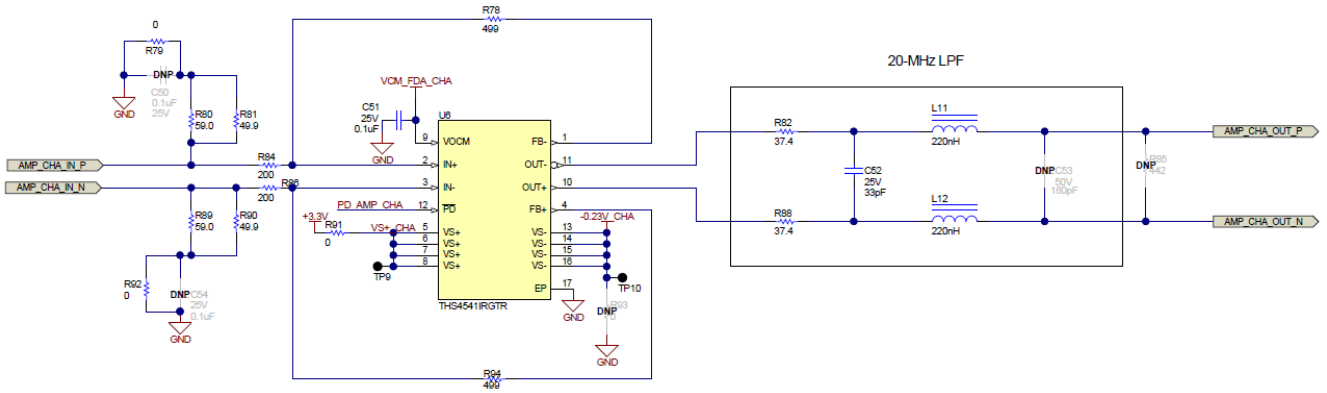


Figure 6-3. FDA schematic

For further information on the THS4541 FDA, please refer to the THS4541 datasheet.

7 ADC36xxEVM Power Monitor

The ADC366xEVM is equipped with on-board current shunt monitors that are able to measure the current consumption on the +1.8 VDC rails (AVDD and IOVDD). The user has the ability to read the ADC366xEVM power consumption on the front page of the ADC35XX EVM GUI. Click the "Measure Power" button to refresh the current values. This feature is useful for determining what mode/sampling speed offers the best power consumption for your application needs.

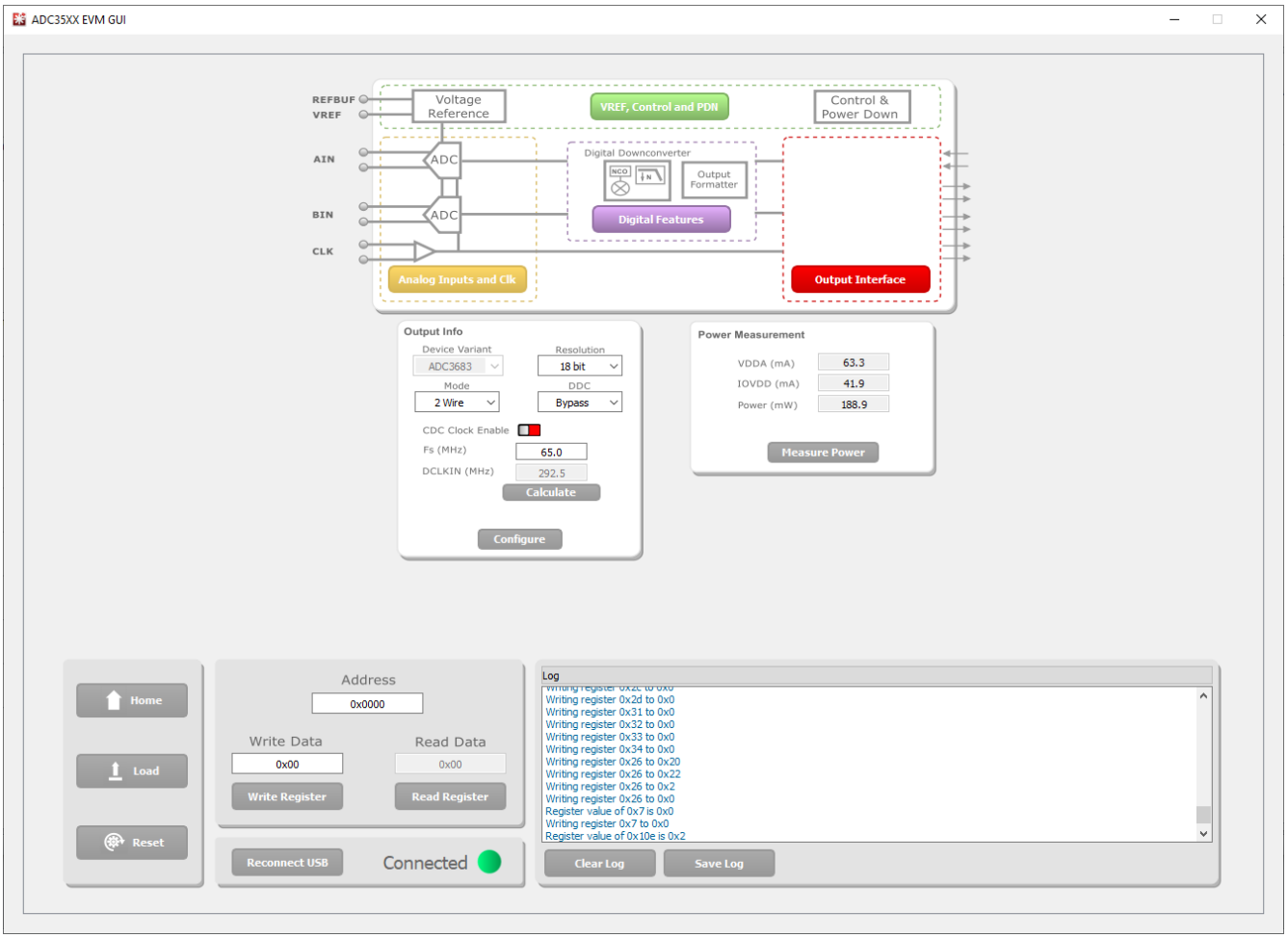


Figure 7-1. ADC36xxEVM Power Meter

8 Test Pattern

Test patterns are often used to help verify the correct reciept of digital data at the microcontroller or FPGA. A ramp pattern can be enabled by following these steps:

- Click the yellow button "Analog Inputs and Clk"
- Next to "Test Pattern CHA", click the drop down menu, and select "RAMP CUSTOM". This can be done for "Test Pattern CHB" as well.
- In the field next to "Custom Pattern",
  - For 16 bit ramp mode (ADC3663EVM, ADC3662EVM), "4" must be entered in the "Custom Pattern" field.
- The digital ramp pattern is now enabled on the ADC. The output of the ADC is now an 16 bit, incrementing ramp pattern.

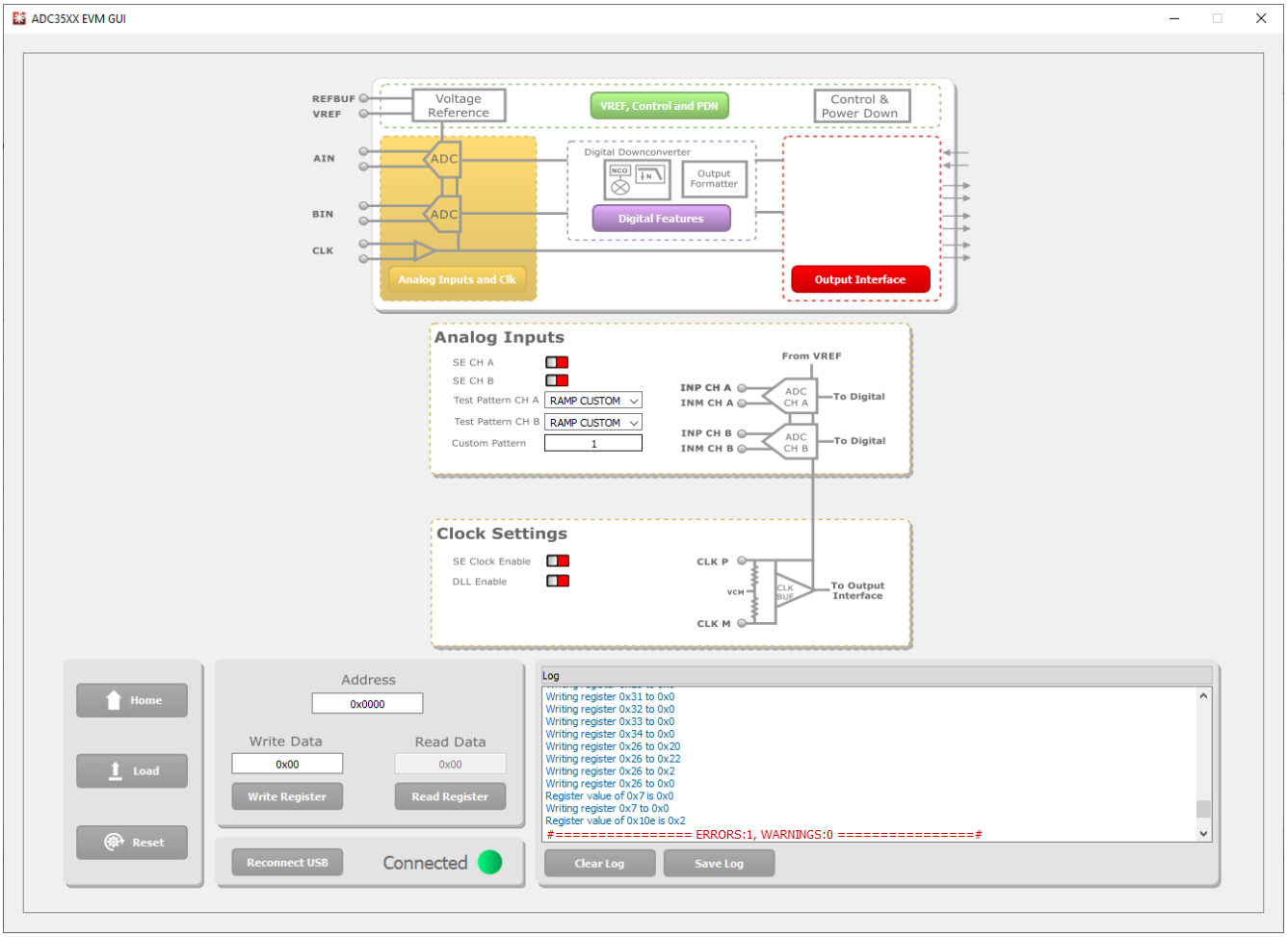


Figure 8-1. ADC36xxEVM 16-bit Ramp Pattern

- In HSDC Pro, the ramp pattern can now be seen when data is captured. These same steps apply to any data output mode (Bypass, Real Decimation and Complex Decimation).

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