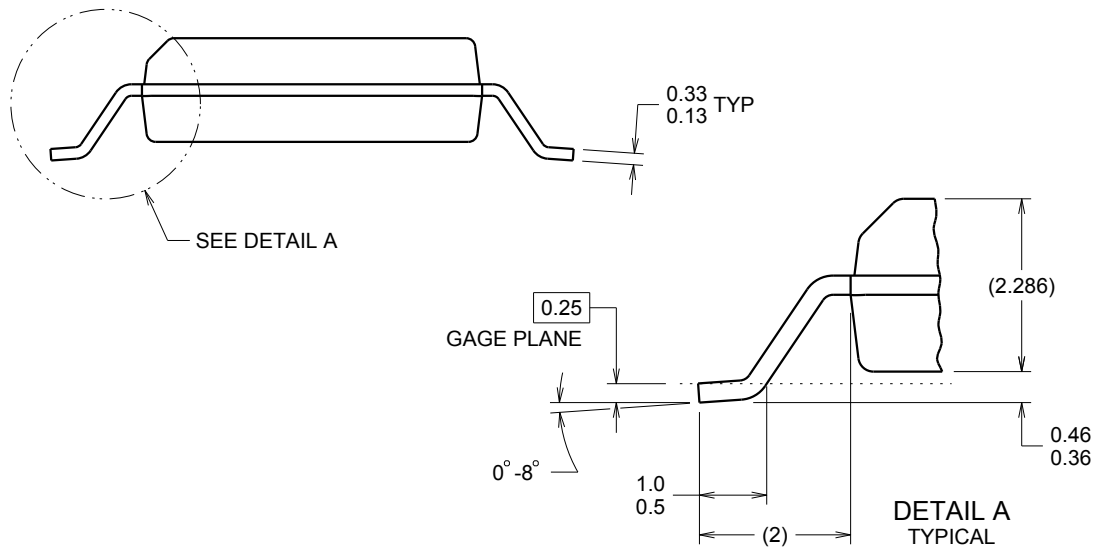
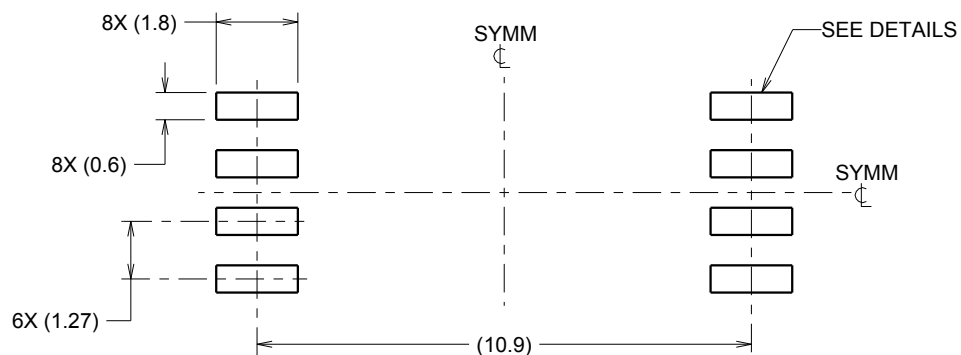


SOIC - 2.8 mm max height

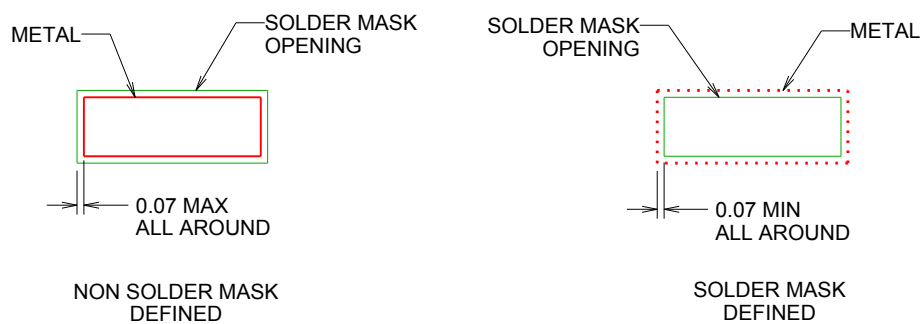
PIN 1 ID AREA  
 11.5 ± 0.25 TYP  
 5.95  
 5.75  
 NOTE 3  
 4  
 8  
 6X 1.27  
 2X 3.81  
 5  
 8X 0.51 / 0.31  
 7.6  
 7.4  
 NOTE 4  
 A  
 B  
 SEATING PLANE  
 0.1 C  
 2.8 MAX  
 C  
 A  
 B



1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X

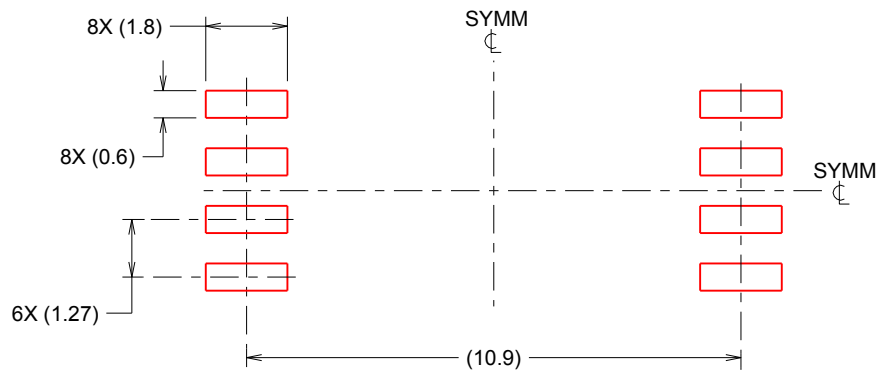


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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