Application Report

Power Management Optimizations – Low Cost LC Filter Solution

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ABSTRACT

This application report discusses the Power supply ripple and noise specifications, reference solutions and introduces its trade off, an LC filter-based low cost solution.

Table of Contents

Trademarks.....1
1 Introduction.....2
2 Power Supply Ripple and Noise Specifications.....2
3 Reference Solution.....4
4 Low Cost LC Filter Solution.....6
4.1 LDO vs LC Filter Scheme Comparison.....6
4.2 System Tests.....9
5 Summary.....19

List of Figures

Figure 3-1. Power Management Scheme With LDOs.....4
Figure 3-2. Reference Schematic.....5
Figure 4-1. Power Management Scheme With LC filter.....6
Figure 4-2. Capture With LDO Scheme, RX Gain-48dB.....10
Figure 4-3. Capture With LDO Scheme, RX Gain-30dB.....11
Figure 4-4. Capture With LC Filter Scheme, RX Gain-48dB.....12
Figure 4-5. Capture With LC Filter Scheme, RX Gain-30dB.....13
Figure 4-6. LDO Scheme –Spur Level.....15
Figure 4-7. LDO Scheme - Noise Floor With Tx –OFF.....16
Figure 4-8. LC Filter Scheme – Spur Level.....17
Figure 4-9. LC Filter Scheme - Noise Floor With Tx –OFF.....18

List of Tables

Table 2-1. XWR1xx Supply Ripple (µVrms).....2
Table 2-2. XWR1xx Noise Spectral Density (µVrms/RtHz).....2
Table 2-3. XWR1xxx Supply Ripple (µVrms).....3
Table 2-4. XWR1xxx Noise Spectral Density (µVrms/RtHz).....3
Table 4-1. Recommended Ferrite Bead Components.....6
Table 4-2. Sensor Configuration.....6
Table 4-3. Spur/Noise Level Measurements With Tx to Rx Waveguide Loopback.....7
Table 4-4. Voltage Transient Behavior.....8
Table 4-5. Sensor Configuration.....9
Table 4-6. SNR Comparison Between LDO and LC Filter Scheme for RX Gain = 30 and 48.....14

Trademarks

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1 Introduction

XWR1xx is a family of Texas Instrument's mmWave Radar sensor devices with RFCMOS technology. These devices are intended for the automotive and industrial applications. The devices are powered by four voltage rails, namely 3.3 V, 1.2 V, 1.8 V and 1.0 V.

Contents of this document apply to the following mmWave devices:

- xWR1xxx/xWR2xxx
- xWR6xxx

2 Power Supply Ripple and Noise Specifications

Out of the four Power supply rails mentioned above, the 1.0 V and the 1.8 V supplies are sensitive to the supply ripple and noise because these supplies feed the critical blocks in the device like PLL, baseband ADC, synthesizer, and so forth. For more details on the power supply rail and the logic that it feeds in the device, see the device-specific data sheet. Table 2-1 and Table 2-2 provide the ripple and noise spec for 1.0 V

Table 2-1. XWR1xx Supply Ripple (μVrms)

Sl. Number	Frequency (KHz)	XWR1xx Supply Ripple (μVrms)
1	17.1875	
2	34.375	
3	68.75	
4	137.5	
5	275	
6	550	
7	1100	
8	2200	
9	4400	35.48133892
10	6600	

Table 2-2. XWR1xx Noise Spectral Density (μVrms/RtHz)

Sl. Number	Frequency (KHz)	XWR1xx Noise Spectral Density (μVrms/RtHz)
1	17.1875	0.01
2	34.375	0.01
3	68.75	0.01
4	137.5	0.015
5	275	0.02
6	550	0.02
7	1100	0.009
8	2200	0.002
9	4400	0.05
10	6600	0.002

Table 2-3 and Table 2-4 provide the ripple and noise spec for 1.8 V.

Table 2-3. XWR1xxx Supply Ripple (μVrms)

Sl Number	Frequency (KHz)	XWR1xxx Supply Ripple (μVrms)
1	17.1875	
2	34.375	
3	68.75	
4	137.5	
5	275	
6	550	
7	1100	
8	2200	
9	4400	35.48133892
10	6600	

Table 2-4. XWR1xxx Noise Spectral Density (μVrms/RtHz)

Sl Number	Frequency (KHz)	XWR1xxx Noise Spectral Density (μVrms/RtHz)
1	17.1875	0.08
2	34.375	0.07
3	68.75	0.07
4	137.5	0.07
5	275	0.07
6	550	0.07
7	1100	0.07
8	2200	0.07
9	4400	0.07
10	6600	0.07

3 Reference Solution

TI recommends the reference solution with the PMIC and the LDOs as shown in Figure 3-1, which is also incorporated in the XWR1xxx EVMs. The reference solution meets these specifications. The XWR1xx device would expect 1.0 V to be fed on the H5, G5, J5, D2 and C2 pins. The PMIC needs to be reconfigured for the Buck outputs shown in Figure 3-1 using the Inter-Integrated Circuit (I2C) interface from the host. Initially during the power up, the buck outputs would be 3.3 V, 1.2 V, 1.3 V and 2.1 V. Using I2C interface, the buck outputs needs to be reconfigured as shown in Figure 3-1 before the nRESET of XWR1xx is released.

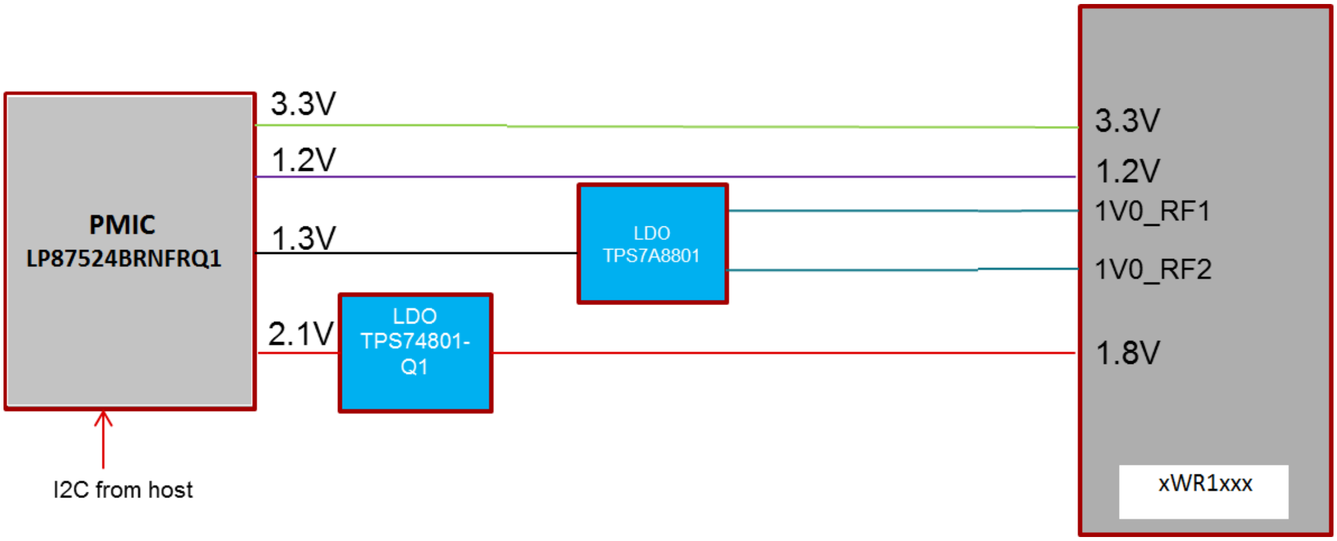

Figure 3-1. Power Management Scheme With LDOs

The above reference solution consists of the LP87524BRNFRQ1 PMIC with the switching frequency localized at 4 MHz, so that the fundamental and the harmonics could easily be filtered out during RADAR data post processing. The reference schematic is shown in Figure 3-2.

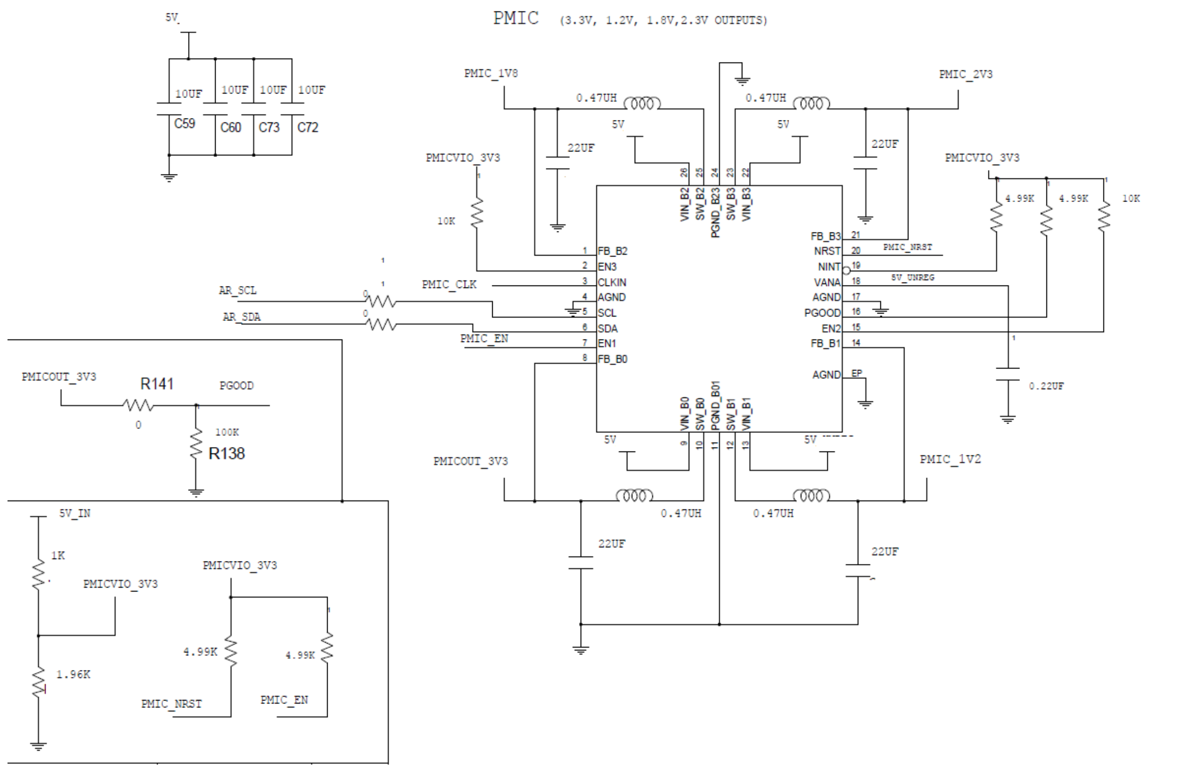

Figure 3-2. Reference Schematic

4 Low Cost LC Filter Solution

For the cost sensitive use cases, a low cost LC filter (Ferrite bead + Device Decoupling capacitor) based solution could be used, which would effectively replace the LDOs on the 1.8 V and 1.0 V rails. This approach would have performance and the system level trade-off.

Figure 4-1 shows the Power management scheme.

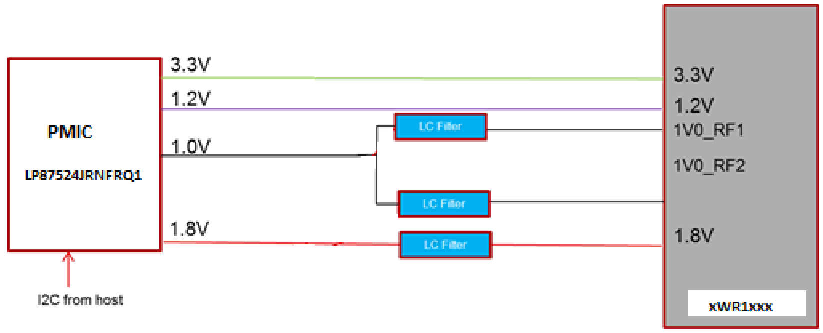

Figure 4-1. Power Management Scheme With LC filter

Note

The capacitors shown above in the LC filter are the device decoupling capacitors.

The recommended Ferrite bead components are shown in Table 4-1.

Table 4-1. Recommended Ferrite Bead Components

LC Filter	Inductor Value (µH)	DC Resistance (mΩ)	Impedance @ 100 MHz (Ω)	Size (inches)	Pole Frequencies w.r.t. 1V Rail Decaps/1.8V Rail Decaps (KHz)	DC Current (A)	Theoretical Rejection Offered by the Filter (dB)	Manufacturer Part Number
Ferrite Bead	0.1909	25	120	0603	113.9	3	64	BLM18KG121TH1

4.1 LDO vs LC Filter Scheme Comparison

4.1.1 Waveguide Loopback Tests

Two consecutive chirps have been analyzed with 10 µSec and 100 µSec of idle time and the below chirp configuration.

Table 4-2 provides the sensor configuration for the below tests.

Table 4-2. Sensor Configuration

Parameter	Value
Start frequency (GHz)	77
Frequency slope (MHz)	35.003
Tx start time (µsec)	0
ADC start time (µsec)	5
ADC samples	1024
Sample rate (Kbps)	10000
Ramp end time (µsec)	110
Rx gain	33

4.1.2 Spur/Noise Floor Level

The measurements shown in Table 4-3 are done with TX to RX loopback with Tx Back-0ff=0 and Complex Rx gain=33dB.

Table 4-3. Spur/Noise Level Measurements With Tx to Rx Waveguide Loopback

PM Scheme	Idle Channel Noise Floor (Rx-alone) at the ADC Output (dBFs/Hz)	Amplitude Level of PMIC Ripple Frequency Spur (4.05M-4.17M) Seen at the ADC Output (dBFs)	(Tx+Rx) SNR dBc/Hz	Amplitude Level of PMIC Ripple Frequency Spur (4.05M-4.17M) Seen at the ADC Output (dBFs)
	Additive (Rx1 - alone)		Loop back (Tx2-Rx1)	
LDO Scheme	-138.80	Not seen	-118.74	Not seen (less than noise floor)
LC Filter Scheme	-138.27	Not seen	-120.6	-104

4.1.3 Voltage Transient Behavior

Table 4-4. Voltage Transient Behavior

PM Scheme	XWR1xx Supply Rail	Voltage Setting Parameters on Chirp 1				Voltage Setting Parameters on Chirp 2				Steady State DC Value (mV) at the Input of XWR1642 Rail	Calculated IR Drop (mV) (difference between steady state DC and actual input voltage)
		Undershoot Voltage (mV)		Undershoot Period (µs)		Undershoot Voltage (mV)		Undershoot Period (µs)			
	Idle time (µs)	10	100	10	100	10	100	10	100	10	10/100
LDO	RF1_1V0	55.6	79.0	4.4	6.7	67.0	214.5	5.0	10.0	982.0	17
	RF2_1V0	33.9	34.6	7.2	11.1	42.0	208.3	5.6	12.2	982.0	17
	CLK_1V8	20.0	20.0	1.6	2.5	24.0	20.0	2.4	2.6	1760.0	35
LC Filter	RF1_1V0	59.0	51.2	6.2	6.1	59.0	51.2	4.4	5.0	949.5	49.5
	RF2_1V0	44.1	47.0	5.9	5.5	44.1	41.1	4.3	5.7	944.6	54.4
	CLK_1V8	30.5	17.9	3.1	4.0	30.5	17.9	3.5	3.5	1737.0	58

4.2 System Tests

4.2.1 Sensor Configuration

Table 4-5. Sensor Configuration

Parameter	Value	Comments
Start frequency (GHz)	77	
Frequency slope (MHz)	68.65	
Tx start time (uSec)	0	
ADC start time (uSec)	5.99	
Idle time (uSec)	12	Inter Chirp power saving enabled for idle time+Tx start time >10usec
ADC samples	256	
Sample rate (Kbps)	5000	
Ramp end time	58.22	
Rx gain	48	

4.2.2 System Test With Static Object

The test involves detecting an object at approximately 1m from the sensor. Both captures with LDO and LC filter schemes are shown below. No major degradation in the signal power is detected as shown below.

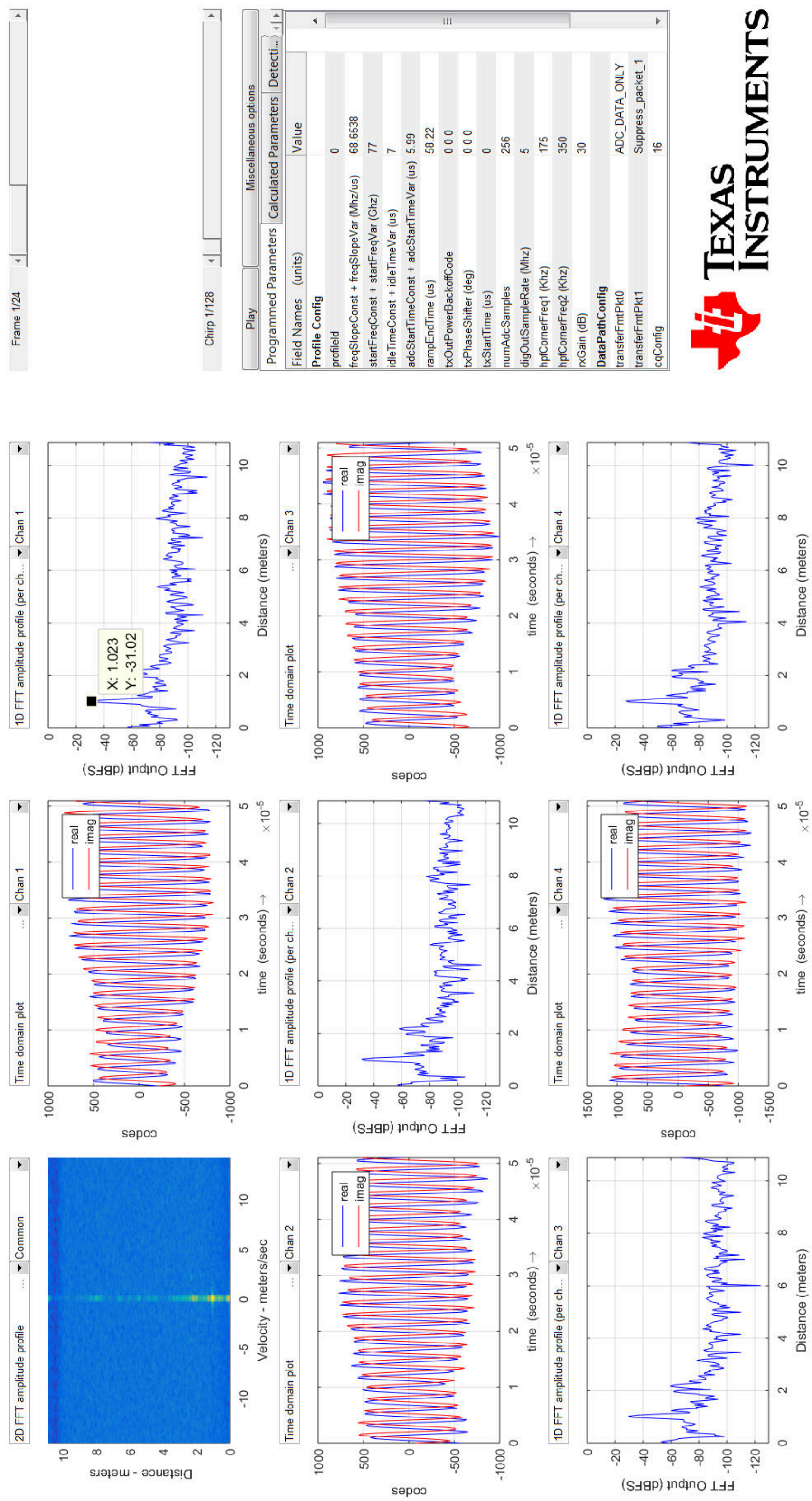

Figure 4-2. Capture With LDO Scheme, RX Gain-48dB

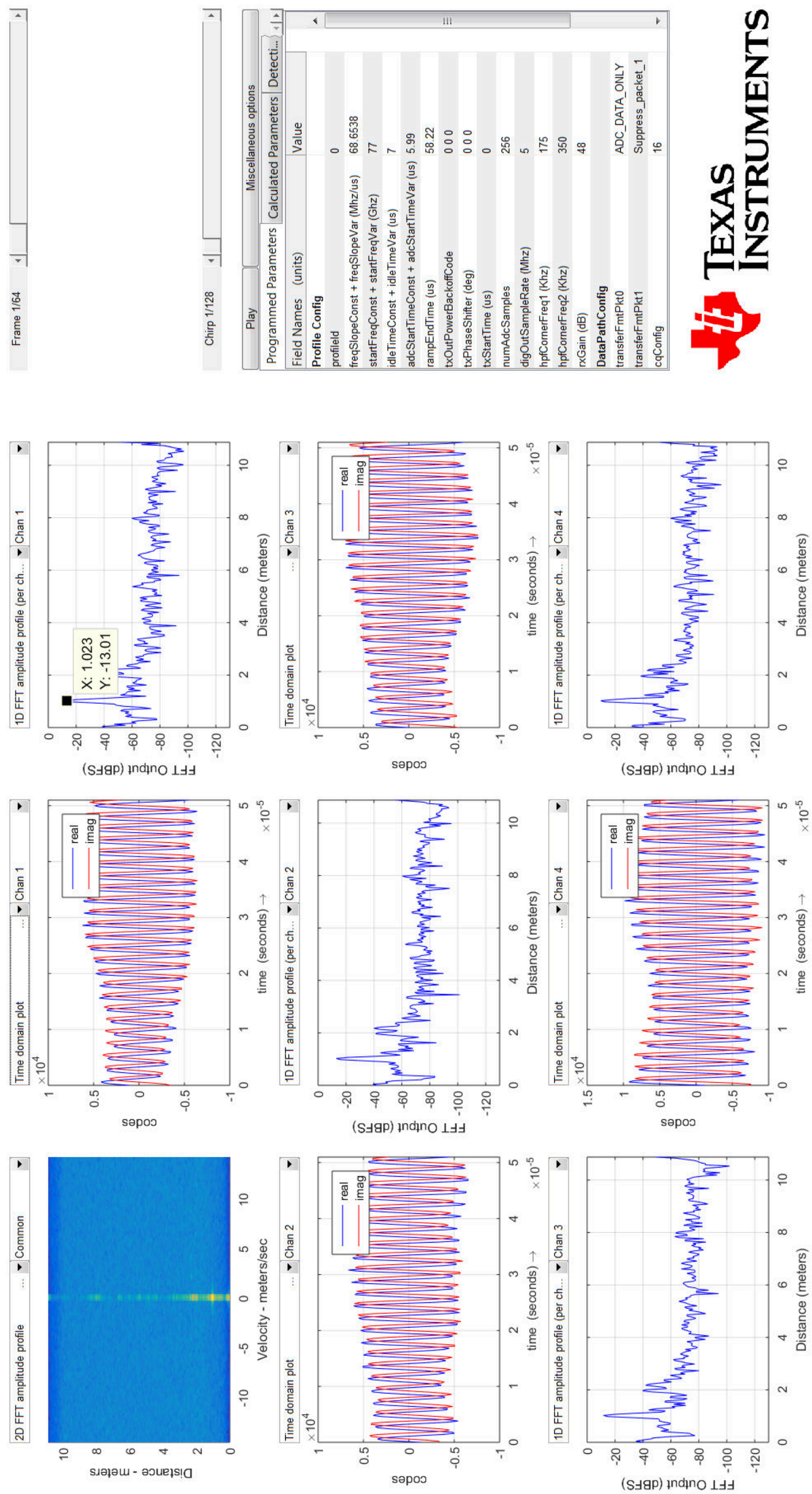

Figure 4-3. Capture With LDO Scheme, RX Gain-30dB

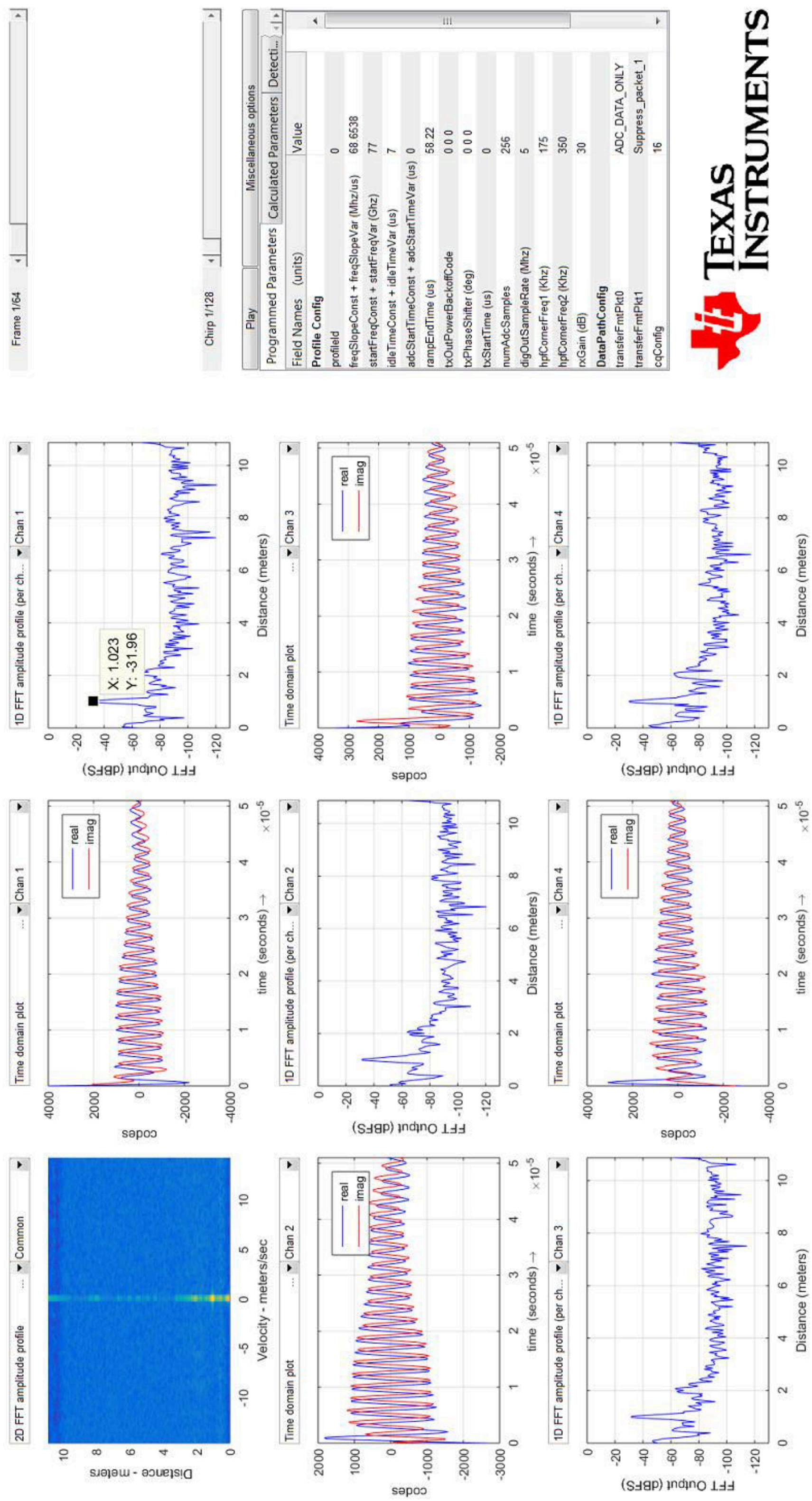

Figure 4-4. Capture With LC Filter Scheme, RX Gain-48dB

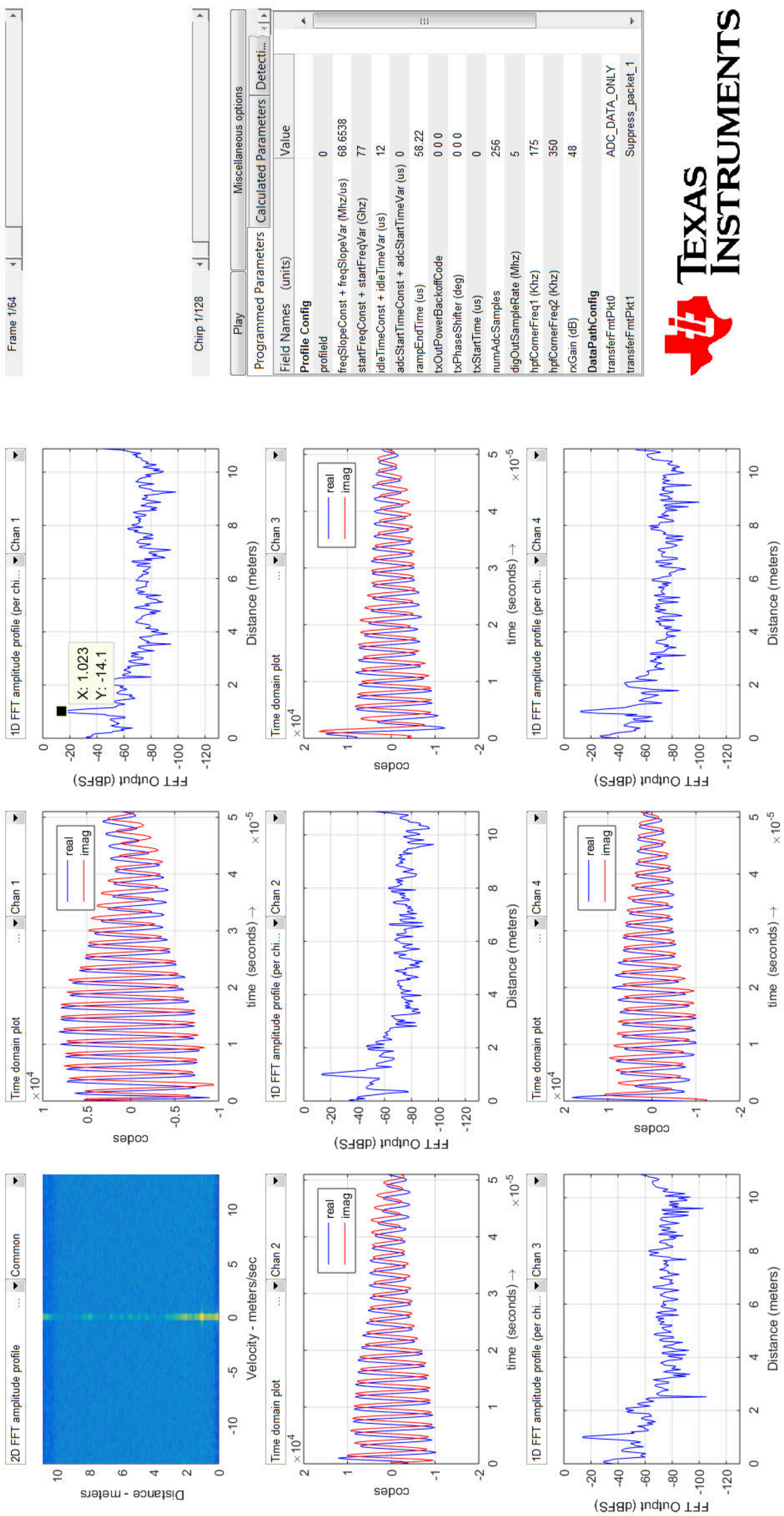

Figure 4-5. Capture With LC Filter Scheme, RX Gain-30dB

Table 4-6. SNR Comparison Between LDO and LC Filter Scheme for RX Gain = 30 and 48

PM Scheme	RX Gain(dB)	SNR(dB)-RBW 152.6Hz
LDO	30	81.93
	48	83.9
LC Filter	30	79.6
	48	81.9

4.2.3 Spur/Noise Floor Level

For Spur level measurements, a continuous tone at 77 GHz is transmitted and the received signal is analyzed with 524288 samples for the presence of the PMIC switching frequency spur at ~4 MHz. The Rx gain is set at 48dB with an observation that PMIC spur level tracks the Rx gain.

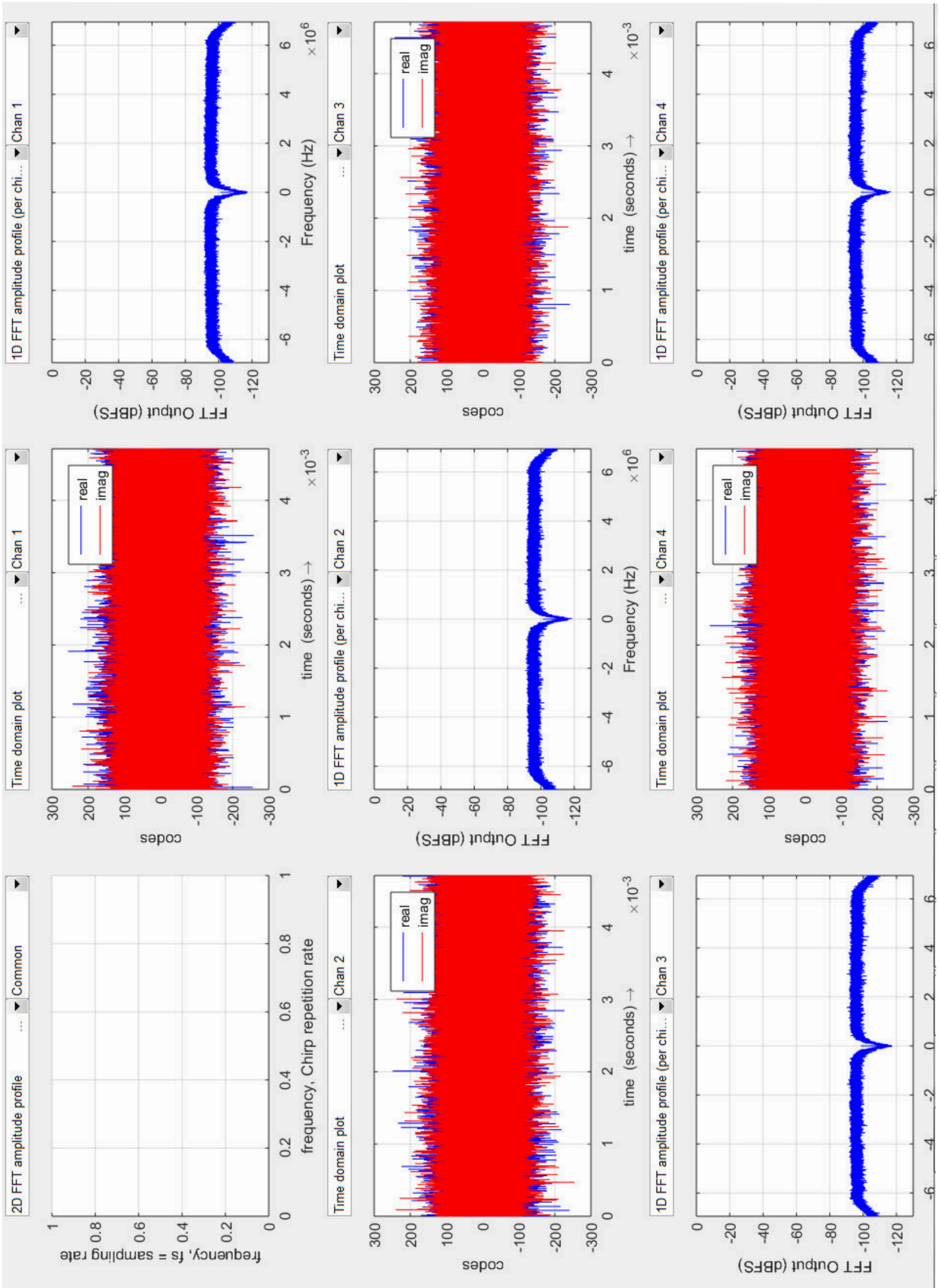

Figure 4-6. LDO Scheme –Spur Level

Note

No PMIC switching Frequency (approximately 4 MHz) Spur seen.

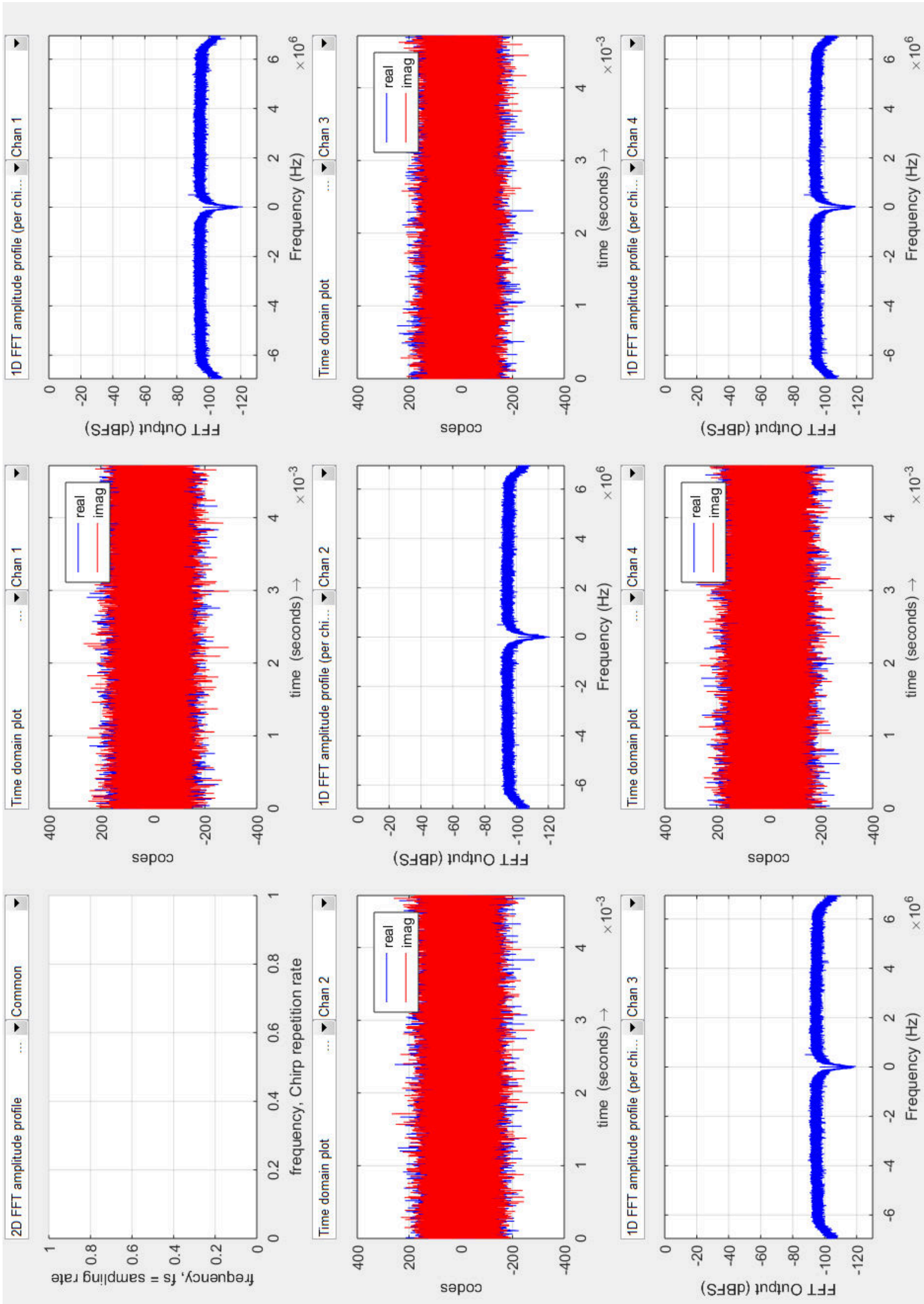

Figure 4-7. LDO Scheme - Noise Floor With Tx –OFF

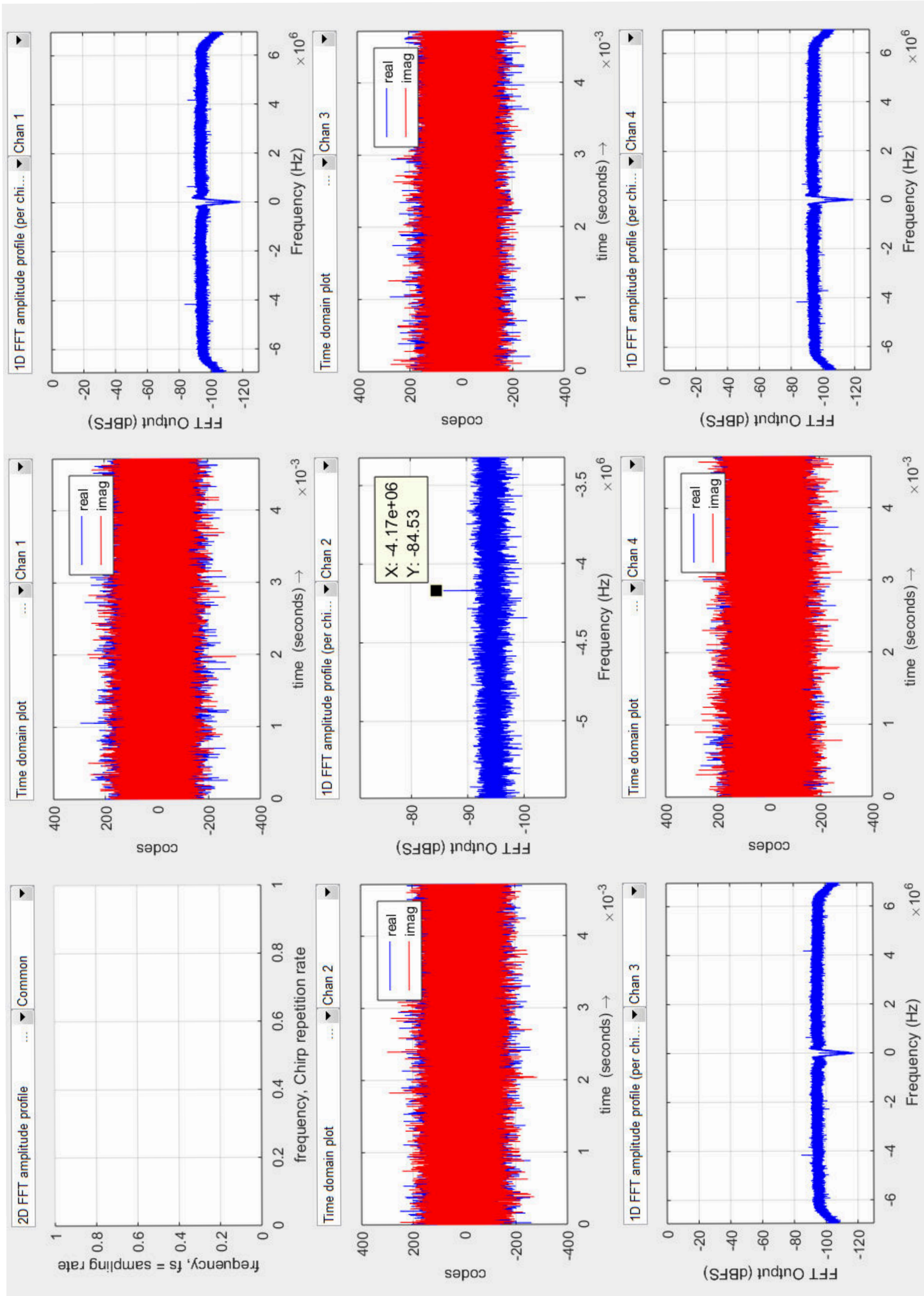

Figure 4-8. LC Filter Scheme – Spur Level

Note

PMIC spur is observed at -84.53 dBFS at RX gain of 48dB.

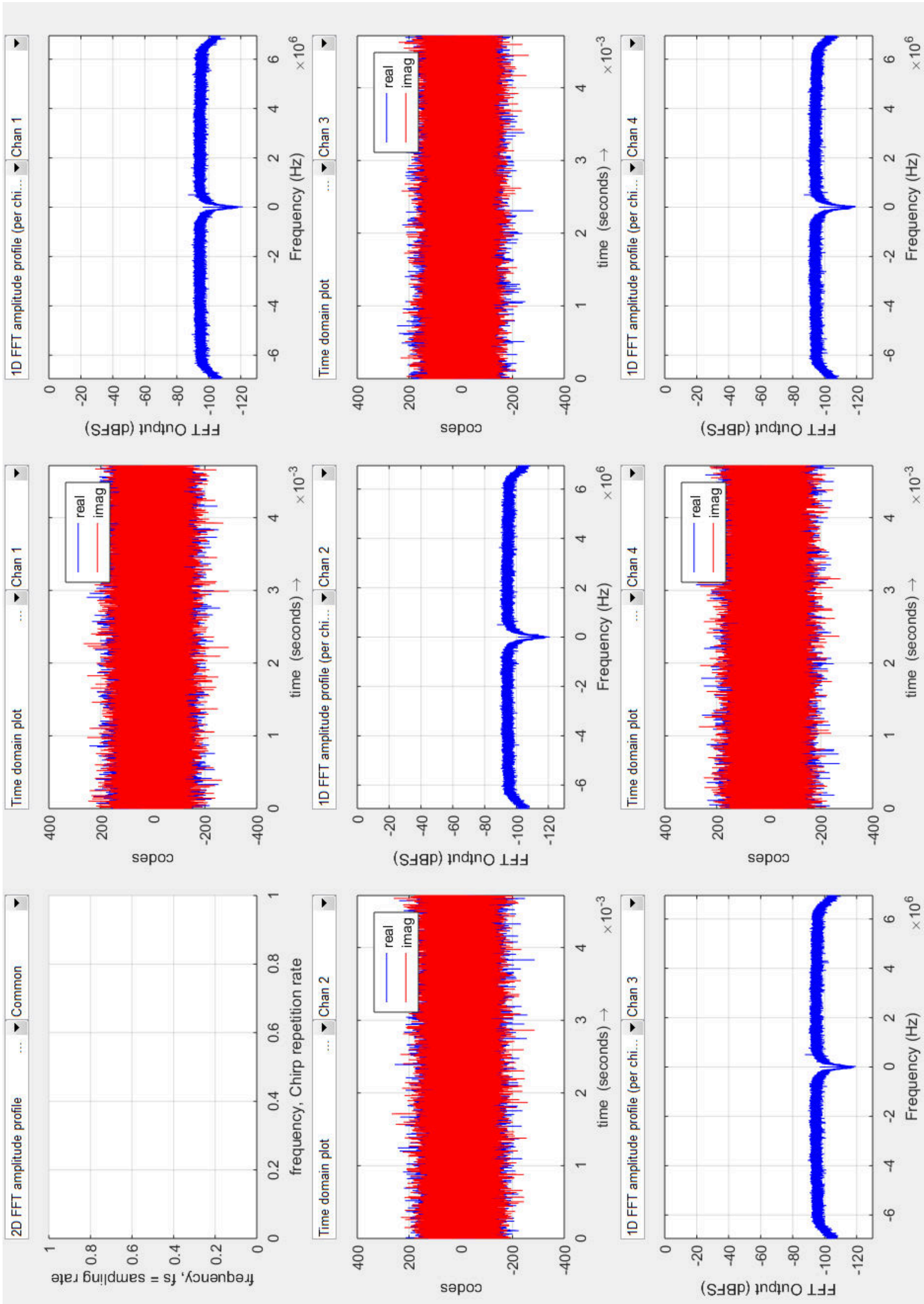

Figure 4-9. LC Filter Scheme - Noise Floor With Tx –OFF

5 Summary

This application report proposes two power management schemes for XWR1xxx devices. Section 4 puts forth an optimal scheme with respect to bill of material and power dissipation, using LC filters. Section 3 explains a scheme using LDOs for achieving better power supply ripple/noise rejection. The LC Filter solution scores better on the Cost and overall System Power saving front in comparison to the LDO scheme."

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