Application Note

TMS320F2833x/2823x to TMS320F2837xD/2837xS/2807x Migration Overview

![Texas Instruments]

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ABSTRACT

This application report describes the differences between the Texas Instruments TMS320F2833x/2823x and the TMS320F2837xD/2837xS/2807x series of microcontrollers for the purpose of assisting with application migration. Functions that are identical in both devices are not necessarily included. All efforts have been made to provide a comprehensive list of the differences between the two device generations within the C2000™ product family; however, the descriptions are explained only to the extent of highlighting areas that require attention when migrating from one device to another. For a detailed description of features specific to each device, see the most recent device-specific data sheet, technical reference manual (TRM), errata and software packages.

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1 Introduction

The TMS320F2833x/2823x and TMS320F2837xD/2837xS/2807x are device members of the C2000 MCU product family. These devices are most commonly used in embedded control applications. The TMS320F2837xD/2837xS/2807x devices feature an updated version of the enhanced control peripherals found on the TMS320F2833x/2823x, which allows for greater flexibility and improved application performance. In addition, the TMS320F2837xD/2837xS/2807x devices feature a boot mode flow which enables expanded booting options that provide the ability to use alternate boot mode selection pins. Enhancements to the CPU include the addition of a trigonometric math unit (TMU) and a Viterbi/Complex Math Unit (VCU-II). Other device enhancements include eight cross-bars (XBARs) for providing a flexible means for interconnecting multiple inputs, outputs, and internal resources.

For the purposes of migration, these devices will be referenced in two groups:

- TMS320F2833x and TMS3202823x - these devices will be referenced as the F2833x and F2823x, respectively. When referenced as both the F2833x and F2823x, this combined group of devices may be referenced as F2833x/23x . If a feature is unique to a specific device type, it will be referenced as F2833x or F2823x.
- TMS320F2837xD, TMS320F2837xS and TMS320F2807x - these devices will be referenced as the F2837xD, F2837xS and F2807x respectively. The combined group of devices may be referenced as F2837xD/S/07x . If a feature is unique to a specific device type, it will be referenced as F2837xD, F2837xS or F2807x.

For a full list of devices currently available within the F2833x/23x and F2837xD/S/07x families, see the TI website at http://www.ti.com/c2000.

As the focus of this document is to describe the differences between the two device groups, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to the other. For a detailed description of features specific to each device, see the device-specific technical reference manuals available on the TI website. This application report does not cover the silicon exceptions or advisories that may be present on each device.

Consult the following silicon errata for specific advisories and workarounds:

- *TMS320F2833x, TMS320F2823x DSCs Silicon Errata*
- *TMS320F2837xD Dual-Core MCUs Silicon Errata*
- *TMS320F2837xS MCUs Silicon Errata*
- *TMS320F2807x MCUs Silicon Errata*

Note

For information regarding any electrical specifications, see the device-specific data sheet.

1.1 Abbreviations

The following abbreviations are used in this document:

- F2833x: Refers to the TMS320F2833x devices. Specifically, TMS320F28335, TMS320F28334, TMS320F28333 and TMS320F28332 . The individual devices in this group are abbreviated as F28335, F28334, F28333 and F28332.
- F2823x: Refers to the TMS320F2823x devices. Specifically, TMS320F28235, TMS320F28234 and TMS320F28232 . The individual devices in this group are abbreviated as F28235, F28234 and F28232.
- F2837xD: Refers to the TMS320F2837xD devices. Specifically, TMS320F28379D, TMS320F28378D, TMS320F28377D, TMS320F28376D, TMS320F28375D and TMS320F28374D. The individual devices in this group are abbreviated as F28379D, F28378D, F28377D, F28376D, F28375D and F28374D.
- F2837xS: Refers to the TMS320F2837xS devices. Specifically, TMS320F28379S, TMS320F28378S, TMS320F28377S, TMS320F28376S, TMS320F28375S and TMS320F28374S. The individual devices in this group are abbreviated as F28379S, F28378S, F28377S, F28376S, F28375S and F28374S.
- F2807x: Refers to the TMS320F2807x devices. Specifically, TMS320F28076 and TMS320F28075. The individual devices in this group are abbreviated as F28076 and F28075.

2 Central Processing Unit (CPU)

The F2837xD/S/07x devices extend the capabilities of the existing TI C28x 32-bit fixed-point CPU architecture by adding a trigonometric math unit (TMU) and a Viterbi/Complex Math Unit (VCU-II). No changes have been made to existing instructions, pipeline, or memory bus architecture and programs written for the C28x CPU are completely compatible with these architectural enhancements.

The Trigonometric Math Unit (TMU) is an extension of the FPU and the C28x instruction set, and it efficiently executes trigonometric and arithmetic operations commonly found in control system applications. Similar to the FPU, the TMU provides hardware support for IEEE-754 single-precision floating-point operations. Seamless code integration is accomplished by built-in compiler support that automatically generates TMU instructions where applicable. This dramatically increases the performance of trigonometric functions, which would otherwise be very cycle intensive. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. Since the TMU uses the same register set and flags as the FPU, there are no special considerations relating to interrupt context save and restore.

The VCU-II is the second-generation Viterbi, Complex Math, and CRC extension to the C28x CPU. The VCU-II extends the capabilities of the C28x CPU by adding registers and instructions to accelerate the performance of FFTs and communications-based algorithms such as Viterbi decoding and Cyclic Redundancy Check.

The C28x CPU, FPU, TMU and VCU architecture and instruction set are documented in the following reference guides:

- *TMS320C28x CPU and Instruction Set Reference Guide*
- *TMS320C28x Extended Instruction Sets Technical Reference Manual*
- *C2000 Real-Time Control Peripherals Reference Guide*
  - This document describes the differences for the above 'unit' types; where a type change represents a major functional feature difference.

3 Development Tools

The F2837xD/S/07x devices have a new set of bit field header files, a new driver library, and new code examples, which are available in C2000Ware. C2000Ware is the successor to controlSUITE as the centralized repository for software and documentation. It has a new structure and all new content updates will be through C2000Ware and Software Development Kits (SDK) only. Note that C2000Ware, unlike controlSUITE, is versioned at the package level and thus results in a separate directory installation for each revision. C2000Ware can be downloaded from:

- http://www.ti.com/tool/C2000WARE

The SDKs are not included in the base C2000Ware download and needs to be downloaded and installed separately. Each SDK contains the development kit files and collateral related to the specific application solution. The SDKs also include a full version of the C2000Ware package. For additional information, see the *controlSUITE™ to C2000Ware Transition Guide*.

3.1 Driver Library (Driverlib)

The Driver Library (Driverlib) is a set of drivers for accessing the peripherals and device configuration registers. While Driverlib is not drivers in the pure operating system sense (does not have a common interface and does not connect into a global device driver), they do provide a software layer to facilitate a slightly higher level of programming. Driverlib provides a more readable and portable approach to peripheral register programming. This portability allows for an easier migration to future device families since the function calls can remain the same even though the control bits may change within and between registers.

3.2 Embedded Application Binary Interface (EABI) Support

The F2837xD/S/07x devices are among the first C2000 device families to support both Common Object File Format (COFF) and Embedded Application Binary Interface (EABI). Refer https://software-dl.ti.com/C2000/docs/optimization_guide/phase1/index.html#application-binary-interface-abi for more information. EABI overcomes several limitations of COFF, which includes the symbolic debugging information not being capable of supporting C/C++, and the limit on the maximum number of sections and length of section names and source files. Note that EABI and COFF are not compatible and conversion between the two formats is not possible. The following is a brief summary of EABI differences compared to COFF.

- Direct initialization
  - Uninitialized data is zero by default in EABI.
  - Initialization of RW data is accomplished via linker-generated compressed copy tables in EABI.
- C++ language support
  - C++ inline function semantics: In COFF, inline functions are treated as static inline and this causes issues for functions that cannot be inlined or have static data. In EABI, inline functions without the 'static' qualifier have external linkage.
  - Better template instantiation: COFF uses a method called late template instantiation and EABI uses early template instantiation. Late template instantiation can run into issues with library code and can result in long link times. Early instantiation uses ELF COMDAT to guarantee templates are always instantiated properly and at most one version of each instantiation is present in the final executable.
  - Table-Driven Exception Handling (TDEH): Almost zero impact on code performance as opposed to COFF which uses setjmp/longjmp to implement C++ exceptions Features enabled by EABI.
- Features enabled by EABI
  - Location attribute: Specify the run-time address of a symbol in C-source code.
  - Noinit/persistent attribute: Specify if a symbol should not be initialized during C auto initialization.
  - Weak attribute: Weak symbol definitions are pre-empted by strong definitions. Weak symbol references are not required to be resolved at link time. Unresolved weak symbols resolve to 0.
  - External aliases: In COFF, the compiler will make A an alias to B if all calls to A can be replaced with B. A and B must be defined in the same file. In EABI, the compiler will make A an alias to B even if B is external.
- Calling convention
  - Scalar calling convention is identical between COFF and EABI.
  - Struct calling convention (EABI):
    - Single field structs are passed/returned by value corresponding to the underlying scalar types.
    - For FPU32, homogenous float structs with size less than 128 bits will be passed by value.
    - Passed in R0H-R3H, then by value on the stack.
    - Structs that are passed by value are also candidates for register allocation.
    - For FPU64, the same applies for 64-bit doubles (R0-R3).
- Double memory size
  - In EABI, double is 64-bit size while in COFF, double is still represented as 32-bit size.
  - C/C++ requires that double be able to represent integer types with at least 10 decimal digits, which effectively requires 64-bit double precision.

Table 3-1 summarizes the compiler-generated section names used by COFF and EABI.

Table 3-1. Section Names

Description	COFF	EABI
Read-Only Sections		
Constdata	.econst	.const
Constdata above 22-bits	.farconst	.farconst
Code	.text	.text
Pre-main constructors	.pinit	.init_array
Exception handling	N/A	.c28xabi.exidx/.c28xabi.extab
Read-Write Sections		
Uninitialized data	.ebss	.bss
Initialized data	N/A	.data
Uninitialized data above 22-bits	.farbss	.farbss
Initialized data above 22-bits	N/A	.fardata
Heap	.esysmem	.sysmem
Stack	.stack	.stack
CIO Buffer	.cio	.bss:cio

For more information about EABI and the migration process, see the following reference guides:

- *TMS320C28x AssemblyLanguage Tools User's Guide*
- *TMS320C28x OptimizingC/C++ Compiler User's Guide*
- C2000Migration from COFF to EABI https://software- dl.ti.com/ccs/esd/documents/ C2000_c28x_migration_from_coff_to_eabi.html

4 Package and Pinout

Both device families are available in an 176-pin low-profile quad flatpack (LQFP) package; however they are not pin-compatible. All other package options are neither package nor pin-compatible. Any application being migrated from the F2833x/23x to the F2837xD/S/07x will require a new board layout to accommodate the changes in the pinout and/or the package. For more information, see the device-specific data sheet.

5 Operating Frequency and Power Management

The F2837xD/S devices have a maximum operating frequency of 200 MHz (120 MHz for 2807x). By comparison, the F2833x/23x devices have a maximum operating frequency of 150 MHz or 100 MHz depending upon the specific device family member.

The F2833x/23x devices require 3.3 V and 1.8 V for operation whereas the F2837xD/S/07x devices require 3.3 V and 1.2 V. In the 2807x device alone, the 1.2 V can be generated with the on-chip voltage regulator (VREG). The F2837xD/S/07x devices have a built-in power-on reset (POR) circuit. During power up, the POR circuit drives the XRS pin low. A watchdog or NMI watchdog reset also drives the pin low. An external circuit may drive the pin to assert a device reset. The POR circuit keeps the I/Os in a high-impedance state during power up. For details related to power management, see the device-specific data sheet.

6 Power Sequencing

Before powering the F2837xD/S/07x devices, no voltage larger than 0.3 V above VDDIO can be applied to any digital pin, and no voltage larger than 0.3 V above VDDA can be applied to any analog pin (including VREFHI). The 3.3-V supplies VDDIO and VDDA should be powered up together and kept within 0.3 V of each other during functional operation. The VDD sequencing requirements are handled by the device. The F2833x/23x devices do not have specific power sequencing requirements, with the exception of the requirement to avoid glitches on the GPIO pins.

7 Input Clock Options

F2833x/23x devices require either an external quartz crystal or an oscillator for clocking the device. F2837xD/S/07x devices feature two on-chip zero-pin internal oscillators (INTOSC1 and INTOSC2) that may be used to clock the device. Note that the accuracy of INTOSCx may not be sufficient for certain applications. In this case, an external quartz crystal or an oscillator may still be used.

8 Memory Map

The memory map between the F2837xD/S/07x and F2833x/23x are different for both Flash as well as RAM and code must be rebuilt accordingly. For specific details about the memory map, see the device-specific data sheet and the specific part number you are interested in.

9 Flash and OTP

This section highlights the major differences in the flash and OTP memory.

9.1 Size and Number of Sectors

The size and number of sectors has changed and code must be rebuilt accordingly. The exact flash size as well as sector configuration varies from device to device. For details, see the device-specific data sheet. Note that code to program the flash should be executed out of RAM and that there should not be any kind of access to the flash bank when an erase or program operation is in progress.

9.2 Flash Parameters

The F2837xD/S/07x and F2833x/23x devices are manufactured using different process technologies. The API used to program the flash memory is therefore completely different. Flash parameters such as erase/program time, number of erase/program cycles and endurance differ between the two device families. Refer to the datasheets for more details.

9.3 Flash Programming

The flash technology used with the F2837xD/S/07x devices is different than that of F2833x/23x devices. The F2837xD/S/07x flash offers faster erase and program operations. It also supports ECC for safety reasons. Since ECC is supported, F2837xD/S/07x flash API allows users to program in four modes – *Fapi_DataOnly, Fapi_AutoEccGeneration, Fapi_DataAndEcc, and Fapi_EccOnly*. Also, F2837xD/S/07x flash allows programming 128-bits at-a-time, whereas F2833x/23x allows programming only 16-bits at-a-time. F2837xD/S/07x flash API supports all these enhanced features and hence API prototypes are not compatible with that of F2833x/23x. For more details, refer to F2837xS Flash API (V1.55) Reference Guide and F2837xD and F2807x Flash API (V1.54) Reference Guide.

9.4 Entry Point into Flash

The flash entry point on F2833x/23x devices is 0x33FFF6. On the F2837xD/S/07x devices, the entry point os 0x00080000.

9.5 Dual Code Security Module (DCSM) and Password Locations

The code security mechanism differs considerably between the F2837xD/S/07x (DCSM) and F2833x/23x (CSM) devices. The DCSM offers protection for two zones (zone-1 and zone-2), and is intended to block access and visibility to the various on-chip memory resources with the purpose of preventing duplication and reverse engineering of proprietary code. The options for both zones are identical, and each memory resource can be assigned to either zone. Either zone can protect each sector of flash individually, each Dx/LSx memory block individually, User OTP, and secure ROM.

Each zone is secured by its own 128-bit (four 32-bit words) user defined password, which is stored in its dedicated OTP location based on a zone-specific link pointer. The user accessible CSMKEY registers are used to secure and unsecure the device, and a new or un-programmed device will be unsecure by default. Since the OTP cannot be erased, flexibility is provided by using a link pointer to select the location of the active zone region within the OTP block, allowing the user to make multiple modifications to the configuration up to thirty times. This is accomplished by exploiting the fact that each bit in the OTP can be programmed one bit at a time, and a "1" can be programmed to a "0", but not erased back to a "1".

The most significant bit position in the link pointer that is programmed to a "0" defines the valid offset base address for the active zone region within the OTP block. This differs from the F2833x/23x devices where the 128-bit (eight 16-bit words) password is stored in the last eight locations in flash.

9.6 OTP

On the F2837xD/S/07x devices, the entire OTP is reserved and unlike the F2833x/23x, it is not available for user code/data (that is, no boot ROM entry point into the OTP). It consists of two 1K x 16 bit error correction code (ECC) protected sectors. The TI OTP sector is reserved for TI internal use only and it contains device calibration/trim data and settings used by the flash state machine for erase and program operations. The DCSM OTP (also known as User OTP) sector contains the user-configurable locations for security and boot process.

10 Boot ROM

This section highlights the boot ROM enhancements of the F2837xD/S/07x devices. The boot ROM has increased in size to 32K x 16 words (per CPU) on the F2837xD/S/07x from 8K x 16 words on the F2833x/23x. The F2837xD/S/07x boot ROM starts at 0x003F 8000.

10.1 Boot ROM Reserved RAM

On the F2837xD/S/07x devices the boot ROM reserved memory is the first 0x0121 words starting at 0x0002. This section contains the boot status, boot mode, and boot stack. Do not to allocate code or data to these memory locations until bootloading is complete.

10.2 Boot Mode Selection

The F2837xD/S/07x device is extremely flexible in its ability to use alternate or reduce boot mode selection pins by programming a BOOTCTRL register, whereas the F2833x/23x boot mode pins are hard-coded and provide pre-determined boot options with no room for flexibility. Table 10-1 compares the two boot mode options which are available for the respective device families.

Table 10-1. Comparison of Boot Mode Options

	F2833x/23x		F2837xD/S/07x	
Boot mode pins	GPIO87, GPIO86, GPIO85 and GPIO84 are the boot mode select pins for this device. Boot mode pins cannot be modified.		GPIO72 and GPIO84 are default boot mode pins for this device. Other GPIOs can be configured to be used as boot mode pins by configuring DCSM-OTP-BOOTCTRL in stand-alone mode and EMU-BOOTCTRL in emulation mode.	
Bootloader options			**Stand-alone mode:** Z1/Z2-OTP-BOOTDEF-LOW and Z1/Z2-OTP-BOOTDEF-HIGH can be configured to select boot modes available below. **Emulation mode:** EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH can be configured to select boot modes available below.	
	Boot mode	No. of options available	Boot mode	No. of options available
	PARALLEL_GPIO	1	PARALLEL_BOOT	2
	SCI_BOOT	1	SCI_BOOT	5
	SPI_BOOT	1	SPI_BOOT	4
	I2C_BOOT	1	I2C_BOOT	3
	CAN_BOOT	1	CAN_BOOT	3
	RAM_BOOT	1	RAM_BOOT	1
	FLASH_BOOT	1	FLASH_BOOT	4
	OTP_BOOT	1	OTP_BOOT	Not available
	WAIT_BOOT	Not available	WAIT_BOOT	2
	McBSP_BOOT	1		Not available
	XINTF x16	1		Not available
	XINTF x32	1		Not available

Table 10-1. Comparison of Boot Mode Options (continued)

	F2833x/23x		F2837xD/S/07x	
	Parallel XINTF	1		Not available
	Jump to SARAM	1		Not available

For additional information about the boot mode selection, see the device-specific TRM.

10.3 Bootloaders

The F2837xD/S/07x allows for flexible pin selection when using a peripheral boot loader, such as SCI, SPI, I2C, or CAN. Unlike the F2833x/23x, the F2837xD/S/07x does not support the OTP boot mode.

11 Architectural Enhancements

The F2837xD/S/07x devices include many new architectural enhancements. This section briefly describes the architectural changes from F2833x/23x to F2837xD/S/07x devices. For more information, refer to the respective TRMs.

11.1 Clock Sources and Domains

There are numerous enhancement and changes to the clock sources and additional clock domains on the F2837xD/S/07x device. These major enhancements and changes include:

- Increase in the number of Peripheral Clock Gating Register to handle the additional and new peripherals
- INTOSC2 is the primary internal clock source and is the default system clock at reset
- INTOSC1 is a backup clock source which normally only clocks the watchdog timers and missing clock detection circuit (MCD)
- External Clock Source (XTAL) can be used as the main system and CAN bit clock source; frequency limits and timing requirements can be found in the datasheets

- External Clock Output (XCLKOUT) can be routed to GPIO73, and the available clock sources are PLLSYSCLK, PLLRAWCLK, CPU1.SYSCLK, CPU2.SYSCLK, AUXPLLRAWCLK, INTOSC1, and INTOSC2.
- SYSPLL Integer Multiplier (IMULT) can vary from 1 to 127. SYSPLL Fractional Multiplier (FMULT) supports four different values: 0, 0.25, 0.5 and 0.75.
- PLLSYSCLK Divide Select (PLLSYSCLKDIV) can be a value of either 1 or an even value up to 126
- XCLKOUT Divide Select (XCLKOUTDIV) has /8 (default on reset) in addition to /1, /2, and /4

11.2 Watchdog Timer

The F2837xD/S/07x watchdog timer includes an optional "windowing" feature which is used to set a minimum delay between counter resets. This, along with the watchdog prescaler, provides a wide range of timeout values. The minimum window check feature complements the timeout mechanism in helping protect against error conditions that bypass large parts of the normal program flow but still include watchdog handling. A WDWCR register contains the desired minimum watchdog count. Any attempt to service the watchdog when WDCNTR is less than WDWCR will trigger a watchdog interrupt or reset. When WDCNTR is greater than or equal to WDWCR, the watchdog can be serviced normally. At reset, the window minimum is zero, which disables the windowing feature.

11.3 Peripheral Interrupt Expansion (PIE)

The F2837xD/S/07x PIE module multiplexes up to sixteen peripheral interrupts into each of the twelve CPU interrupt group lines, further expanding support for up to 192 peripheral interrupt signals. As a result, the interrupt vector table has expanded, and all 16-bit fields in the PIEIFRx and PIEIERx registers are being utilized. The interrupt vector table addressing is effectively split into two tables, where peripheral group interrupts 1 to 8 ranges from 0x0D40 to 0x0DFF and peripheral group interrupts 9 to 16 ranges from 0x0E00 to 0x0EBF. This provides backwards compatibility for the lower range peripheral interrupt vector addresses. The PIE vector table has been updated to accommodate the interrupts issued by the additional peripherals. By comparison, the F2833x/23x multiplexes up to eight peripheral interrupts into each of the twelve groups for up to 96 peripheral interrupt signals.

11.4 Lock Protection Registers

The F2837xD/S/07x devices utilize "LOCK" protection with several configuration registers to protect from spurious CPU writes. Once these associated LOCK register bits are set the respective locked registers can no longer be modified by software. Table 11-1 is a summary of the available LOCK registers.

Table 11-1. LOCK Registers

CLKCFGLOCK1	CPUSYSLOCK1	DMACHSRCSELLOCK	CLA1TASKSRCSELLOCK
DEVCFGLOCK1	DxLOCK	LSxLOCK	GSxLOCK
GPxLOCK	INPUTSELECTLOCK	OUTPUTLOCK	SYNCSOCLOCK
TRIPLOCK	AUXSIGLOCK	DACLOCK	LOCK
COMPLOCK	EMIF1LOCK	EMIF2LOCK	

11.5 General-Purpose Input/Output (GPIO)

The F2837xD/S/07x allows up to twelve independent peripheral signals to be multiplexed on a single GPIO-enabled pin in addition to the CPU-controlled I/O capability. Each pin can be controlled by either a chosen peripheral or the CPU. There are six I/O ports; Port A consists of GPIO0-GPIO31, Port B consists of GPIO32-GPIO63, Port C consists of GPIO64-GPIO95, Port D consists of GPIO96-GPIO127, Port E consists of GPIO128-GPIO159 and Port F consists of GPIO160-GPIO168. The analog signals on this device are multiplexed with digital inputs. These analog I/O (AIO) pins do not have digital output capability and they are assigned to a single port.

11.6 External Interrupts

The F2837xD/S/07x has five external interrupts (two less than the F2833x/23x). Each external interrupt (XINT1-5) can be mapped to any GPIO pin via the Input X-BAR. XINT1-3 has a free-running 16-bit counter which can measure the elapsed time between interrupts.

11.7 Crossbar (X-BAR)

The X-BARs provide a flexible means for interconnecting multiple inputs, outputs, and internal resources in various configurations. The F2837xD/S/07x devices contains three X-BARs: the Input X-BAR, the Output X-BAR, and the ePWM X-BAR.

- Input X-BAR – is used to route external GPIO signals into the device. It has access to every GPIO pin where each signal can be routed to any or multiple destinations which include the ADCs, eCAPs, ePWMs, Output X-BAR, and external interrupts. The F2837xD/S/07x Input X-BAR has fourteen inputs (INPUT1 through INPUT14) and INPUT7 through INPUT12 can be selected as an external input to each of the eCAP modules.

Note

This differs from the F2833x/23xdevices which uses the GPIO multiplexer to select a specific dedicated input pin to access the eCAP module.

- Output X-BAR – is used to route various internal signals out of the device. It contains eight outputs that are routed to the GPIO structure, where each output has one or multiple assigned pin positions, which are labeled as OUTPUTXBARx. Additionally, the Output X-BAR can select a single signal or logically OR up to 32 signals.
- ePWM X-BAR – is used to route signals to the ePWM Digital Compare submodules of each ePWM module for actions such as trip zones and synchronizing. It contains eight outputs that are routed as TRIPx signals to each ePWM module. Likewise, the ePWM X-Bar can select a single signal or logically OR up to 32 signals.

12 Peripherals

New peripherals have been added and most of the existing peripherals have been updated. This section briefly describes the additions and changes from F2833x/23x to F2837xD/S/07x devices. For an overview of the available peripherals, see the *C2000 Real-Time Control Peripherals Reference Guide*.

12.1 New Peripherals

The F2837xD/S/07x devices include new peripherals that are not available on the F2833x/23x devices. For more information, see the device-specific data sheet.

12.1.1 Analog Subsystem Interconnect

The F2837xD/S/07x utilizes an analog subsystem interconnect which enables flexible pin usage. The CMPSS inputs and digital inputs are multiplexed with the ADC inputs. This type of interconnect permits a single pin to route a signal to multiple analog modules. The analog pins are organized into analog groups around a CMPSS module, and the routing is defined in an analog pin and internal connections table.

12.1.2 Comparator Subsystem (CMPSS)

While there are no CMPSS modules in the F2833x/23xdevices, there are up to eight CMPSS modules available on the F2837xD/S/07x devices. Each module contains two comparators, two reference 12-bit DACs, two digital filters and one ramp generator. The CMPSS modules are useful for implementing peak current mode control and voltage trip monitoring, which are used in applications such as switched-mode power control and power factor correction. The module is designed around a pair of analog comparators which generates a digital output indicating if the voltage on the positive input is greater than the voltage on the negative input. The positive input to the comparator is always driven from an external pin. The negative input can be driven by either an external pin or an internal programmable 12-bit DAC as a reference voltage. Values written to the DAC can take effect immediately or be synchronized with ePWM events. A falling-ramp generator is available to control the internal DAC reference value for one comparator in the module, which enables peak current mode control in digital power applications. Each comparator output is fed through a programmable digital filter to prevent electrical switching noise from causing spurious trip signals. The output of the CMPSS generates trip signals to the ePWM event trigger submodule and GPIO structure. Additionally, the CMPSS features PWM blanking capability to clear-and-reset existing or imminent trip conditions near the ePWM cycle boundaries. Also, by using the analog subsystem interconnect scheme the CMPSS comparator positive and negative input signals are independently selectable.

12.1.3 Control Law Accelerator (CLA)

The F2837xD/S/07x devices have a CLA. CLA is not available on the F2833x/23x devices.

12.2 Control Peripherals

This section describes the changes and additions to the F2837xD/S/07x device control peripherals. For more information, refer to the following reference guide:

• *C2000 Real-Time Control Peripherals Reference Guide*

12.2.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM module on the F2837xD/S/07x devices remains functionally the same, and includes many enhancements. As a result, additional registers have been added, and the ePWM address space has been remapped for better alignment and usage. These enhancements include:

• Counter Compare Sub-module – added counter compares CMPC and CMPD to allow Interrupts and ADC SOC events to be generated.
• Action Qualifier Sub-module – added shadow loading of AQCTLA and AQCTLB registers to enable changes that must occur at the end of a period even when the phase changes. Additionally, shadow to active load on SYNC and Global Reload for the Action Qualifier Sub-module is supported.
• Dead-Band Sub-module – added high resolution capability to dead-band RED and FED in half-cycle clocking mode. Includes features to enable both RED and FED on either PWM outputs. Increased dead-band with 14-bit counters. Dead-band/dead-band high-resolution registers are shadowed to allow dynamic configuration changes.
• Event Trigger Sub-module – Interrupts and ADC start-of-conversion can now be generated on both the TBCTR == zero and TBCTR == period events. This feature enables dual edge PWM control. Additionally, the ADC start-of conversion can be generated from an event defined in the digital compare submodule. Enhanced pre-scaling logic is also implemented to issue interrupt requests and ADC SOC expanded up to every 15 events, to allow software initialization of event counters on SYNC event.
• Trip-Zone Sub-module – independent flags have been added to reflect the trip status for each of the TZ sources. Also, changes have been made to the trip zone module to support certain power converter switching techniques, such as valley switching. Trip-zone TZ4 is sourced from an inverted EQEPxERR signal, TZ5 is connected to the system clock fail logic, and TZ6 is sourced from the EMUSTOP output from the CPU.

- Digital Compare Sub-module – Addition of the digital compare submodule which enhances the event triggering and trip zone submodules by providing filtering, blanking and improved trip functionality to digital compare signals. Such features are essential for peak current mode control and for support of analog comparators. The Digital Compare Trip Select logic [DCTRIPSEL] has up to 12 external trip sources that are selected by the Input X-BAR logic. This is in addition to an ability to OR all of them, for up to 14 external and internal sources which are used to create the respective DCxEVTs. Blanking window filter register width is 16 bits, and the DCCAP functionality has been enhanced to provide more programming flexibility.
- High-Resolution PWM – includes the ability to enable high-resolution period and duty cycle control on both ePWMxA and ePWMxB outputs.
- Simultaneous Writes to TBPRD and CMPx Registers – allows writes to TBPRD, CMPA:CMPAHR, CMPB:CMPBHR, CMPC, and CMPD of any ePWM module to be tied to any other ePWM module, and also allows all ePWM modules to be tied to a particular ePWM module, if desired.
- Shadow to Active Load on SYNC of TBPRD and CMP Registers – supports simultaneous writes of TBPRD and CMPA/B/C/D registers.
- Delayed Trip Functionality – changes have been added to achieve dead-band insertion capabilities to support delayed trip functionality, which is needed for peak current mode control type applications. This has been accomplished by allowing comparator events to go into the Action Qualifier Submodule as a trigger event (Events T1 and T2). If comparator T1/T2 events are used to modify the PWM, changes to the PWM waveform will not take place immediately, but instead they will synchronize to the next TBCLK.
- One Shot and Global Reload of Registers – allows one shot and global reload capability from shadow to active registers. This avoids partial reload conditions in, for example, multi-phase applications. It also allows programmable pre-scale of shadow to active reload events. Global Load can simplify ePWM software by removing interrupts and ensuring that all registers are loaded at the same time.
- PWM SYNC Related Enhancements – sync scheme now includes two possible external PWM SYNCIN sources that feed into every third instance of ePWM modules (ex. ePWM1, ePWM4, ePWM7, and so forth). The sync scheme allows PWM SYNCOUT generation based on CMPC and CMPD events. These events can also be used for PWMSYNC pulse selection.

12.2.2 Enhanced Capture Module (eCAP)

The F2837xD/S/07x devices have six eCAP modules. The F2833x/23x devices have up to six.

12.2.3 Enhanced Quadrature Encode Pulse Module (eQEP)

The F2837xD/S/07x devices have up to three eQEP modules. The F2833x/23x devices have two.

12.2.4 Sigma-Delta Filter Module (SDFM)

The F2837xD/S/07x devices support up to eight Sigma-Delta Filter Module (SDFM) input channels, two parallel filters per channel with the following features:

- Standard SDFM data filtering
- Comparator filter for fast action for out of range

12.3 Analog Peripherals

This section describes the changes and additions to the F2837xD/S/07x device analog peripherals. For more information, refer to the following reference guide:

- *C2000 Real-Time Control Peripherals Reference Guide*

12.3.1 Analog-to-Digital Converter (ADC)

Unlike the ADC found on the F2833x/23x where a single ADC has two sample-and-hold (S/H) circuits, the F2837xD/S/07x utilizes four independent ADCs and each has a single S/H circuit. This allows the F2837xD/S/07x to efficiently manage multiple analog signals for enhanced overall system throughput. By using multiple ADC modules, simultaneous sampling or independent operation can be achieved. The ADC modules are implemented using a successive approximation (SAR) architecture and support 12-bit or 16-bit resolution with throughput of 3.5 MSPS or 1.1 MSPS per ADC, respectively. Note that the 16-bit ADC uses "fully differential inputs" only, which is different than the single ended inputs on the F2833x/23x device. Refer to SAR ADC Input Types for more information. Following are the migration points to be cognizant of:

- F2837xD/S/07x devices employ a start-of-conversion (SOC) based architecture. Individual SOCs can be combined in a flexible way to create sequences of conversions of arbitrary length. This works well to map sampling schemes in auto conversion mode from F2833x/23x (single, dual, or cascaded auto-conversion sequences should all map well to sets of SOCs configured to use the same trigger source).
- The F2837xD/S/07x adds burst priority mode, in addition to the round robin and high priority modes. This mode uses a separate Burst Control register to select the burst size and trigger source. Burst mode functions similarly to the F2833x/23x sequencer architecture in start/stop mode. This can be used to emulate circular buffer sampling strategies or sampling strategies that alternate between different conversion from the same trigger. Note: Only one burst mode sequencer is available. If the F2833x/23x design is using dual sequencers both in start/stop mode, the scheme may not map exactly to the F2837xD/S/07x-based design.
- The F2837xD/S/07x has four flexible PIE interrupts (per ADC) rather than three found on the F2833x/23x.
- To further enhance the capabilities of the F2837xD/S/07x ADC, each ADC module incorporates four post-processing blocks (PPB), and each PPB can be linked to any of the ADC result registers. The PPBs can be used for offset correction, calculating an error from a set-point, detecting a limit and zero-crossing, and capturing a trigger-to-sample delay:
- The F2837xD/S/07x ADC S+H is clocked from SYSCLK (not ADCCLK). The ADCCLK does not free-run when the ADC is not converting.
- It is now possible to individually configure each SOC (each channel) for a different S+H length.
- F2837xD/S/07x V_{REF} is ratiometric (for example, you can input 2.5V into VREFHI to get a 2.5V ADC range or input 3.0V to get a 3.0V range) compared to the fixed 3.0V range of F2833x/23x devices.

12.4 Communication Peripherals

This section describes the changes and additions to the F2837xD/S/07x device communication peripherals. For more information, see the following reference guide:

- *C2000 Real-Time Control Peripherals Reference Guide*

12.4.1 SPI

The F2837xD/S/07x SPI includes the following enhancements:

- High-speed mode
- DMA support

12.4.2 SCI

The F2837xD/S/07x SCI module remains functionally the same as the F2833x/23x .

12.4.3 USB

The F2837xD/S/07x devices have one USB port. No USB port on F2833x/23x devices.

12.4.4 I2C

The F2837xD/S/07x has two I2C modules. The F2833x/23x has one I2C module.

12.4.5 CAN

The F2837xD/S/07x DCAN has a different register structure compared to F2833x/23x eCAN and therefore code written for one module cannot be migrated to another.

The following features are available in F2837xD/S/07x DCAN and are not available in F2833x/23x eCAN:

- Parity check mechanism for all RAM modules
- Automatic Retransmission (upon loss of arbitration) can be disabled
- Silent mode (Node listens passively)
- Mailbox RAM may be combined to form FIFO buffers
- Data can be monitored on CANTX pin in self-test mode

The following are the features that are available in F2833x/23x eCAN and are not available in F2837xD/S/07x DCAN:

- Timestamping of messages
- Transmission priority configuration (TPL)
- Data-byte order configuration (DBO)

For more information, see the following application report:

* *Programming Examples and Debug Strategies for the DCAN Module.*

13 Configurable Logic Block (CLB)

The F2837xD/S/07x devices have the Configurable Logic Block (CLB). The CLB is a collection of configurable blocks that can be inter-connected using software to implement custom digital logic functions. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals, such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as simple PWM generators, or to implement custom serial data exchange protocols.

14 Device Comparison Summary

In this section, Table 14-1 provides a general feature comparison between the F2837xD/S/07x and the F2833x/23x device families. For specific details about device features, maximum clock frequency, memory sizes, and peripheral availability and quantity, see the device-specific data sheet. Only the super-set part number is shown for a device family.

Table 14-1. Device Comparison Matrix

	F28379D	F28075	F28335
Clock	200 MHz	120 MHz	150 MHz
VCU-II	√ [1]	-	-
TMU	√	√	-
CLA	√ (Type 1)	√ (Type 1)	-
Flash / RAM	512K x 16 / 102K x 16	256K x 16 / 50K x 16	256K x 16 / 34K x 16
EMIF	√	√	-
XINTF	-	-	√
32-bit CPU Timers	√	√	√
Watchdog Timer	√	√	√
NMI WD Timer	√	√	-
0-pin internal Oscillators	√	√	-
ADC	16-bit mode and 12-bit mode 3.5 MSPS x 4 /1.1 MSPS x 4	12-bit mode 3.1MSPS x 3	12-bit mode 12.5 MSPS x 1
CMPSS w/ 2 DACs	√	√	-
Buffered DAC	√	√	-
ePWM / HRPWM	√ / √ (Type 4)	√ / √ (Type 4)	√ / √ (Type 0)
eCAP / HRCAP	√ / √ (Type 0)	√ / √ (Type 0)	√ / - (Type 0)
eQEP	√ (Type 0)	√ (Type 0)	√ (Type 0)
SDFM	√	√	-
CAN [2]	√ (DCAN)	√ (eCAN)	√ (eCAN)
I2C	√ (Type 1)	√ (Type 0)	√ (Type 0)
SCI	√	√	√
SPI	√ (Type 2)	√ (Type 2)	√ (Type 0)
McBSP	√	√	√
USB	√	√	-
uPP	√	-	-
X-BARs	√	√	-

Table 14-1. Device Comparison Matrix (continued)

	F28379D	F28075	F28335
CLB	√	√	-

(1) √ indicates available. For details, check the specific device.
(2) DCAN and eCAN are not software compatible.

For more detailed device information, see the following data sheets:

- *TMS320F28002x Microcontrollers Data Sheet*
- *TMS320F2803x Microcontrollers Data Sheet*
- *TMS320F2802x Microcontrollers Data Sheet*

15 References

- Texas Instruments: *TMS320F2833x, TMS320F2823x Digital Signal Controllers (DSCs) Data Sheet*
- Texas Instruments: *TMS320C28x CPU and Instruction Set Reference Guide*
- Texas Instruments: *TMS320C28x Extended Instruction Sets Technical Reference Manual*
- Texas Instruments: *C2000 Real-Time Control Peripherals Reference Guide*
- Texas Instruments: *TMS320C28x Assembly Language Tools User's Guide*
- Texas Instruments: *TMS320C28x Optimizing C/C++ Compiler User's Guide*
- Texas Instruments: *controlSUITE™ to C2000Ware Transition Guide*
- http://www.ti.com/tool/C2000WARE
- Texas Instruments: *C28x Embedded Application Binary Interface*
- C2000 Migration from COFF to EABI https://software-dl.ti.com/ccs/esd/documents/C2000_c28x_migration_from_coff_to_eabi.html
- Texas Instruments: *TMS320F28002x Flash API Reference Guide*
- Texas Instruments: *Programming Examples and Debug Strategies for the DCAN Module*
- Texas Instruments: *TMS320F28004x Boot Features and Configurations*
- Texas Instruments: *TMS320F2833x, TMS320F2823x Digital Signal Controllers (DSCs) Data Sheet*
- Texas Instruments: *TMS320x2833x, TMS320x2823x Technical Reference Manual*
- Texas Instruments: *TMS320F2833x, TMS320F2823x DSCs Silicon Errata*
- Texas Instruments: *TMS320F2837xD Dual-Core Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F2837xD Dual-Core Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F2837xD Dual-Core MCUs Silicon Errata*
- Texas Instruments: *TMS320F2837xS Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F2837xS Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F2837xS MCUs Silicon Errata*
- Texas Instruments: *TMS320F2807x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F2807x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F2807x MCUs Silicon Errata*

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