Application Report
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Migrating From TMS320C5535 to TMS320C5545

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ABSTRACT

This application report provides a summary of the similarities and differences between the TMS320C5535 and TMS320C5545 devices to minimize changes required to migrate from TMS320C5535 to TMS320CC5545.

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1 Introduction

Both C5535 and C5545 are next generation devices of the C5515 single core DSP family products which incorporate new features and improvements based on customer's feedback and requirements.

1.1 The Purpose of C5545

C5545 is not intended as a drop-in replacement to C5535. C5545 is intended to free up increasingly valuable printed circuit board (PCB) space. C5545 provides the same peripherals and functional features as the C5535 but is packaged in a smaller package and reduced pin out for easy routing.

2 Basic Feature Comparisons

Table 1 highlights the differences in features between the two devices (processor operating frequencies, device operating temperature range, device package size and # of pins).

Table 1. Feature Comparison

	TMS320C5535	TMS320C5545
DSP	1 C55 v3.3	1 C55 v3.3
DSP MHz (Max.)	50, 100	60, 100, 120
Other hardware acceleration	FFT Coprocessor	FFT Coprocessor
Total on-chip memory - RAM	320KB	320KB
On-chip memory - SARAM	256KB SARAM	256KB SARAM
On-chip memory - DARAM	64KB DARAM	64KB DARAM
On-chip memory - SAROM	128KB SAROM	128KB SAROM
General-purpose memory	N/A	N/A
DRAM	N/A	N/A
Host-post interface (HPI)	N/A	N/A
Multichannel buffered serial port (McBSP)	N/A	N/A
Universal asynchronous receiver/transmitter (UART) Serial Communications Interface (SCI)	1	1
Inter-IC Sound (I2S)	4	4
Serial peripheral interface (SPI)	1 with 4 chip selects	1 with 3 chip selects
Liquid crystal display (LCD)	1	1
USB 2.0	1 (Full and High Speed, Device Only)	1 (Full and High Speed, Device Only)
Multimedia Card (MMC)/Secure Digital (SD)	2 (no MMC, eMMC/SD)	2 (no MMC, eMMC/SD)
Analog-to-Digital Converter (ADC)	4-Pin 10 Bit	3-pin 10 Bit
Inter-Integrated Circuit (I2C)	1 master or slave	1 master or slave
DMA (Ch)	4-Ch each with 4-Ch for a total of 16-Ch	4-Ch each with 4-Ch for a total of 16-Ch
Timer	2 32-bit GP, 1 32-bit GP or watchdog	2 32-bit GP, 1 32-bit GP or watchdog
Real-Time Clock (RTC)	1	1
Low Drop Out (LDO)	ANA_LDO, USB_LDO, DSP_LDO	ANA_LDO, USB_LDO, DSP_LDO
IO Supply (V)	1.8, 2.5, 2.75, 3.3	1.8, 2.5, 2.75, 3.3
Operating temperature range (°C)	-10 to 70, -40 to 85	-10 to 70, -40 to 85
Pin/Package	144BGA MICROSTAR	118BGA MICROSTAR
BGA Package Size	12 x 12 mm	7 x 7 mm

3 Module Comparison

This section describes the module differences requiring development migrating from C5535 to C5545.

As shown in Table 1, both devices support major module peripherals. The only affected modules are the SAR ADC and RTC. Plus the XF pin is removed.

3.1 SAR ADC

GPAIN0 pin is not supported in C5545. This is a 3.6-V tolerant analog input with internal voltage division for conversion of battery voltage.

3.2 RTC

The wakeup feature is removed in C5545. As a result, RTC_CLKOUT and WAKEUP pins are removed.

3.3 XF

XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. This pin is not supported in C5545.

3.4 LCD_CS1_E1/SPI_CS1

This pin is also removed from C5545.

4 Pin-Out Comparison

This section lists the pins that are removed from C5545.

As described in above section, some functions are removed in order to reduce the pin count for a smaller package. This is the list of pins not supported in C5545: GPAIN0, RTC_CLKOUT, WAKEUP, XF, LCD_CS1_E1/SPI_CS1, RSV1, RSV2, RSV6, RSV7, RSV8, RSV9, RSV11 and RSV12.

RSV17 in C5545 is the same as RSV7 in C5535.

USB_VSSA1P3 is internally tied to USB_VSS1P3.

Table 2. Pin-Out Comparison

C5535 Package Pin	C5535 Data Sheet Name	C5545 Package Pin	C5545 Data Sheet Name
A1	V_{SSA_PLL}	E8	V_{SSA_PLL}
A2	CLKOUT	C12	CLKOUT
A3	RTC_CLKOUT	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
A4	SDA	D11	SDA
A5	WAKEUP	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
A6	RTC_XO	E11	RTC_XO
A7	RTC_XI	F11	RTC_XI
A8	GPAIN0	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
A9	GPAIN2	F10	GPAIN2
A10	GPAIN3	J12	GPAIN3
A11	RSV4	H10	RSV4
A12	RSV0	L12	RSV0
A13	DSP_LDOO	M11	DSP_LDOO
A14	VSS	See (1)	V_{SS}
B1	$\overline{INT1}$	C11	$\overline{INT1}$
B2	V_{SS}	See (1)	V_{SS}
B3	V_{SS}	See (1)	V_{SS}
B4	CV_{DDRTC}		
B5	CV_{DDRTC}	D10	CVDDRTC
B6	V_{SSA_ANA}	K12	V_{SSA_ANA}
B7	V_{DDA_ANA}	G11	V_{DDA_ANA}
B8	GPAIN1	F8	GPAIN1
B9	ANA_LDOO	H11	ANA_LDOO
B10	LDOI	L11	LDOI

Table 2. Pin-Out Comparison (continued)

C5535 Package Pin	C5535 Data Sheet Name	C5545 Package Pin	C5545 Data Sheet Name
B11	RSV5	J10	RSV5
B12	RSV3	K11	RSV3
B13	RSV6	N/A	NOT SUPPORTED
B14	LDOI	L10	LDOI
C1	CLKIN	E12	CLKIN
C2	$\overline{INT0}$	B12	$\overline{INT0}$
C3	DV_{DDRTC}	F12	DV_{DDRTC}
C4	SCL	B11	SCL
C5	V_{SSRTC}	G12	V_{SSRTC}
C6	DV_{DDIO}	B10	DV_{DDIO}
C7	V_{DDA_PLL}	E10	V_{DDA_PLL}
C8	V_{SS}	See (1)	V_{SS}
C9	V_{SSA_ANA}	H12	V_{SSA_ANA}
C10	BG_CAP	J11	BG_CAP
C11	CV_{DD}	See (2)	CV_{DD}
C12	V_{SS}	See (1)	V_{SS}
C13	$\overline{DSP\_LDO\_EN}$	M12	$\overline{DSP\_LDO\_EN}$
C14	LDOI	L11	LDOI
D1	CLK_SEL	D12	CLK_SEL
D2	$\overline{RESET}$	A11	$\overline{RESET}$
D3	CV_{DD}	See (2)	CV_{DD}
D4	V_{SS}	See (1)	V_{SS}
D5	V_{SS}	See (1)	V_{SS}
D10	V_{SS}	See (1)	V_{SS}
D11	CV_{DD}	See (2)	CV_{DD}
D12	USB_V_{SSOSC}	M9	USB_V_{SSOSC}
D13	USB_LDOO	M10	USB_LDOO
D14	USB_MXO	K9	USB_MXO
E1	RSV7	M5	REV17 (NAME CHANGED)
E2	RSV11	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
E3	V_{SS}	A2	V_{SS}
E4	V_{SS}	See (1)	V_{SS}
E11	V_{SS}	See (1)	V_{SS}
E12	USB_V_{DD1P3}	M8	USB_VDD1P3
E13	USB_V_{DDOSC}	K8	USB_V_{DDOSC}
E14	USB_MXI	L9	USB_MXI
F1	RSV8	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
F2	CV_{DD}	See (2)	CV_{DD}
F3	V_{SS}	See (1)	V_{SS}
F12	USB_V_{SSREF}	H8	USB_V_{SSREF}
F13	USB_V_{SSPLL}	L8	USB_V_{SSPLL}
F14	USB_V_{DD1P3}	L5	USB_V_{DD1P3}
G1	RSV9	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
G2	RSV12	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
G3	CV_{DD}	See (2)	CV_{DD}
G12	USB_V_{DDA3P3}	L7	USB_V_{DDA3P3}
G13	USB_V_{DDPLL}	M7	USB_V_{DDPLL}

Table 2. Pin-Out Comparison (continued)

C5535 Package Pin	C5535 Data Sheet Name	C5545 Package Pin	C5545 Data Sheet Name
G14	USB_R1	K7	USB_R1
H1	RSV10	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
H2	CV_{DD}	See (2)	CV_{DD}
H3	V_{SS}	See (1)	V_{SS}
H12	USB_V_{DDA1P3}	K6	USB_V_{DDA1P3}
H13	USB_V_{SSA3P3}	H7	USB_V_{SSA3P3}
H14	USB_DP	L6	USB_DP
J1	SD0_D0/I2S0_DX/GP[2]	D5	SD0_D0/I2S0_DX/GP[2]
J2	LCD_D[2]/GP[12]	E2	LCD_D[2]/GP[12]
J3	XF	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
J12	USB_V_{SSA1P3}	N/A	INTERNALLY TIED TO USB_V_{SS1P3}
J13	V_{SS}	See (1)	V_{SS}
J14	USB_DM	M6	USB_DM
K1	LCD_D[1]/SPI_TX	C2	LCD_D[1]/SPI_TX
K2	TDI	D4	TDI
K3	V_{SS}	See (1)	V_{SS}
K4	V_{SS}	See (1)	V_{SS}
K11	CV_{DD}	See (2)	CV_{DD}
K12	RSV1	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
K13	USB_V_{DD1P3}	N/A	SAME AS L5 AND M8
K14	USB_V_{SS1P3}	H6	USB_V_{SS1P3}
L1	LCD_CS0_E0/SPI_CS0	A2	LCD_CS0_E0/SPI_CS0
L2	EMU0	B3	EMU0
L3	LCD_EN_RDB/SPI_CLK	A1	LCD_EN_RDB/SPI_CLK
L4	DV_{DDIO}	D2	DV_{DDIO}
L5	V_{SS}	See (1)	V_{SS}
L10	V_{SS}	See (1)	V_{SS}
L11	SD1_CMD/I2S1_FS/GP[7]	L4	SD1_CMD/I2S1_FS/GP[7]
L12	SD1_D2/GP[10]	M4	SD1_D2/GP[10]
L13	RSV2	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
L14	USB_VBUS	K5	USB_VBUS
M1	EMU1	B1	EMU1
M2	LCD_CS1_E1/SPI_CS1	N/A	NOT SUPPORTED - Removed to Reduce Pin Count
M3	DV_{DDIO}	H2	DV_{DDIO}
M4	DV_{DDIO}	M2	DV_{DDIO}
M5	LCD_RS/SPI_CS3	A3	LCD_RS/SPI_CS3
M6	CV_{DD}	See (2)	CV_{DD}
M7	V_{SS}	See (1)	V_{SS}
M8	SD0_CLK/I2S0_CLK/GP[0]	E5	SD0_CLK/I2S0_CLK/GP[0]
M9	CV_{DD}	See (2)	CV_{DD}
M10	SD0_CMD/I2S0_FS/GP[1]	J2	SD0_CMD/I2S0_FS/GP[1]
M11	LCD_D[15]/UART_TXD/GP[31]/I2S3_DX	L2	LCD_D[15]/UART_TXD/GP[31]/I2S3_DX
M12	SD1_D3/GP[11]	G5	SD1_D3/GP[11]
M13	SD1_D0/I2S1_DX/GP[8]	L3	SD1_D0/I2S1_DX/GP[8]
M14	SD1_CLK/I2S1_CLK/GP[6]	H5	SD1_CLK/I2S1_CLK/GP[6]
N1	TDO	D1	TDO
N2	LCD_RW_WRB/SPI_CS2	B2	LCD_RW_WRB/SPI_CS2

Table 2. Pin-Out Comparison (continued)

C5535 Package Pin	C5535 Data Sheet Name	C5545 Package Pin	C5545 Data Sheet Name
N3	TCK	C3	TCK
N4	LCD_D[0]/SPI_RX	A4	LCD_D[0]/SPI_RX
N5	LCD_D[3]/GP[13]	E1	LCD_D[3]/GP[13]
N6	TMS	D3	TMS
N7	LCD_D[5]/GP[15]	G1	LCD_D[5]/GP[15]
N8	DV_{DDIO}	N/A	INTERNALLY TIED TO B10, D2, H2 AND M2
N9	CV_{DD}	See (2)	CV_{DD}
N10	LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0	K1	LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0
N11	DV_{DDIO}	N/A	INTERNALLY TIED TO B10, D2, H2 AND M2
N12	LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK	J3	LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK
N13	MMC0_D2/GP[4]	M3	MMC0_D2/GP[4]
N14	DV_{DDIO}	N/A	INTERNALLY TIED TO B10, D2, H2 AND M2
P1	V_{SS}	See (1)	V_{SS}
P2	LCD_D[4]/GP[14]	F1	LCD_D[4]/GP[14]
P3	LCD_D[6]/GP[16]	E3	LCD_D[6]/GP[16]
P4	$\overline{TRST}$	F2	$\overline{TRST}$
P5	LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK	H1	LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK
P6	MMC0_D1/I2S0_RX/GP[3]	G2	MMC0_D1/I2S0_RX/GP[3]
P7	MMC0_D3/GP[5]	G3	MMC0_D3/GP[5]
P8	LCD_D[7]/GP[17]	J1	LCD_D[7]/GP[17]
P9	LCD_D[10]/I2S2_RX/GP[20]/SPI_RX	F5	LCD_D[10]/I2S2_RX/GP[20]/SPI_RX
P10	MMC1_D1/I2S1_RX/GP[9]	H3	MMC1_D1/I2S1_RX/GP[9]
P11	LCD_D[11]/I2S2_DX/GP[27]/SPI_TX	K2	LCD_D[11]/I2S2_DX/GP[27]/SPI_TX
P12	LCD_D[13]/UART_CTS/GP[29]/I2S3_FS	M1	LCD_D[13]/UART_CTS/GP[29]/I2S3_FS
P13	LCD_D[14]/UART_RXD/GP[30]/I2S3_RX	L1	LCD_D[14]/UART_RXD/GP[30]/I2S3_RX
P14	V_{SS}	See (1)	V_{SS}

(1) A5, A6, A7, A8, A10, A12, B6, B7, B9, C4, C7, C9, F3, F7, G6, G8 AND K4 V_{SS}

(2) A9, B5, B8, C6, E6, G7 AND J9 CV_{DD}

5 Package Comparison

This section describes the package differences among the two devices.

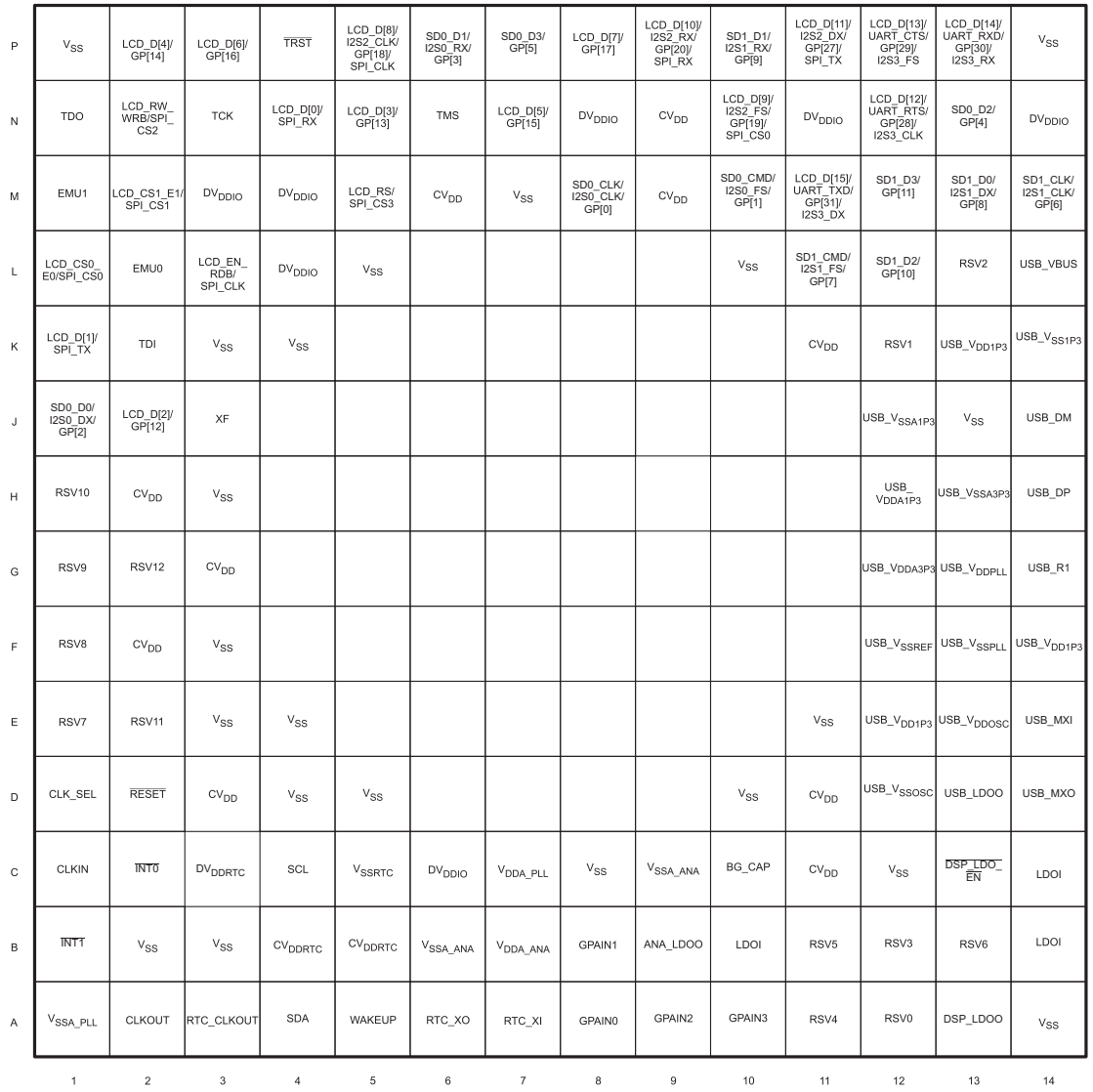
C5545 is housed in a 7x7 mm 118 pins MicroStar BGA. The C5535 is housed in a 12x12 mm 144 pin MicroStar BGA.

Table 3. Package Comparison Table

Device	C5545	C5535
Package Size	7 x 7 mm	12 x 12 mm
Package Pin Count	118	144
Package Type	Micro Star	Micro Star

	1	2	3	4	5	6	7	8	9	10	11	12	
M	LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	DV_{DDIO}	SD0_D2/ GP[4]	SD1_D2/ GP[10]	RSV17	USB_DM	USB_V_{DDPLL}	USB_V_{DD1P3}	USB_V_{SSOSC}	USB_LDOO	DSP_LDOO	$\overline{DSP\_LDO\_EN}$	M
L	LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	SD1_D0/ I2S1_DX/ GP[8]	SD1_CMD/ I2S1_FS/ GP[7]	USB_V_{DD1P3}	USB_DP	USB_V_{DDA3P3}	USB_V_{SSPLL}	USB_MXI	LDOI	LDOI	RSV0	L
K	LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX		V_{SS}	USB_VBUS	USB_V_{DDA1P3}	USB_R1	USB_V_{DDOSC}	USB_MXO		RSV3	V_{SSA_ANA}	K
J	LCD_D[7]/ GP[17]	SD0_CMD/ I2S0_FS/ GP[1]	LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK						CV_{DD}	RSV5	BG_CAP	GPAIN3	J
H	LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	DV_{DDIO}	SD1_D1/ I2S1_RX/ GP[9]		SD1_CLK/ I2S1_CLK/ GP[6]	USB_V_{SS1P3}	USB_V_{SSA3P3}	USB_V_{SSREF}		RSV4	ANA_LDOO	V_{SSA_ANA}	H
G	LCD_D[5]/ GP[15]	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]		SD1_D3/ GP[11]	V_{SS}	CV_{DD}	V_{SS}		LDOI	V_{DDA_ANA}	V_{SSRTC}	G
F	LCD_D[4]/ GP[14]	$\overline{TRST}$	V_{SS}		LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX		V_{SS}	GPAIN1		GPAIN2	RTC_XI	DV_{DDRTC}	F
E	LCD_D[3]/ GP[13]	LCD_D[2]/ GP[12]	LCD_D[6]/ GP[16]		SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}		V_{SSA_PLL}		V_{DDA_PLL}	RTC_XO	CLKIN	E
D	TDO	DV_{DDIO}	TMS		SD0_D0/ I2S0_DX/ GP[2]					CV_{DDRTC}	SDA	CLK_SEL	D
C	TCK	LCD_D[1]/ SPI_TX		V_{SS}		CV_{DD}	V_{SS}		V_{SS}		$\overline{INT1}$	CLKOUT	C
B	EMU1	LCD_RW_ WRB/ SPI_CS2	EMU0	TDI	CV_{DD}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	DV_{DDIO}	SCL	$\overline{INT0}$	B
A	LCD_EN_ RDB/ SPI_CLK	LCD_CS0_E0/ SPI_CS0	LCD_RS/ SPI_CS3	LCD_D[0]/ SPI_RX	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	$\overline{RESET}$	V_{SS}	A
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 1. C5545 Pin Map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	V_{SS}	LCD_D[4]/ GP[14]	LCD_D[6]/ GP[16]	$\overline{TRST}$	LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	LCD_D[7]/ GP[17]	LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	V_{SS}
N	TDO	LCD_RW_ WRB/SPI_ CS2	TCK	LCD_D[0]/ SPI_RX	LCD_D[3]/ GP[13]	TMS	LCD_D[5]/ GP[15]	DV_{DDIO}	CV_{DD}	LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	DV_{DDIO}	LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV_{DDIO}
M	EMU1	LCD_CS1_E1/ SPI_CS1	DV_{DDIO}	DV_{DDIO}	LCD_RS/ SPI_CS3	CV_{DD}	V_{SS}	SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}	SD0_CMD/ I2S0_FS/ GP[1]	LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	LCD_CS0_ E0/SPI_CS0	EMU0	LCD_EN_ RDB/ SPI_CLK	DV_{DDIO}	V_{SS}					V_{SS}	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	LCD_D[1]/ SPI_TX	TDI	V_{SS}	V_{SS}							CV_{DD}	RSV1	USB_V_{DD1P3}	USB_V_{SS1P3}
J	SD0_D0/ I2S0_DX/ GP[2]	LCD_D[2]/ GP[12]	XF									USB_V_{SSA1P3}	V_{SS}	USB_DM
H	RSV10	CV_{DD}	V_{SS}									USB_ V_{DDA1P3}	USB_V_{SSA3P3}	USB_DP
G	RSV9	RSV12	CV_{DD}									USB_V_{DDA3P3}	USB_V_{DDPLL}	USB_R1
F	RSV8	CV_{DD}	V_{SS}									USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DD1P3}
E	RSV7	RSV11	V_{SS}	V_{SS}							V_{SS}	USB_V_{DD1P3}	USB_V_{DDOSC}	USB_MXI
D	CLK_SEL	$\overline{RESET}$	CV_{DD}	V_{SS}	V_{SS}					V_{SS}	CV_{DD}	USB_V_{SSOSC}	USB_LDOO	USB_MXO
C	CLKIN	$\overline{INT0}$	DV_{DDRTC}	SCL	V_{SSRTC}	DV_{DDIO}	V_{DDA_PLL}	V_{SS}	V_{SSA_ANA}	BG_CAP	CV_{DD}	V_{SS}	$\overline{DSP\_LDO\_EN}$	LDOI
B	$\overline{INT1}$	V_{SS}	V_{SS}	CV_{DDRTC}	CV_{DDRTC}	V_{SSA_ANA}	V_{DDA_ANA}	GPAIN1	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V_{SSA_PLL}	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	GPAIN0	GPAIN2	GPAIN3	RSV4	RSV0	DSP_LDOO	V_{SS}

Figure 2. C5535 Pin Map

Some of the BGA package pin-out balls are located in the middle of the package as compare to the C5535 annotation. This approach allows easier board layout routing.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2016) to A Revision	Page
• Added industrial temperature to the TMS320C5545 in Table 1.	2

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