Application Note

VREFHI Driver Design for C2000 ADCs

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ABSTRACT

The analog-to-digital converter (ADC) is a key module used to sense feedback and monitor signals in real-time control applications. Without careful design and evaluation of the reference circuits for the ADC, however, significant AC and linear errors can occur, resulting in poor performance of the ADC sensing and thus the system. This application note identifies some common sources of these errors, and provides topologies that can be used in designs for C2000™ real-time microcontrollers.

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1 Introduction

For SAR ADCs, poor design of reference voltage circuits leads to inaccurate conversions of sampled signals. It is therefore necessary to evaluate the circuits that are driving the ADC References when designing a system that utilizes the ADCs included in C2000 real-time MCUs. This application report recommends a few reference circuit topologies and briefly highlights the ideas presented in the video series on ADC Reference Circuits by TI Precision Labs - Driving the reference input on a SAR ADC in the specific context of the ADCs on C2000 real-time MCUs.

1.1 Symptoms of an Unreliable Reference

C2000 device data sheets provide specifications for many aspects of ADC performance. These include linear specifications like INL, DNL, gain error, offset error. The data sheet also provides AC specifications such as SNR, THD and ENOB. Please refer to the *TI Glossary of Analog-to-Digital Specifications and Performance Characteristics* to see definitions for these specifications. When ADC performance is outside of these data sheet specifications, it can be difficult to find the source of the problem. For this reason, it can be helpful to know which errors are likely to be caused by a poor ADC voltage reference circuit.

For example, high gain error can be caused by an ADC reference voltage with DC error, since the voltage represented by each ADC code is different than the expected value. Conversely, dynamic errors can occur when the ADC reference voltage is unstable during fast changes in the load impedance. These concepts are discussed in detail in TI Precision Labs - Driving the reference input on a SAR ADC.

1.2 ADC Principle of Operation

Based on a given analog input voltage, the expected conversion result for a 12-bit single-ended C2000 ADC is given by the formula below.

$$\text{ADCRESULTx} = 4095\left(\frac{\text{ADCINy} - \text{VREFLO}}{\text{VREFHI} - \text{VREFLO}}\right) \quad (1)$$

For a single-ended 16-bit ADC, the expected conversion result is instead given by the formula below.

$$\text{ADCRESULTx} = 65535\left(\frac{\text{ADCINy} - \text{VREFLO}}{\text{VREFHI} - \text{VREFLO}}\right) \quad (2)$$

The expected conversion result for a 12-bit differential-ended ADC is given by the formula below. Notice that a differential conversion requires two inputs.

$$\text{ADCRESULTx} = 4095\left(\frac{\text{ADCINyP} - \text{ADCINyN} + \text{VREFHI}}{2\ \text{VREFHI}}\right) \quad (3)$$

For a differential-ended 16-bit ADC, the expected conversion result is instead given by the formula below.

$$\text{ADCRESULTx} = 65535\left(\frac{\text{ADCINyP} - \text{ADCINyN} + \text{VREFHI}}{2\ \text{VREFHI}}\right) \quad (4)$$

Most C2000 ADCs can operate in two different reference modes: internal and external reference modes. When the internal bandgap is chosen to generate the reference voltage for the ADC, the C2000 device itself drives a voltage out onto the VREFHI pin. In external reference mode, the VREFHI and VREFLO are driven by an external circuit. The VREFHI and VREFLO pins then set the ADC conversion range.

1.3 Layout Guidelines

VREFHI is sampled several times during each conversion of a SAR ADC, and high-current transients occur when the ADC's internal capacitor array is switched and charged as the bit decisions are made. VREFHI must remain stable and settle appropriately to avoid conversion errors. Because of these dynamic currents, the reference pin requires good decoupling using a high-quality bypass capacitor (C_{REF}). In the below figure, the inductance between the reference capacitor and the REF pin is minimized by placing the capacitor close to the pin and connecting it with wide traces. The design also uses a small 0.1-Ω series resistor (R_{REF}) to keep the overall impedance low and constant at high frequencies.

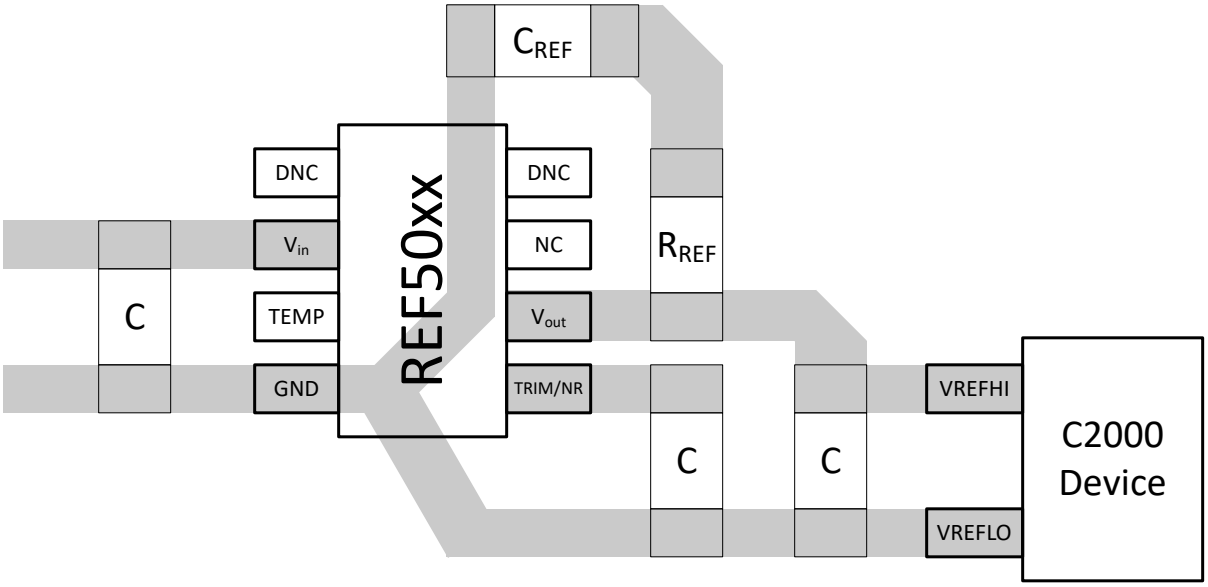


Figure 1-1. Example Layout

1.4 Key Reference Buffer Specifications

The term "reference buffer" is used to describe an amplifier placed between the reference IC and the ADC reference input. The reference buffer responds to very fast transient current requirements on the ADC reference input. Since a capacitor C_{bypass} is used between VREFHI and VREFLO, the ADC reference can draw current from this capacitor during the conversion of each bit, but the reference circuit needs to recharge the bypass capacitor between bit decisions. If the reference IC alone is unable to fully recharge the capacitor quickly enough, then a reference buffer is needed to preserve ADC performance.

The key specifications for the reference buffer are maximum output current, offset voltage, offset voltage drift, bandwidth, and output impedance across that bandwidth. For definitions of these terms, see *Understanding Operational Amplifier Specifications*. Low offset voltage and offset voltage drift are needed for DC accuracy across temperature. High bandwidth and low output impedance are needed to respond to fast transient current requirements. For more details, see TI Precision Labs - Driving the reference input on a SAR ADC.

1.5 VREFHI Example for C2000 MCUs

To illustrate the importance of ADC reference accuracy, this section presents a basic scenario in which the ADC reference has a DC error. If VREFLO= 0 V and VREFHI = 2.5V, then each of the 4096 possible codes of a 12-bit ADC represents a voltage of about .61mV.

If VREFHI is not at the expected voltage, the value of each ADC code is no longer .61mV. In an extreme case, if the ADC reference voltage unexpectedly drops to 2.4V, then each code represents a voltage range of about .59mV. If the ADC returns the code 4090, it appears to the user that the sampled voltage is almost 2.5V. The real input voltage is almost 100mV lower!

2 Unbuffered Reference

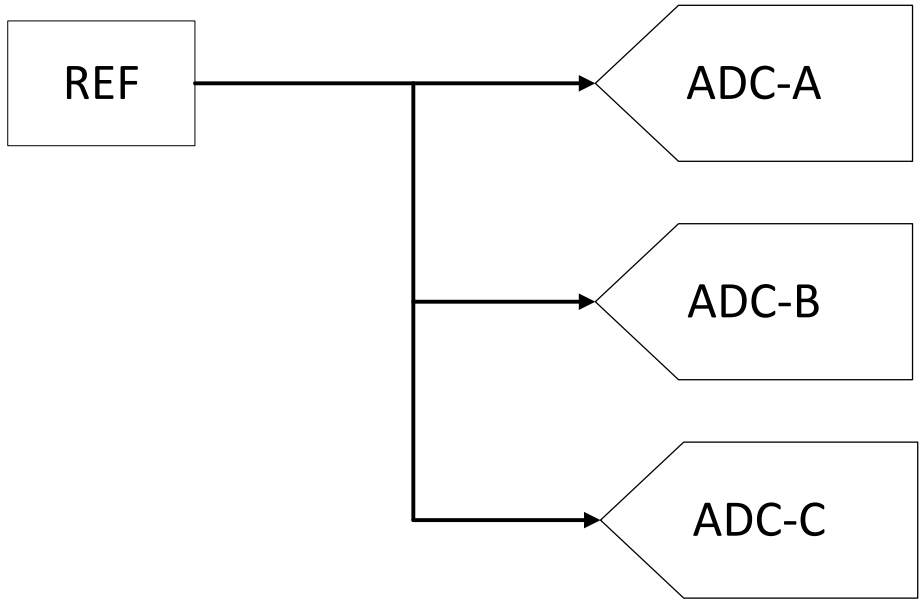
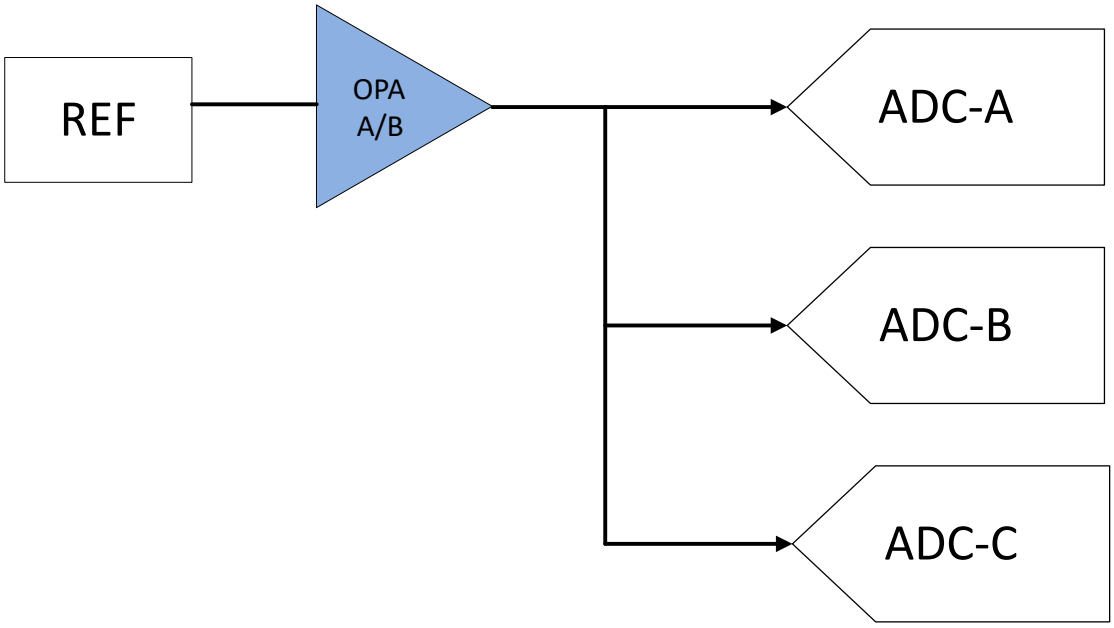


Figure 2-1. Unbuffered Reference

This topology uses a single voltage reference part to drive multiple C2000 ADCs. This topology is sufficient for driving up to three ADCs in 12-bit single-ended and differential modes. It is also acceptable for driving up to three 16-bit single-ended ADCs, but it is recommended to use a buffered reference to drive 16-bit differential ADCs. It is important to use a sufficient bypass capacitor on the output of the reference IC for the best performance.

3 Buffered Reference



REFERENCE PART OPTIONS:

REF35 (Recommended)

REF50xx

REF34

OP-AMP PART OPTIONS:

A:

OPA328 (Recommended)

OPA320

OPA350

B:

TLV365 (Recommended)

OPA322

Figure 3-1. Buffered Reference

This topology uses one voltage reference IC and a single precision OP-AMP to drive multiple ADCs. This topology provides the best performance for all C2000 ADCs. It is especially recommended to use this topology for 16-bit differential ADCs, since there will be a considerable performance difference between unbuffered and buffered reference circuits. It is also recommended to use this topology when driving more than three ADCs.

Note

The zero-crossover technology of the OPA328 makes it possible to accurately drive the output voltage close to the supply voltage of the OP-AMP. For most traditional rail-to-rail OP-AMPs, this can cause an unacceptable input offset voltage. For details, see *Reference-Buffer, ADC-Driver and Transimpedance Applications for OPAx328*.

The 'B' options for OP-AMPs provide a cost-effective alternative to precision OP-AMPs, where DC performance is traded for cost. These amplifiers are able to drive the reference when the ADC is sampling at high frequencies, but there can be a DC error of up to 2mV due to the amplifiers' input offset error.

4 VDDA as Reference Voltage for ADC

For C2000 devices without an internal reference, the cheapest option for VREFHI is to use VDDA as the reference. For C2000 devices with an internal reference, the internal reference is always a better performance option than using VDDA as the reference. Also, some low pin-count C2000 packages have VDDA as the only option to use for a voltage reference. In theory, it is possible to achieve good performance with VDDA as the reference, but in practice there are some common design decisions that can prevent this.

A common design decision that can limit performance is using an inaccurate low-dropout regulator (LDO) to directly supply VDDA, as many of these ICs supply an output voltage with a relatively large margin of error. A 10% margin of error in VDDA directly causes a 10% gain error in conversions. That results in a 400 LSB error for a full scale conversion!

Another key specification for the VDDA supply is transient response. Since VDDA is used to supply power to multiple analog peripherals in the device, there can be frequent changes in the load current sourced from VDDA. If the VDDA supply is not able to quickly resolve to the target voltage, this can cause large ADC conversion errors and overall poor dynamic performance. This problem can sometimes be alleviated by choice of capacitor at the VDDA pin, so make sure to carefully read the output capacitor recommendations for the IC that is supplying VDDA.

When using VDDA as a reference, it is possible to carefully design the input circuit so that ADC conversion errors are minimized. Key considerations for the VDDA supply circuit are DC accuracy, temperature drift, and transient response.

5 Summary

Reference voltage circuit design is an important consideration for systems where ADC accuracy is critical. Without a reliable reference circuit, users can see poor linear and dynamic performance, resulting in degraded sensing performance and accuracy.

By using the excellent resources provided by in the TI Precision Labs: TI Precision Labs - Driving the reference input on a SAR ADC, and the guidance in this application report, users can learn how and why to design an ADC reference circuit to achieve the performance shown in C2000 data sheets.

6 References

- TI Precision Labs - Driving the reference input on a SAR ADC
- Texas Instruments: *TI Glossary of Analog-to-Digital Specifications and Performance Characteristics*
- Texas Instruments: *Reference-Buffer, ADC-Driver and Transimpedance Applications for OPAx328*
- Texas Instruments: *ADC Input Circuit Evaluation for C2000 MCUs (using TINA-TI simulation tool)*
- Texas Instruments: *ASIL D Safety Concept-Assessed High-Speed Traction, Bi-directional DC/DC Conversion Reference Design*
- Texas Instruments: *Understanding Operational Amplifier Specifications*

7 ADC Related Collateral

Foundational Materials

- *ADC Input Circuit Evaluation for C2000 MCUs (TINA-TI) Application Report*
- C2000 Academy - ADC
- PSpice for TI design and simulation tool
- *Real-Time Control Reference Guide*
  - Refer to the ADC section
- TI Precision Labs - ADCs
- TI Precision Labs: Driving the reference input on a SAR ADC (Video)
- TI Precision Labs: Introduction to analog-to-digital converters (ADCs) (Video)
- TI Precision Labs: SAR ADC input driver design (Video)
- TI e2e: Connecting VDDA to VREFHI
- TI e2e: Topologies for ADC Input Protection
- TI e2e: Why does the ADC Input Voltage drop with sampling?
  - Sampling a high impedance voltage divider with ADC
- *Understanding Data Converters Application Report*

Getting Started Materials

- ADC-PWM Synchronization Using ADC Interrupt
  - NOTE: This is a non-TI (third party) site.
- Analog-to-Digital Converter (ADC) Training for C2000 MCUs (Video)
- *C2000 ADC (Type-3) Performance Versus ACQPS Application Report*
- *Hardware Design Guide for F2800x C2000 Real-Time MCU Series*
- *Interfacing the ADS8364 to the TMS320F2812 DSP Application Report*

Expert Materials

- *An Overview of Designing Analog Interface With TM320F28xx/28xxx DSCs Application Report*
- Analog Engineer's Calculator
- *Analog Engineer's Pocket Reference*
- *Charge-Sharing Driving Circuits for C2000 ADCs (using PSPICE-FOR-TI) Application Report*
- *Charge-Sharing Driving Circuits for C2000 ADCs (using TINA-TI) Application Report*
- Debugging an integrated ADC in a microcontroller using an oscilloscope
- *Methods for Mitigating ADC Memory Cross-Talk Application Report*
- TI Precision Labs: ADC AC specifications (Video)
- TI Precision Labs: ADC Error sources (Video)
- TI Precision Labs: ADC Noise (Video)
- TI Precision Labs: Analog-to-digital converter (ADC) drive topologies (Video)
- TI Precision Labs: Electrical overstress on data converters (Video)
- TI Precision Labs: High-speed ADC fundamentals (Video)
- TI Precision Labs: SAR & Delta-Sigma: Understanding the Difference (Video)
- TI e2e: ADC Bandwidth Clarification
- TI e2e: ADC Calibration and Total Unadjusted Error
- TI e2e: ADC Reference Driver Options
- TI e2e: ADC Resolution with Oversampling
- TI e2e: ADC configuration for interleaved mode
- TI e2e: Simultaneous Sampling with Single ADC
- *TMS320280x and TMS320F2801x ADC Calibration Application Report*
- *TMS320F2810, TMS320F2811, TMS320F2812 ADC Calibration Application Report*

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