Application Report
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# Calculating FIT for a Mission Profile

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**ABSTRACT**

This application report explains how use TI's reliability de-rating tools to calculate a component level FIT under power on conditions for a system mission profile.

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## 1 Introduction

Figure 1 shows the 'bathtub curve' model for reliability with three phases of reliability over time.

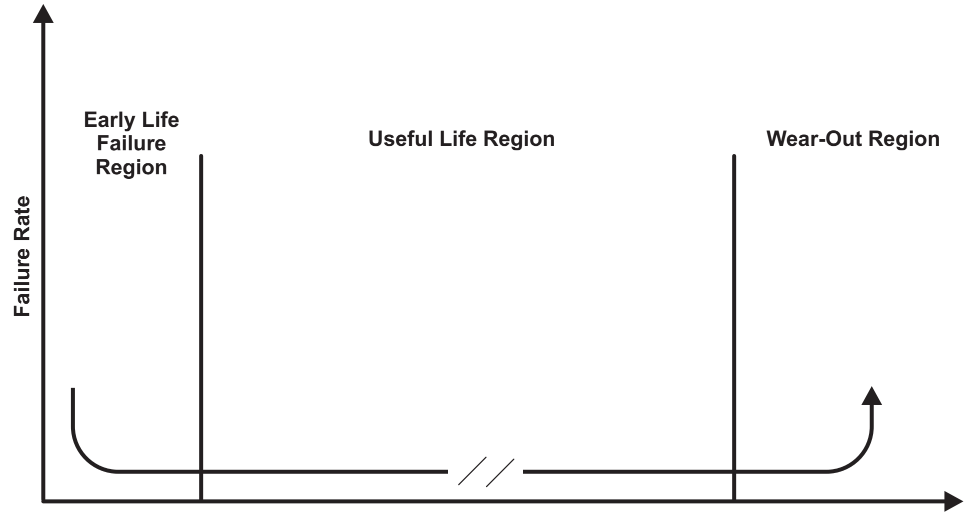


**Figure 1. Bathtub Curve Concept of Reliability**

- Early life (also known as infant mortality) – Characterized by declining failure rates and expressed in ppm. Usually attributed to manufacturing defects.
- Steady state and useful life – Constant failure rate (λ) expressed as FIT (number of failures/1E9 hours).
- Wear out – Characterized by increasing failure rate, but normally the onset of wear out should occur later than the target useful life of a system [1].

Assuming the part is operating within its useful life, which most systems will be, this document shows how to calculate an application-specific FIT for the TI semiconductor device under power-on conditions.

## 2 Where to Obtain FIT Rates?

The steady state FIT rate for a TI part number can be obtained from www.ti.com under the quality section → reliability estimator.

Figure 2 shows an example of TMS320F28355 device type (as of February 2015) where the FIT provided was 2.26 at 55°C assuming 60% statistical confidence level and 0.7eV.

Download Derating Tool | Download Spreadsheet | Definitions | Disclaimers

Search Results

| | Early Life Failure Rate | MTBF / FIT | | Early Life Failure Rate Supporting Data | | | | MTBF / FIT Suppor | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Part # | ELFR-DPPM | MTBF | FIT | Confidence Level (%) | Test Temp. (°C) | Sample Size | Number of Failures | Usage Temp. (°C) | Confidence Level (%) | Activation Energy (eV) | Test Temp. (°C) |
| TMS320F28335PGFA | - | 4.416* 10[illegible] | 2.26 | - | - | - | - | 55 | 60.0 | 0.7 | |

**Figure 2. Example of a FIT Number for TMS320F28335 (Feb 2015)**

(1) For more information on how to assess whether a TI Embedded Processor semiconductor is operating within the targeted useful lifetime of an end application, see [3].

A de-rating spreadsheet is available on the same location, which can be used to de-rate the FIT to different temperatures or confidence levels. Figure 3 shows the TMS320F28335 FIT de-rated to 0°C.

Note the FIT value scales with temperature where it changes from 2.26 FIT @ 55°C to 0.015 FIT@ 0°C.

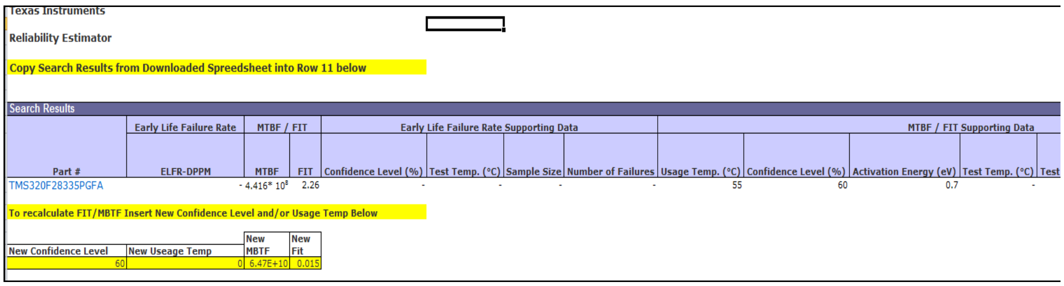


**Figure 3. Example of De-Rating FIT of 55°C Data**

## 3 Applying FIT to a Mission Profile

A common mistake of engineers unfamiliar with reliability modeling is to take the worst case FIT and apply that as the overall failure rate.

However, FIT is a failure rate (number of failures/1E9 hours) and not an absolute number and needs to be aggregated over the life of the product.

For reliability modeling, the mapping of time spent at different temperatures is known as a mission profile.

Table 1 provides an example of applying de-rated FIT data to an application mission profile. In this example, the overall FIT rate for the device was estimated to be 1.90. (Compare this to the worse case FIT at 85°C of 19.88 to which is only exposed for 2% of its lifetime.)

**Table 1. Example of Calculating FIT for TI Component in an Application**

| Ambient Temp ($T_A$) in °C | % Time | De-Rated Fit [(1)] | FIT × % Time |
|---|---|---|---|
| -5 | 2% | 0.01 | 0.0002 |
| 5 | 8% | 0.03 | 0.0024 |
| 15 | 10% | 0.08 | 0.008 |
| 25 | 15% | 0.21 | 0.0315 |
| 35 | 20% | 0.5 | 0.1 |
| 45 | 18% | 1.15 | 0.207 |
| 55 | 15% | 2.5 | 0.375 |
| 65 | 5% | 5.2 | 0.26 |
| 75 | 5% | 10.36 | 0.518 |
| 85 | 2% | 19.88 | 0.3976 |
| | | | **1.8997** |

(1) MSP430F5438AIPZ data using CL of 60% and Ea of 0.7eV using TI de-rating tool. Data obtained from www.ti.com on 10/29/2013.

## 4 Converting FIT to MTTF

Some customers may assess their reliability in terms of MTTF [2]. To convert FIT to MTTF is a simply inversion:

MTTF = 1E9/ FIT in the above example, 1.9 FIT would be 5.26E8 hours MTTF.

## 5 How are TI's FIT Numbers Derived?

JEDEC document JESD85 *Methods for Calculating Failure Rates in Units of FITs* [1] explains an electronic industry practice for calculating FIT.

The FIT is calculated from High Temperature Operational Life reliability studies and based on the Arrhenius equation for acceleration assuming a χ2 distribution as a reasonable approximation of the failure distribution over time.

Sample sizes for running HTOL vary from different qualification standards, but one example of AEC-Q100 grade 1 sample size would be 231 units subjected to HTOL out to 1000 hours @ 125°C $T_A$.

While JESD85 shows methodologies for assessing failures in time due to different fail mechanisms, for most modern day semiconductor technologies, the qualification acceptance is on 0 failures.

1. Calculate acceleration factor AF.

   Assuming a 125°C HTOL test, a common practice to gauge FIT is to de-rate to 55°C based on activation energy of 0.7eV.

$$
\begin{aligned}
AF &= \exp\left[\left(\frac{E_A}{k}\right)\cdot\left(\left(\frac{1}{T_{USE}}\right)-\left(\frac{1}{T_{STRESS}}\right)\right)\right] \\
&= \exp\left[\left(\frac{0.7\,eV}{8.6\cdot 10^{-5}\,eV/K}\right)\cdot\left(\left(\frac{1}{(55+273)\circ K}\right)-\left(\frac{1}{(125+273)\circ K}\right)\right)\right] \\
&= 78.6
\end{aligned}
$$

**Calculation of Acceleration Factor Example of 125°C to 55°C [JESD85]** (1)

2. Calculate upper confidence bound of failure rate.

   Use the formula in Equation 2 to calculate λ (FIT)

$$
\lambda_{CL} = \frac{X^2_{\%CL,2f+2}\cdot 10^9}{2\cdot t\, ss\cdot AF}
$$

**Formula to Calculate FIT [JESD85]** (2)

   where,
   - %CL = % Confidence level. (Typically 60% for industrial calculations)
   - f = number of failures,
   - t= number of hours of reliability testing
   - ss = sample size

Assuming 0 failures from 231 samples for 1000 hours HTOL @ 125°C, the FIT would calculate to be 50.9 FIT with 60% CL at 55°C.

(2) Mean Time To Failure (MTTF) is often used interchangeability with Mean Time Before Failure (MTBF). The difference is in a repairable MTBF and non-repairable failure MTTF. The assumption here is that the semiconductor is not repairable but, potentially, that the system could be de-soldered and replaced making the system repairable. It does not alter the mathematics for component fail rate. In addition, the exponential distribution used in calculating semiconductor steady-state FIT rates, MTBF = MTTF because the hazard rate of failures is independent of past failures (constant, not a function of time).

## 6 Questions and Answers of "FIT"

1. **Question 1**: The FIT numbers look high on your newer devices. How do I get lower FIT numbers?

   **Answer**: FIT values are a statistical confidence bound and a function of samples sizes. Equation 2 shows the impact of sample size to FIT for a 60% and 90% confidence levels.

**Table 2. Impact of 125°C HTOL Samples Sizes to FIT @ 55°C**

| Derating 125°C × 1000 hr HTOL to 55°C | | |
|---|---|---|
| Impact of 0 Failures and Sample Size | | |
| Sample Size | FIT @ 60% CL | FIT @ 90% CL |
| 231 | 50.9 | 127 |
| 461 | 25.5 | 64 |
| 922 | 12.8 | 32 |
| 1800 | 6.5 | 16.4 |
| 3600 | 3.3 | 8.2 |
| 5000 | 2.4 | 5.9 |
| 7500 | 1.6 | 3.9 |

   With increasing sample sizes, the upper confidence bound of the failure rate decreases but it never gets to be zero.

   The samples sizes and costs to demonstrate low FIT numbers eventually become prohibitive and have diminishing returns.

   This also illustrates one of the drawbacks of FIT as a projection of reliability: the actual numbers of failures in customer application may be zero but the statistical formula used is conservative. Even with no failures observed on reliability testing, the math of the Chi-square calculation introduces an uncertainty number based on the statistical confidence level, see Equation 2.

2. **Question 2**: Part number x has better FIT than part number *y*. Does that mean better reliability?

   **Answer**: Assuming both parts have zero failures to HTOL testing, the difference is one of statistical confidence levels: Part *x* likely had more devices tested, but you should note whether the activation energy used was the same.

   You should also note that FITs vary across technology. Newer technologies may have lesser samples submitted to HTOL, but yet their real life failure rates will likely be comparable since most modern semiconductors are designed to have intrinsic reliability where wear-out occurs much later than most customer applications.

3. **Question 3**: The de-rating is for $T_A$. How does this apply for devices specified in $T_J$?

   **Answer**: While calculating to $T_J$ would be technically correct for silicon reliability, the calculation of $T_J$ itself has uncertainty around it.

   TI normally runs HTOL at accelerated voltages (in excess of Vmax) in addition to accelerated temperature and the self-heating on HTOL is higher than the self-heating in a customer application. The AF given in FIT calculation only credits temperature acceleration where AF from voltage acceleration is not applied.

   De-rating ambient temperature should be sufficient for most reliability estimates.

4. **Question 4**: How does your example of mapping FIT to a mission profile differ from applying an overall effective acceleration factor?

   **Answer**: They are essentially doing the same calculation and methodology is the equivalent.

$$Af_{Eff} = \left( \frac{a_1}{AF_{T1}} + \frac{a2}{AF_{T2}} + \frac{a3}{AF_{T3}} + \cdots + \frac{aN}{AF_{TN}} \right)^{-1} = \left( \sum_{i=1}^{N} \frac{a1}{AF_{T1}} \right)^{-1}$$

*where $a_1$ is the fraction of the mission profile time to $T_i$*

**Calculation of Effective Acceleration Factor [2]** (3)

5. **Question 5**: What happens to FIT at higher temperature, for example, above 85°C $T_A$?

   **Answer**: The FIT rate increases with temperature, you should aggregate the time spent at the higher temperature.

   However, the total time spent at higher temperatures should be minimized as higher temperatures potentially shorten the useful life of a semiconductor. [(1)] Assuming that it is still operating within its useful life, the steady state FIT can be used.

   Implicit in operating at higher temperature is that the device-specific data sheet supports that temperature range.

(1) Time at high temperatures influence the onset of wear out mechanisms and once the part is moves into the wear out stage of reliability model, the steady state FIT rate no longer applies and advanced reliability modeling is required. For more information, see*Calculating Useful Lifetimes of Embedded Processors* (SPRABX4).

## 7 Limitations of This Document

- For limitations of TI reliability estimates, see www.ti.com.
- The FIT values are for semiconductor reliability under power-on conditions only (silicon lifetime). It does not include assessment of package reliability conditions that needs separate reliability assessments.
- Data retention periods of non-volatile memories are not considered in this document. For those values, see the device-specific data sheets.

## 8 References

1. JESD85 *Methods for Calculating Failure Rates in Units of FITs*, which is located at: www.jedec.org
2. *Applied Reliability* (3rd Ed.), pg 244-245, Tobias and Trindade, CRC Press, 2012
3. *Calculating Useful Lifetimes of Embedded Processors* (SPRABX4)