Distortion and source impedance in JFET-input op amps

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Designers of low-distortion analog circuits in industrial data acquisition, seismic measurement, and high-fidelity audio are aware that many operational amplifiers (op amps) produce greater distortion when configured as non-inverting amplifiers. In the non-inverting configuration, the input signal appears as a common-mode signal at both inputs. The subtraction performed by the op amp on the two inputs is finite and slightly non-linear, producing a small amount of additional distortion at the op amp output. This effect is often referred to as common-mode distortion.[1]

It is less widely known that some op amps show more severe common-mode distortion when the input-signal source has a high output impedance. Using the TL072, a JFET-input general-purpose op amp, let's compare the output distortion for two source impedances. Figure 1 shows the TL072's output distortion when the source impedance is 20 Ω and 10 kΩ. The total harmonic distortion and noise (THD+N) is substantially increased in the 10-kΩ case – more than could be attributed to the additional source resistor.

This behavior is typical of older JFET-input op amps like the TL072 and limits their usability in many circuits such as Sallen-Key active filters.[2] At the time, JFETs offered some advantages over bipolar transistors when used as the input devices of an op amp. For example, the reduced current noise allowed JFET-input op amps to be used in high-impedance applications. Furthermore, JFETs could be fabricated with the existing bipolar semiconductor processes, giving them a major advantage over MOSFETs.

Figure 2 shows the cross section of a p-channel JFET fabricated using ion implantation on a p-type substrate in a junction-isolation process.[3] The channel was formed by implanting p-type impurities into an n-type region. An n-type region is then implanted on top of the channel (n-type top gate) and connected to the region below the channel to form the gate.

The junction between the p-type substrate and n-type gate acts as a reverse-biased diode. This allows the JFET to have extremely low input current, while creating a parasitic capacitance (C_{GSS}) from the gate to the substrate.

At the interface of p-type and n-type semiconductor material, a process of diffusion occurs where electrons and holes migrate across the interface leaving behind charged ions on their respective sides. The migrating charge carriers recombine with the opposing charge carriers from the opposite side and are eliminated, which produces an area with no mobile charge carriers. This area is called the depletion region because the mobile charge carriers have been depleted. In this region, the semiconductor material behaves as an insulator. The resulting structure resembles a capacitor with n- and p-type regions being the conductive electrodes, and the depletion region acts as the dielectric. Due to the large contact area between the gate

Figure 1. THD+N measurement of a TL072 op amp

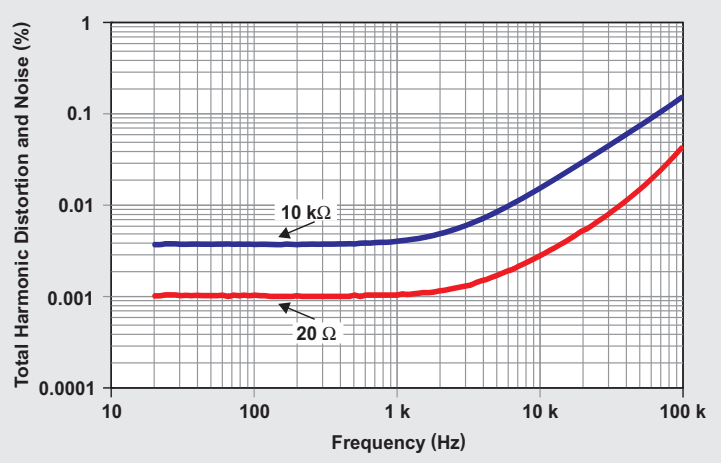
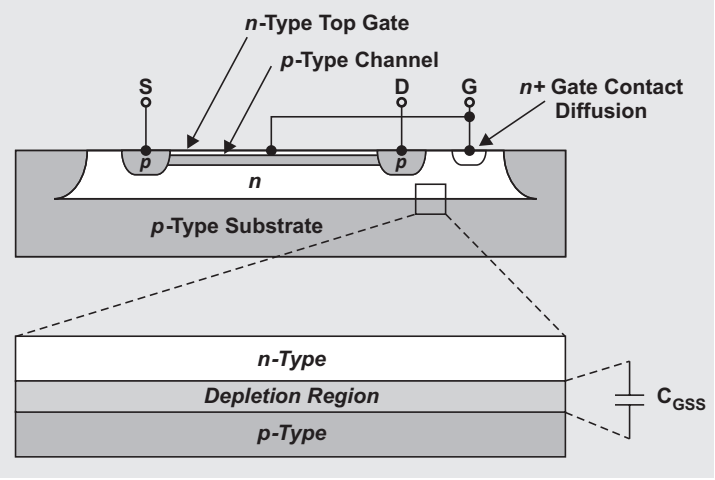


Figure 2. Ion-implanted p-channel JFET structure



and the substrate, the gate-to-substrate capacitance, C_{GSS}, is typically much larger than the gate-to-source and gate-to-drain capacitances.[3] Therefore, the C_{GSS} of the input JFETs is the dominant contributor to the input common-mode capacitance of these op amps.

Like all capacitors, the capacitance of the p-n junction is dependent on the area of its electrodes and the distance they are separated. Although the area of the junction is fixed, the width of the depletion region is not. It depends on the direction and intensity of the electric field across the depletion region.

During the initial diffusion, the ions left behind by the diffusing charge carriers produce an electric field which opposes further diffusion. This is called the built-in voltage of the junction. The application of an external voltage to the junction has the effect of growing or shrinking the width of the depletion region and changing the capacitance of the junction. The gate-to-substrate capacitance of a JFET varies as a function of gate-to-substrate voltage according to the equation:

$$C_{GSS} = \frac{C_{GSS0}}{\sqrt{1+\frac{V_{GSS}}{\psi_0}}} \quad (1)$$

In Equation 1, C_{GSS0} is the junction capacitance at 0 V, V_{GSS} is the gate-to-substrate voltage. Further, ψ_0 is the built-in voltage of the junction, which typically is about 0.7 V. In most op amps, the substrate is held at the negative supply voltage (V_{EE}). Therefore, as the common-mode voltage changes, the V_{GSS} term in Equation 1 changes, which increases or decreases the gate-to-substrate capacitance, C_{GSS}.

In Figure 3, input common-mode capacitances, C_{CM1} and C_{CM2}, were added to represent C_{GSS} of the input JFETs.

The input common-mode capacitance of the non-inverting input, C_{CM1}, must be charged and discharged by a small current, I_S, from the input source, V_S. If the input capacitance is not a constant, but depends on the input voltage, the charging current drawn from the source is no longer linearly related to the rate-of-change of the input voltage signal:

$$I_S \neq C_{CM1}\frac{dV_S}{dt} \rightarrow I_S = \frac{C_{GSS0}}{\sqrt{1+\frac{V_{IN}-V_{EE}}{\psi_0}}} \times \frac{dV_S}{dt} \quad (2)$$

This behavior is similar to the voltage coefficient of discrete ceramic capacitors.[4,5] The change in capacitance with applied voltage distorts the current in the capacitor. This distorted current drawn from the source produces a distorted signal at the op-amp input due to the voltage drop across R_S.

$$V_{IN} = V_S - I_S R_S \quad (3)$$

It is possible to cancel this distortion by placing a resistance equal to the source impedance in the op amp's feedback loop. This produces an identical distortion signal at the op amp's inverting input. Because the distortion is now common to both inputs, it is removed by the op amp's common-mode rejection. Unfortunately, the resistance in the feedback path introduces additional noise and also can cause stability issues if it is very large.[6]

Figure 3. The varying common-mode capacitances of a JFET-input op amp

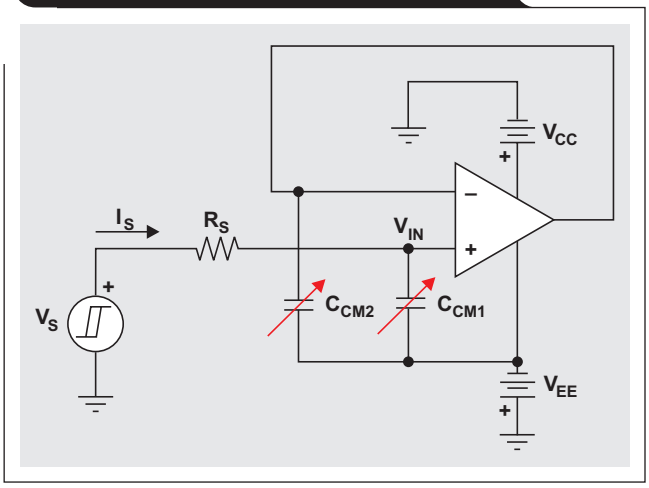
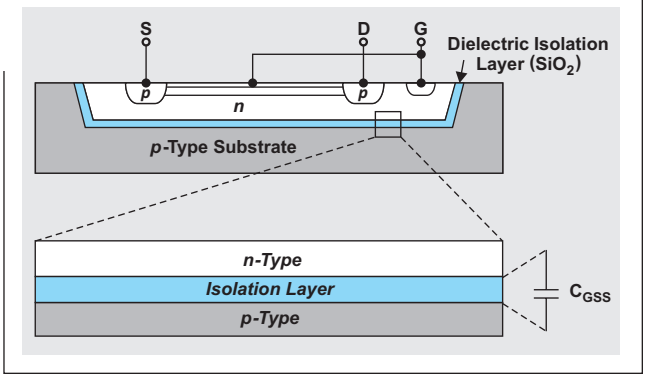


Figure 4. The isolation layer in DI processes



Ideally, to preserve low distortion when operating with high source impedances, the input common-mode capacitance needs to be stabilized to a constant value. One method to accomplish this is to fabricate the op amp with a dielectrically isolated (DI) process. As shown in Figure 4, DI processes use a layer of dielectric material, such as silicon dioxide (SiO_2), to isolate devices from the substrate and other adjacent structures. These processes were originally introduced to improve the speed of on-chip transistors by reducing the capacitance at their collectors.[3]

An additional benefit of dielectric isolation is that the JFET's gate-to-substrate capacitance no longer varies with the input common-mode voltage. The value of the gate-to-substrate capacitance is determined by the size of the device and width of the isolation layer, which is completely unaffected by an applied electric field. Furthermore, the isolation layer prevents the diffusion of charge carriers across the p-n interface that would form a depletion

region. There is still an electric field across the barrier, but its effect on the mobile charge carriers in the silicon is not large enough to affect the total capacitance.

In Figure 5, the common-mode capacitance of two op amps was measured very precisely with a network analyzer. The TL072 op amp was fabricated with a standard junction-isolated process. Over the measurement range, the input common-mode capacitance varies from 4.87 pF at +10 V to 7.10 pF at –10 V, a total change of 2.23 pF. As expected, the input common-mode capacitance increases with negative common-mode voltages because the gate-to-substrate voltage is decreasing.

Alternatively, the OPA1642 was fabricated with a DI process. The input common-mode capacitance is greatly stabilized and shows a variation of only 30 fF over the entire measurement range.

The improved stability of the input common-mode capacitance is immediately apparent in distortion measurements. Figure 6 shows the measured THD+N of the OPA1642 configured in a gain of +1 for source impedances of 20 Ω and 10 kΩ. Unlike the TL072, the distortion of the OPA1642 is unaffected by an increase in source impedance.

The need for JFET-input op amps is still prevalent today because they continue to offer a unique combination of low noise, low bias current, and excellent AC/DC performance. The introduction of DI processes in their fabrication and the resulting stabilization of the input capacitance allow modern JFET-input op amps to achieve extremely low distortion regardless of source impedance.

Figure 5: Common-mode capacitance of two JFET-input op amps

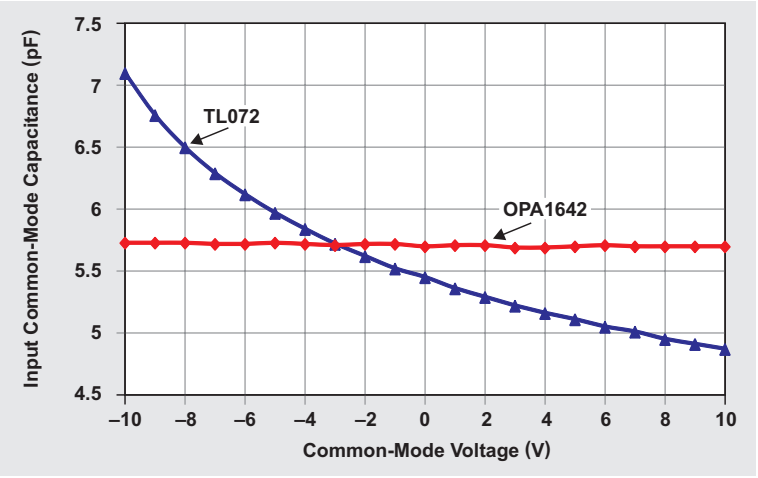
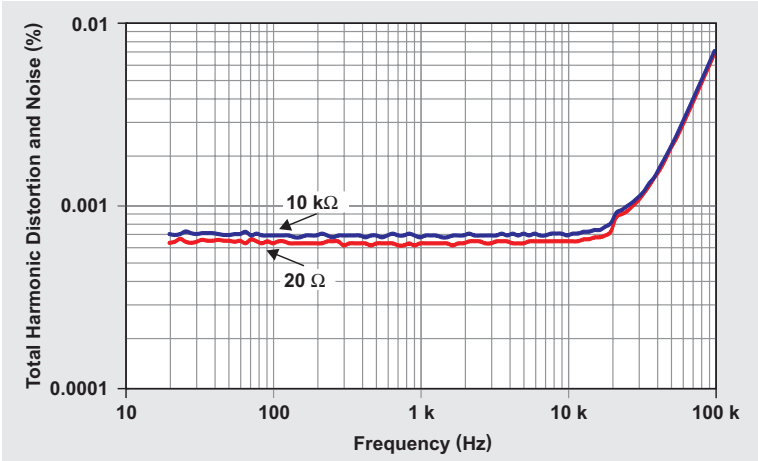


Figure 6. THD+N measurements of an OPA1642 op amp



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