Application Report
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Driving High-Speed Analog-to-Digital Converters: Circuit Topologies and System-Level Parameters

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ABSTRACT

This application report discusses the performance-related aspects of passive and active interfaces at the analog input of high-speed pipeline analog-to-digital converters (ADC). The report simplifies the many possibilities into two main categories: passive and active interface circuits. The first section of the report gives an overview of equivalent models of buffered and unbuffered ADC input circuits, passive interfaces based on transformers, as well as an overview of the metrics used to gauge the ADC analog performance in addition to the entire mixed-signal chain. Passive interfaces are frequently the best choice when there is flexibility in the applied signal level and signal loss in the interface is a non-issue. While the noise and distortion contributions of passive interfaces can be negligible, the inherent frequency-dependent power loss, passband ripple, low frequency limitations (for example, ac coupling), and cost can limit the usefulness of these interfaces.

The second section of the report covers interface circuits using high-speed operational amplifiers and fully-differential amplifiers. High-speed amplifiers can provide flexible, cost-effective solutions when the application demands gain, a flat passband with low ripple, dc level shifts, or a dc-coupled signal path. The second section covers amplifier-specific performance metrics, common circuit topologies for high-speed amplifiers, and some detailed performance models that can help pick the best amplifier to achieve the desired combined (that is, an amplifier + ADC) performance.

Contents

List of Figures

1 Analog Input Topologies of High-Speed Pipeline ADCs

Today's CMOS and bipolar high-speed, analog-to-digital converters (ADCs) usually have pipeline architectures, but can have different analog input circuit topologies. CMOS ADCs (for example, the ADS55xx and ADS61xx series devices) have unbuffered inputs where the sample-and-hold circuitry is directly connected to the analog input pins. Bipolar ADCs (such as the ADS54xx series devices), on the other hand, usually have analog inputs that are isolated from the sample-and-hold circuitry by an internal amplifier. Both types of high-speed ADCs often have input bandwidths much greater than the maximum sampling frequency and are capable of undersampling narrowband input signals. The following sections cover the equivalent input circuit models and major performance metrics for these types of high-speed ADCs.

2 High-Speed Pipeline ADCs with Unbuffered Analog Inputs

The equivalent model of an analog input from the ADS6444 data sheet is shown in Figure 1 as an example of an unbuffered input stage. The analog input consists of a switched-capacitor-based, differential, sample-and-hold (S/H) architecture. Note that the FET which serves as a sampling switch is the only active device between the analog input pins and the sampling capacitor. This device controls the charge flow from the analog input pins into the sampling capacitor. The RLC networks that contain the L_{pkg}, C_{bond},and R_{esr}, are equivalent models of the package and bond-wire parasitics. The RCR filter sets the analog bandwidth of the device. The FETs control the charge and discharge of the sampling capacitors.

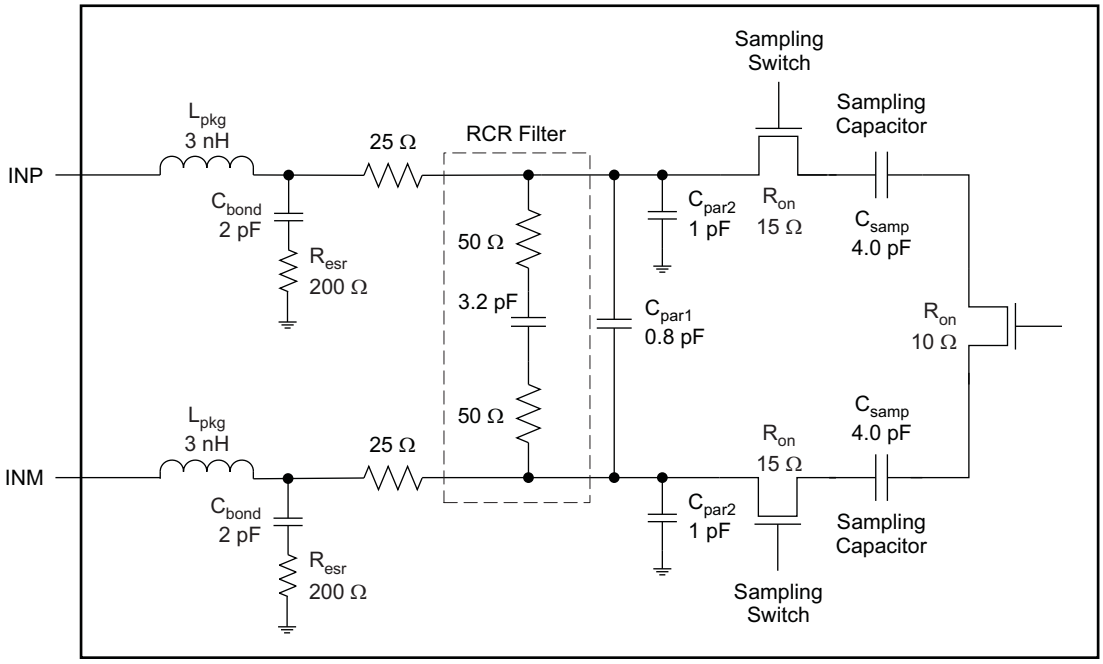

Figure 1. Example of an Equivalent Model of an Unbuffered Analog Input

The differential input topology results in good ac performance for high input frequencies at high sampling rates. The input sampling circuit of the ADS6149 has a high, –3-dB bandwidth that extends up to 700 MHz (measured from the input pins to the sampled voltage).The INP and INM pins must be externally biased around a common-mode voltage that is available as a reference voltage on the ADC VCM pin. For a full-scale differential input, each input pin INP, INM pair must swing symmetrically between VCM ±V_{PEAK}. In general, this architecture results in a full-scale, differential, peak-to-peak input swing of 4 x V_{PEAK}, where V_{PEAK} is the peak voltage at either input pin. As an example, the ADS6149 has a differential full-scale input voltage of 2 V_{PP}, which is the result of a peak swing of ±0.5 V (at INP, INM) about the 1.5-V common-mode voltage.

3 Unbuffered Analog Input Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. It is also necessary to present low impedance (<50 Ω) for the common-mode switching currents. For example, this is achieved by using two resistors from each input terminated to the common-mode voltage (VCM), as shown in Figure 2.

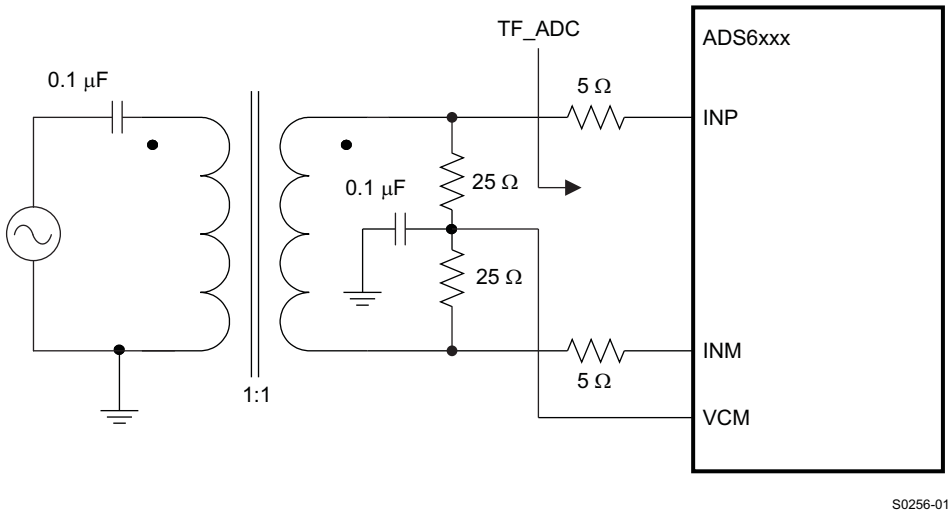

Figure 2. Example of a Passive Single Transformer Drive Circuit for an Unbuffered Analog Input

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high-frequency input signals. Figure 3 shows an example using two transformers (for example, a Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the shaded box in Figure 3) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground to ensure optimal balance.

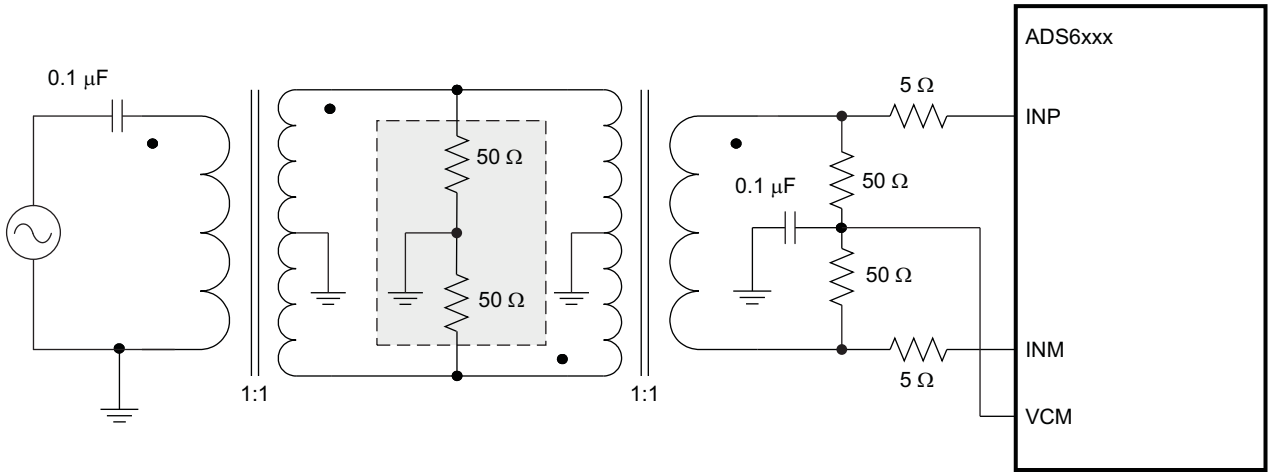

Figure 3. Example of a Passive Dual Transformer Drive Circuit for an Unbuffered Analog Input

In addition to the preceding considerations for unbuffered ADC inputs, the drive circuit may also have to provide:

1. Low insertion loss over the desired frequency range;
2. Input impedance that is matched to the signal source; and
3. Output impedance that matches the ADC input.

For all of these reasons, the ADC input impedance must be taken into account when designing the drive circuit. Figure 4 (from the ADS6444 product data sheet) shows that the impedance (Z_{IN}, looking differentially into the ADC input pins) decreases at high input frequencies. A Smith chart representation of the differential input impedance shows that the input impedance is capacitive over the operating band and can be approximated by a series R-C up to about 500 MHz.

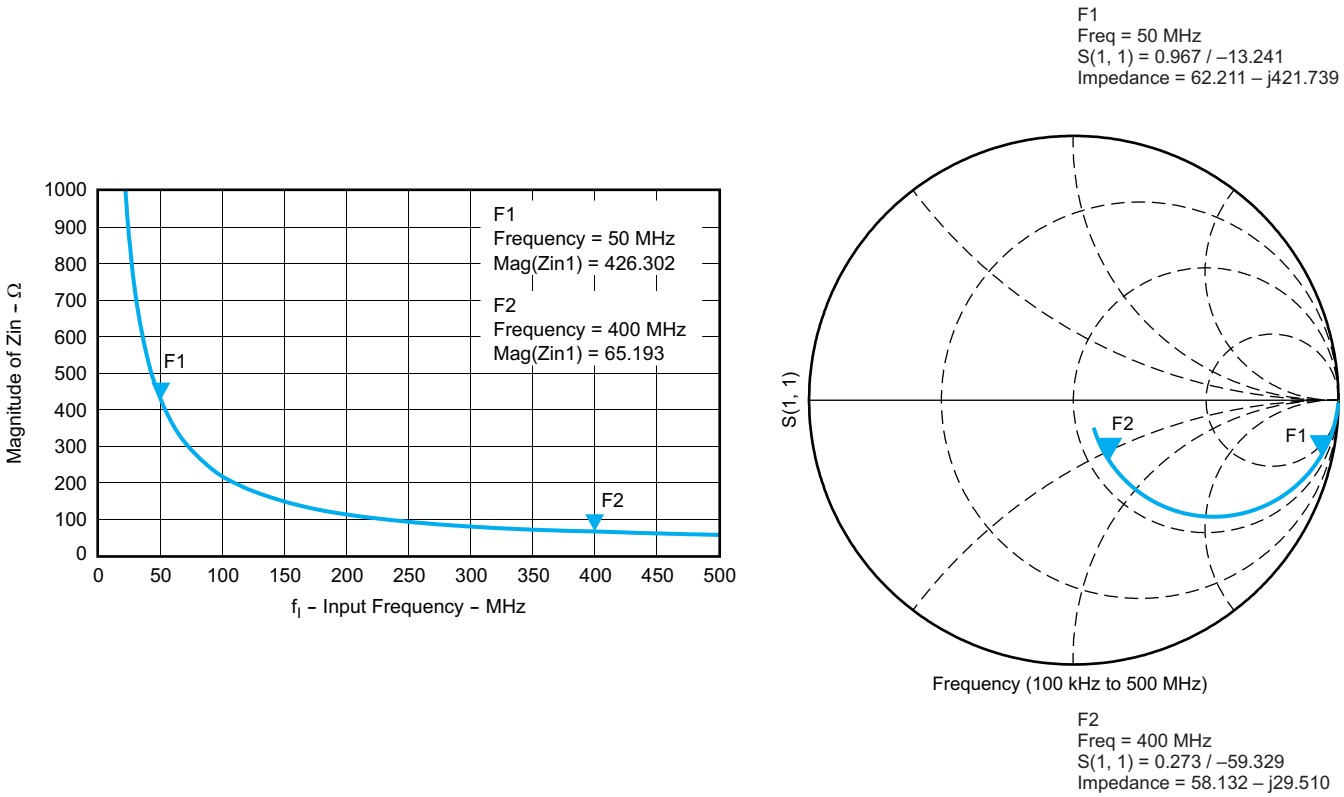

Figure 4. Differential Input Impedance vs Frequency for an Unbuffered Sample-and-Hold Input

4 Buffered Analog Input Equivalent Circuit Model

The equivalent model of a buffered analog input is shown in Figure 5, taken from the ADS5483 device data sheet. The ADS5483 is a fast, 16-bit, bipolar ADC. When an analog signal is applied to the device input pins, it first passes through high-performance bipolar buffers before it is sampled by the track-and-hold circuit. The buffer isolates the board circuitry external to the ADC from the sampling glitches caused by the track-and-hold within the ADC. The buffers also present high impedances to the analog inputs that are relatively constant over the usable bandwidth, unlike devices with unbuffered inputs. The conversion process is initiated by the falling edge of the external input clock. At that instant, the differential input signal is captured by the input track-and-hold, and the input sample is converted sequentially by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. For the 16-bit ADS5483, this process results in a data latency of 4.5 clock cycles, after which the output data are available as a 16-bit parallel word, coded in offset binary format.

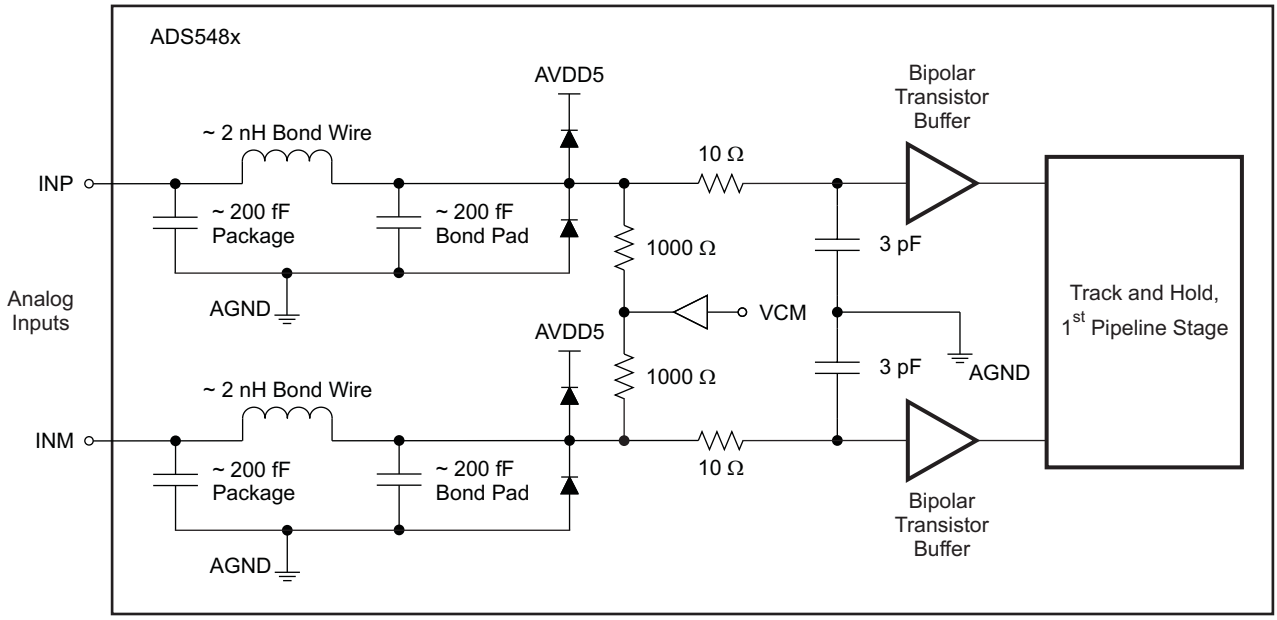

Figure 5. Example of an Equivalent Model of a Buffered Analog Input

The input common-mode of a buffered device is frequently set through internal resistors connecting each input signal path to the common-mode reference VCM. In the example (Figure 5), this configuration results in a differential dc input impedance of 2 kΩ. In contrast, unbuffered inputs frequently require external biasing circuitry to provide the common-mode voltage.

For the example shown in Figure 5 based on the ADS5483, a full-scale differential input is represented by each input pin swinging symmetrically between 3.1 V ±0.75 V. This range means that each input has a maximum signal swing of 1.5 V_{PP} for a total differential input signal swing of 3 V_{PP}. Note that other converters may have different values for the full-scale input swing and/or the input common-mode voltage.

5 Buffered Analog Input: Drive Circuit Requirements

In the same way as unbuffered ADCs, buffered ADCs perform optimally when the analog inputs are driven differentially. Figure 6 shows one possible configuration that uses an RF transformer to convert the output of a single-ended RF signal generator into a balanced differential signal that is applied to the ADC. The 200-Ω resistor between INP and INM serves as a matching component and current path for the applied signal. Using a higher value resistor may result in degraded performance.

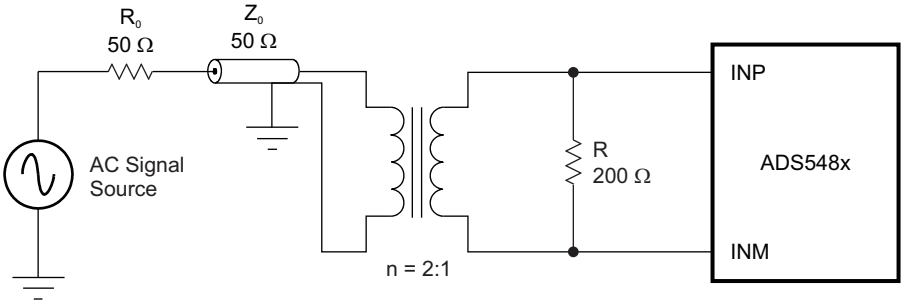

Figure 6. Example of a Passive Transformer Drive Circuit for a Buffered Analog Input

As mentioned previously, the high-performance buffers that precede the track-and-hold circuit present input impedances which are relatively constant over the usable frequency range of the device. As a result, the overall input impedance of the ADC is dominated by the input bias circuit and the small buffer input capacitors (that is, the 1000-Ω resistors and 3-pF capacitors in Figure 5), and not the characteristics of the track-and-hold. The reverse isolation of the buffer amplifiers minimizes common-mode currents generated by the track-and-hold switching; therefore, two-transformer configurations are often not required to achieve optimum performance. The net effect of the input impedance and minimized common-mode transients is that the input circuitry is simplified compared to the unbuffered inputs.

6 High-Speed A/D Performance Metrics

Performance metrics in high-speed systems generally emphasize frequency-domain parameters for signal, distortion, and noise. Time domain parameters such as settling time and acquisition time are also considerations, but they tend not to be primary parameters that are considered during system definition and in related discussions. In addition, static precision-related parameters such as integral nonlinearity (INL) and differential nonlinearity (DNL) can be critical parameters in some systems, but they are often not a primary concern in many of today's high-speed systems. For this reason, and because of space considerations, this application report concentrates on performance metrics such as signal-to-noise ratio (SNR) and other metrics related to nonlinear distortion. The brief descriptions are included here to facilitate the high-speed discussion in the subsequent sections.

Analog Bandwidth—Defined as the analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value. It also serves as a measure of the analog signal integrity versus increasing frequency. High-speed data converters are frequently used in digital radio applications to convert narrowband IF signals with carrier frequencies in the second or third Nyquist zones where the input signal frequency is near or above the sampling frequency. If the signal chain has an appropriate degree of filtering, the signal does not alias onto itself, but an inadequate analog-to-digital (A/D) analog bandwidth degrades the desired signal, and possibly leads to degraded SNR and SFDR. Figure 7 (from the data sheet for the ADS5481/2/3 series of ADCs) illustrates the variability of the analog bandwidth within a product family.

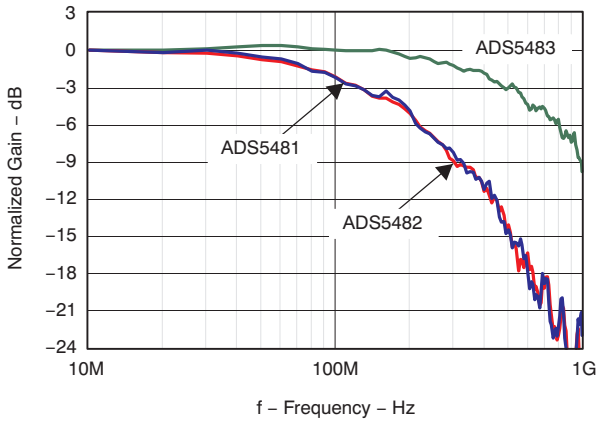

Figure 7. Analog Input Response of the ADS5481/2/3 Family

Signal-to-Noise Ratio (SNR)—In high-speed ADC data sheets, SNR is expressed as the ratio of the power of the fundamental (P_S) input to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10\log_{10}\left(\frac{P_S}{P_N}\right) \quad (1)$$

SNR is either given in units of dBc (dB relative to the carrier) or dBFS (dB relative to the A/D full-scale). In dBc units, the total *measured* noise is expressed relative to the *measured* carrier level. In dBFS units, the *measured* noise is expressed as relative to the A/D full-scale level, but the measurement is usually executed with a carrier level –1 dB below the A/D full scale (for example, –1 dBFS). SNR expressed in dBFS units is frequently used when defining system requirements because it represents a maximum noise-limited dynamic range; or alternatively, the effective noise floor of the converter device.

See Figure 8 for a contour plot of the ADS5483 SNR with input frequency and sampling frequency as the plotting variables. The plot shows that the best SNR performance occurs when input frequencies are in the first Nyquist zone, and that SNR degrades by only 3 dB when the input frequency moves to the third Nyquist zone, which matches the behavior shown in Figure 7 of analog bandwidth.

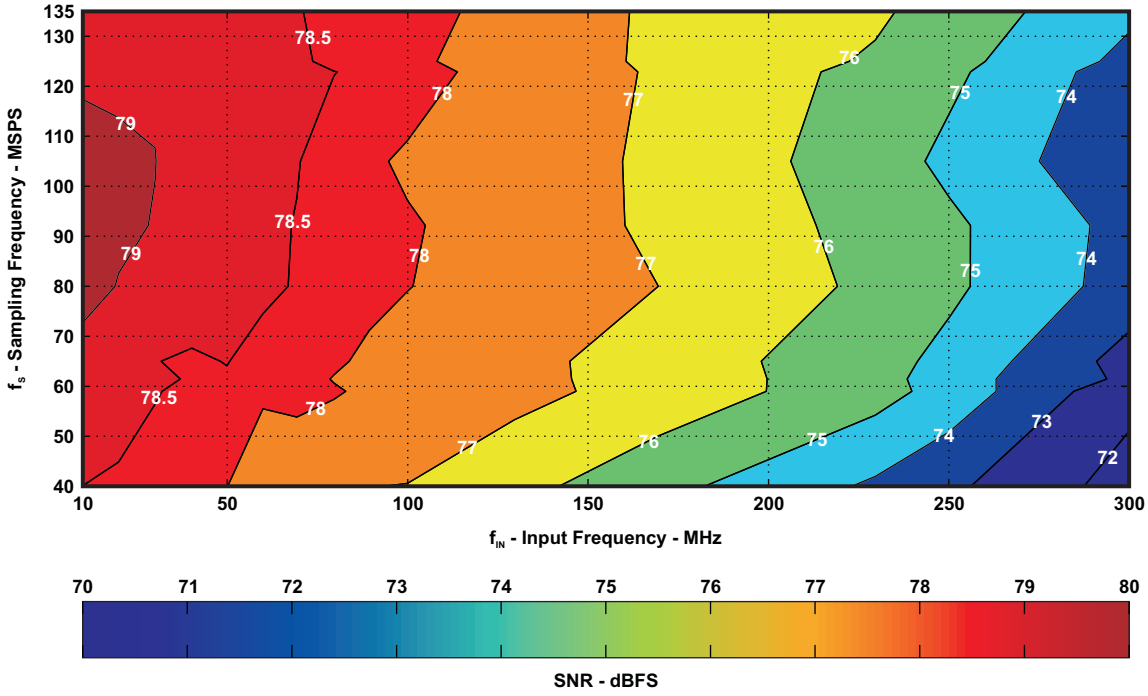

Figure 8. ADS5483 SNR (in dBFS): Contour Plots with Sampling Frequency vs Signal Input Frequency

Spurious-Free Dynamic Range (SFDR)—The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier). A contour plot of SFDR versus input frequency and sampling frequency as the plotting variables is shown in Figure 9 (taken from the ADS6445 data sheet).

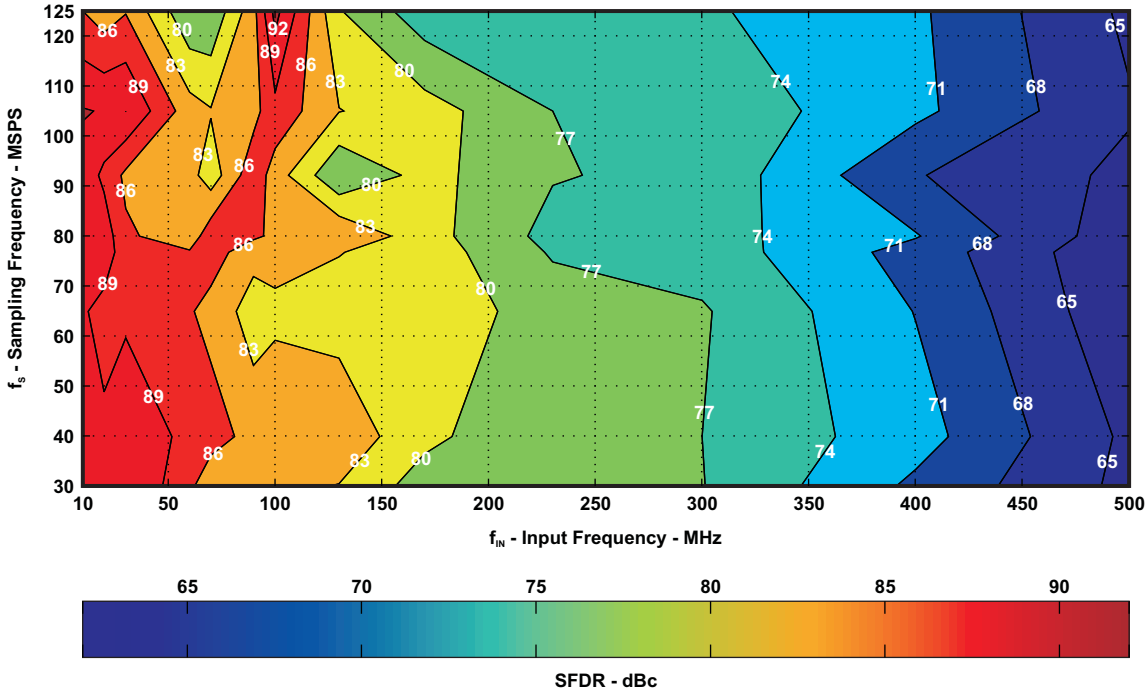

Figure 9. ADS6445 SFDR: Contour Plots with Sampling Frequency vs Input Signal Frequency

Third-Order Intermodulation Distortion (IMD3)—IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB relative to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

7 Examples of Active Drive Circuit Topologies for High-Speed ADCs

Many times, a driver amplifier is required to meet the signal chain requirements. These factors include, but are not limited to:

- Gain
- DC-coupled signal path.
- Buffering of the signal source
- Conversion of a single-ended signal path to a differential signal path
- Level shift

If a driver amplifier is needed, its parameters can have a major impact on the overall performance of the system formed by the amplifier and the converter. The next section describes major amplifier metrics and how they affect the overall amplifier/converter performance. Subsequent sections describe various circuit architectures as well as other design and performance considerations.

8 Amplifier Performance Metrics

Small-Signal Bandwidth

Small-signal bandwidth is a measure of the ability of a device to act as a linear gain element over a defined frequency span. It is implicitly assumed that the signal level is small enough that its presence does not change the operating point of the amplifier; this metric also serves as the noise bandwidth of the amplifier. It is related to the small-signal rise and fall times via the relationship expressed in Equation 2:

$$\tau_{SS} = \frac{0.35}{f_{-3dB}} \tag{2}$$

where f_{-3dB} is the –3dB small-signal bandwidth.

Slew Rate/Large-Signal Bandwidth

Slew rate is defined as the maximum $\Delta V_{OUT}/\Delta t$ for a specified gain, output level, and R_{LOAD}. As a large-signal parameter, it represents the maximum possible speed of the device as it moves through its dynamic range. Slew rate measurements are frequently done by measuring the rising and falling edges of a large-signal pulse waveform. In these cases, the measurement range for ΔV_{OUT} is the voltage deflection that covers 10% to 90% of the rising edge of the output waveform (or 90% to 10% of the falling edge). Slew rate is a large-signal parameter, and is unrelated to small-signal rise and fall times. *Slew rate limiting* is distortion caused by transitions of the input signal that are too fast for the amplifier output to track. Recall that during normal operation, an op amp acts as a closed-loop device that feeds back some of the output signal in an attempt to minimize an error signal. When the amplifier is slew-limited, the amplifier output can no longer track the input signal. Consequently, the feedback mechanism breaks down, which in turn allows the error signal to increase along with a subsequent increase in signal distortion. For all intents and purposes, the slew-limited device is operating as an open-loop amplifier with degraded distortion performance.

For the limiting case of a sinusoidal signal, $V_{OUT} = A\cos(2\pi f t + \theta)$, the slew rate can be expressed in terms of the large-signal bandwidth through the following relationships:

$$SR = \left(\frac{\Delta V_{OUT}}{\Delta t}\right)_{MAX} \Rightarrow \left(\frac{dV_{OUT}}{dt}\right)_{MAX} = \left(\frac{d}{dt}\left[A\sin\left(2\pi f t + \theta\right)\right]\right)_{MAX}$$
$$= \left(2\pi f A\cos\left(2\pi f t + \theta\right)\right)_{MAX} \tag{3}$$

If the input sinusoid frequency increases while holding the input peak amplitude constant, the slew rate is maximized when the frequency equals the large-signal bandwidth, which corresponds to a 3-dB decrease in the output signal (that is, $f = f_{-3dB}$, $V_{O,Peak} = A/\sqrt{2}$). The slew rate is related to the –3-dB large-signal bandwidth as shown in Equation 4:

$$SR = 2\pi f A\cos\left(2\pi f t + \theta\right)_{t=0} \xrightarrow[V_{O,Peak} = A/\sqrt{2}]{f = f_{-3dB}} 2\pi f_{-3dB}\frac{A}{\sqrt{2}}$$

$$SR = 2\pi f_{-3dB}\frac{A}{\sqrt{2}} \tag{4}$$

Where:

f_{-3dB} = amplifier –3-dB large-signal bandwidth (BW)
A = peak output before slew limiting

As a first-order approximation, the highest frequency in the desired signal should be five times ***less*** than the large-signal BW of the amplifier if distortion is to be minimized.

Noise/SNR

Signal-to-noise ratio was defined and discussed in an earlier section as the noise-related performance metric for ADCs. However, the noise performance of high-speed amplifiers is usually expressed in the product data sheet in terms of the quantities shown in Figure 10. I_{ni} and I_{nn} represent the equivalent current noise of the inverting input and noninverting input, respectively. An ideal operational amplifier (op amp) has no noise or current flow through the input terminals, so the current noise represents the non-ideality and the uncertainty of the actual op amp inputs. These noise parameters are usually expressed in high-speed op amp data sheets as current spectral densities, with the units typically in $pA/Hz^{1/2}$ for a high-speed op amp with NPN or PNP input transistors, or $fA/Hz^{1/2}$ for FET-input devices. If the high-speed op amp is a voltage-feedback amplifier, then $I_{ni} \approx I_{nn}$, and the device data sheet has a single entry for current noise. If the device is a current-feedback amplifier, then as a rule, $I_{ni} > I_{nn}$ and the device data sheet shows the noise currents with separate entries. The quantity e_n is an input-referred voltage noise spectral density, and its units are usually $nV/Hz^{1/2}$ for a high-speed op amp. Additional information on high-speed, op amp noise performance and modeling may be found in application reports SLVA043 and SBOA066, both available for download from the TI web site.

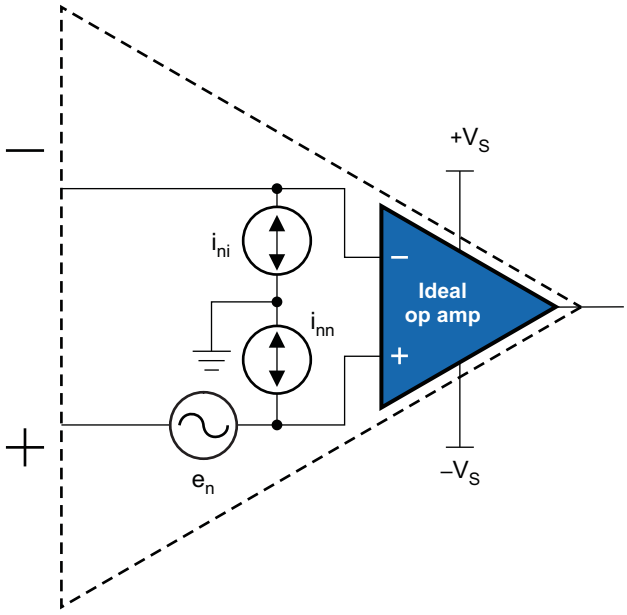

Figure 10. Input-Referred Op Amp Noise Model

Figure 11 shows an example of input-referred noise spectrum plots taken from the OPA2695 data sheet, a dual, broadband, current-feedback operational amplifier. The increase of noise with decreasing frequency is a result of the low-frequency dominance of *flicker noise* or *1/f* noise. As the frequency increases away from 0 Hz, 1/f noise decreases until it disappears below the *flat-band* or *thermal noise* that depends on temperature and is constant across frequency. For high-speed amplifiers, flat-band noise tends to be the dominant noise mechanism above 10 kHz to 100 kHz. See application reports SLVA043 and SBOA066 for additional details.

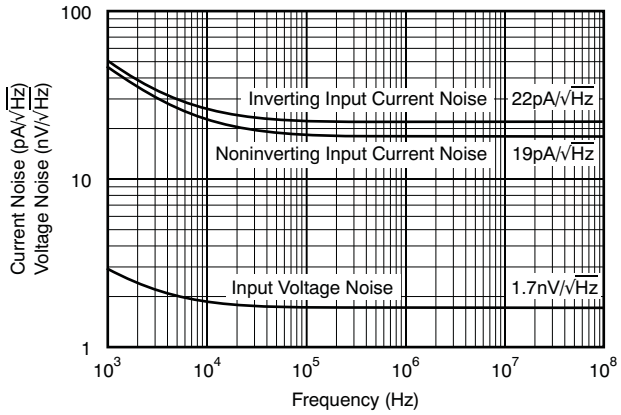

Figure 11. Input-Referred Noise for the OPA2695

Selecting an Amplifier

The amplifier/ADC combination represents a simple two-component system, and the implicit assumption is that the overall system performance requirements are usually centered on the performance of the high-speed ADC. The choice of the driver amplifier often simplifies to a device with convenient operating voltage and/or feature set that is compatible with the application. This selection criteria must be considered on a case-by-case basis. This section focuses on simple calculations to estimate the potential noise and distortion performance of a two-device system, and uses these calculations to estimate the required performance of the amplifier.

Figure 12 illustrates the general model for a band-limited driver circuit for a typical high-speed ADC.

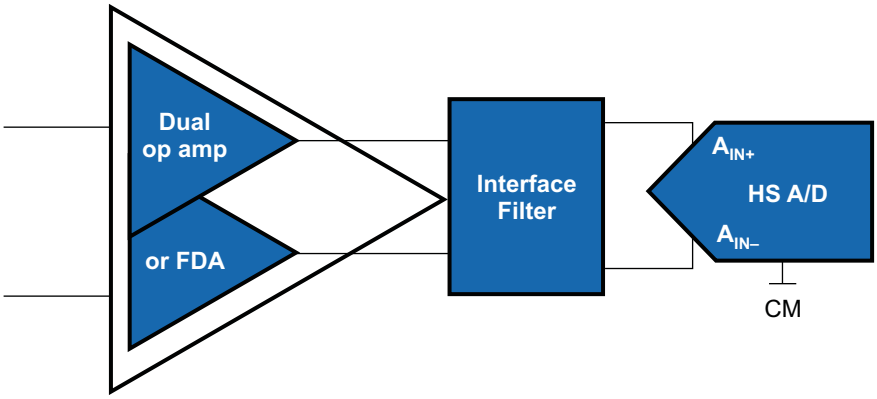

Figure 12. General Model for a Band-Limited Driver Circuit for a High-Speed ADC

For optimal system performance, it is generally best to place antialiasing filters before the driver amplifier. The interface filter is generally a low-pass filter (LF) or bandpass filter (BF) to limit the out-of-band noise. Recall that flat-band noise on the amplifier output has a wide bandwidth, and if the out-of-band noise is not attenuated, it can alias into the passband, thus increasing the noise floor.

Noise

The following discussion gives an example of a noise analysis for a common circuit architecture used as a high-speed ADC driver. Figure 13 shows a differential noninverting amplifier similarly based on the OPA2695, a dual current-feedback device with a symmetrical pinout optimized to serve as an A/D driver. The amplifier/ADC interface filter is formed by the 100-Ω output resistors and the 12-pF capacitor acting as a differential LF with a –3-dB corner frequency of 66 MHz. The function of the LF is to attenuate the high-frequency noise that falls out of the usable band. The equivalent noise bandwidth of a single-pole RC filter is $(\pi/2)f_{-3dB}$. This value can be interpreted as the cutoff frequency of an ideal brick-wall filter. If passband flatness is critical, then the –3-dB corner of a single-pole RC filter must be 6.5 times greater than the highest signal frequency. In this example, the recommended passband is f <10 MHz. For additional information on filter design for ADC driver circuits, see application reports SLWA053 and SBAA108.

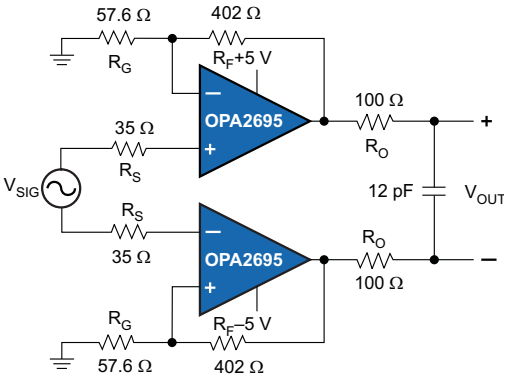

Figure 13. Differential Noninverting Amplifier

For the purposes of noise analysis, the circuit can be split into two single-ended amplifiers, with the SNR performance of either half being representative of the entire circuit (see Figure 14). Figure 14 shows the amplifier input-referred noise sources described earlier (I_{nn}, I_{ni}, and e_n) as well as the equivalent noise sources arising from the external resistors ($e_{n,RG}$, $e_{n,RF}$, $e_{n,Ro}$, and $e_{n,RS}$).

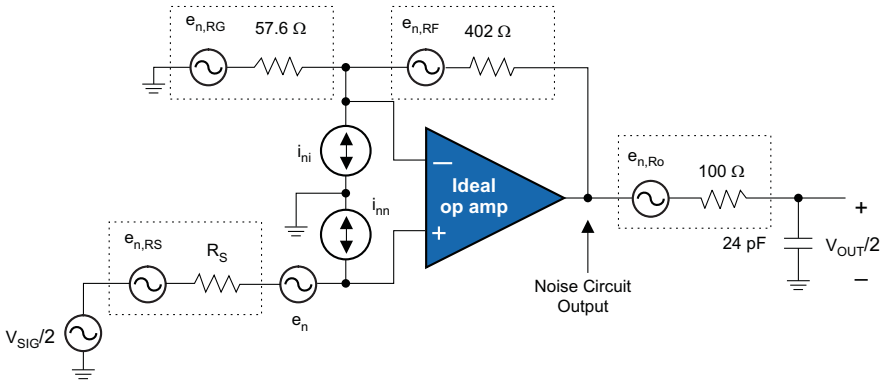

Figure 14. Noise Analysis Circuit

Many high-speed applications require an operating bandwidth that is much greater than the op amp 1/f noise bandwidth. Because of this requirement, low-frequency 1/f noise often has a negligible impact on the overall noise performance of the circuit. For example, Figure 11 shows the OPA2695 noise is dominated by flat-band noise for f > 10 kHz (that is, the device 1/f noise is negligible for f > 10 kHz); so, for operating bandwidths greater than 1 MHz, ignore the effects of 1/f noise, which results in an error of less than 6%. This device is intended to operate at frequencies well above 1 MHz; therefore, this error will be negligible. Table 1 summarizes the op amp flat-band noise sources and their individual contributions to the circuit output noise spectrum.

Table 1. Op Amp Flat-Band Noise Sources and Contributions to Typical Circuit Output Noise Spectrum

Noise Source	Noise Source Value	Noise Source Origin	Output Noise Expression	Output Noise Spectrum, $e_{o,n}$
I_{nn}	19 nV/Hz$^{1/2}$	OPA2695 data sheet	$i_{nn}R_S\left(1+R_F/R_G\right)$	5.3 nV/Hz$^{1/2}$
I_{ni}	22 pA/Hz$^{1/2}$		$i_{ni}R_F$	8.8 nV/Hz$^{1/2}$
e_n	1.7 nV/Hz$^{1/2}$		$e_N\left(1+R_F/R_G\right)$	13.6 nV/Hz$^{1/2}$
$e_{n,RG}$	0.96 nV/Hz$^{1/2}$	$\sqrt{4kTR_G}$	$R_F\sqrt{4kT/R_G}$	6.7 nV/Hz$^{1/2}$
$e_{n,RF}$	2.54 nV/Hz$^{1/2}$	$\sqrt{4kTR_F}$	$\sqrt{4kTR_F}$	2.54 nV/Hz$^{1/2}$
$e_{n,RS}$	0.75 nV/Hz$^{1/2}$	$\sqrt{4kTR_S}$	$\sqrt{4kTR_S}\left(1+R_F/R_G\right)$	6 nV/Hz$^{1/2}$

Where *k* is Boltzmann's constant (1.381×10^{-23} J/K) and T is the temperature in Kelvins (290°K for this analysis). For additional background and details on high-speed operational amplifier noise analysis, see application reports SLVA043 and SBOA066.

Because the individual noise sources are statistically independent from and uncorrelated with one another, the total output spectrum of our noise analysis circuit may be calculated as a sum-of-squares:

$$\begin{aligned} e_{OUT,Amp,(\pm)} &= \sqrt{\sum_n e_{o,n}^2} \\ &= \sqrt{5.3^2 + 8.8^2 + 13.6^2 + 6.7^2 + 2.54^2 + 6^2} \\ &= 19.4 \text{ nV}/\sqrt{\text{Hz}} \end{aligned} \quad (5)$$

Which is the equivalent flat-band output noise spectrum of this single-ended analysis circuit. The noise in this single-ended circuit is equal to and uncorrelated from any noise in the other single-ended circuit that forms the other half of this differential amplifier. So, the total noise of the entire differential circuit is the sum-of-squares of the two individual noise terms:

$$\begin{aligned} e_{OUT,Amp} &= \sqrt{e_{OUT,Amp,(+)}^2 + e_{OUT,Amp,(-)}^2} = \sqrt{2e_{OUT,Amp}^2} \\ &= e_{OUT,Amp}^2\sqrt{2} \\ &= 27.4 \text{ nV}/\sqrt{\text{Hz}} \end{aligned} \quad (6)$$

Following from the earlier assumption of dominant flat-band noise, it can be assumed that the output spectrum is constant over the passband of the op amp, and only the output low-pass filter limits the bandwidth of the amplifier output noise. The 66-MHz, single-pole, low-pass filter has an equivalent noise bandwidth of $(\pi/2) \times f_{-3dB} = 1.57 \times 66$ MHz = 104 MHz (see SLVA043), which allows the calculation of an equivalent filter output noise voltage over the passband.

$$e_{Amp,Filter} = \sqrt{BW_N \times \left(e^2_{OUT,Amp} + e^2_{n,Ro}\right)}$$
$$= \sqrt{104 \times 10^6 \times \left[e^2_{OUT,Amp} + 4kT(100)\right]} = 280\ \mu V_{rms} \quad (7)$$

If the nominal signal out of the low-pass filter is a 2-V_{PP} sinusoid, then the available SNR for the entire differential amplifier/filter circuit is:

$$SNR_{Amp/Filter} = 10\log\left(\frac{V_o^2}{e^2_{OUT,Filter}}\right) = 20\log\left(\frac{2/\left(2\sqrt{2}\right)}{\left(280\ \mu V\right)^2}\right) = 69.5\,dB \quad (8)$$

Note that halving the op amp gain (doubling R_G) increases the output SNR by 3.5 dB, whereas halving the low-pass filter f_{-3dB} corner frequency (to 33 MHz) increases the SNR by 3 dB. The output SNR matches any change in the input level decibel for decibel.

Because the amplifier and ADC noise mechanisms are independent, it is reasonable to assume that the noise terms for the two devices are additive in a sum-of-squares sense; the total noise can then be expressed as:

$$e^2_{Total} = e^2_{Amp/Filter} + e^2_{ADC} \quad (9)$$

Recalling that the major noise-related ADC parameter is SNR referenced to the ADC full-scale input voltage, the total noise can be expressed as:

$$\frac{e^2_{Total}}{V^2_{FS}} = \frac{e^2_{Amp/Filter}}{V^2_{FS}} + \frac{e^2_{ADC}}{V^2_{FS}} \quad (10)$$

Where V_{FS} is the ADC full-scale input voltage. Recalling that $SNR = 10\log\left(V^2/e_n^2\right)$, the maximum total SNR can be expressed as:

$$SNR^{-1}_{System} = SNR^{-1}_{Amp/Filter} + SNR^{-1}_{ADC} \quad (11)$$

In Equation 11, SNR is in linear units, not dB. If the quantities are in dB units, the expression becomes:

$$SNR_{System} = -10\log\left(10^{-SNR_{Amp/Filte}/10} + 10^{-SNR_{ADC}/10}\right) \quad (12)$$

One key result from Equation 12 is that an active ADC driver always contributes noise to the signal path, and the overall system SNR_{System} is always less than SNR_{ADC}.

Many times, the ADC noise performance drives the noise requirements of the rest of the signal chain. With that practice in mind, it can be useful to specify the relative difference between the system and ADC SNRs, so that one can then calculate how much larger the amplifier SNR needs to be than the ADC SNR to support the system noise requirement. In other words, if you can specify $x_{dB} = (SNR_{System})_{dB} - (SNR_{ADC})dB$, then it is possible to calculate Δ dB = $(SNR_{Amp/Filter})_{dB} - (SNR_{ADC})_{dB}$ via the following relationship:

$$\Delta_{dB} = \left(SNR_{Amp/Filter}\right)_{dB} - \left(SNR_{ADC}\right)_{dB} = -10\log_{10}\left(10^{-x_{dB}/10} - 1\right)$$

where:

$$x_{dB} = \left(SNR_{System}\right)_{dB} - \left(SNR_{ADC}\right)_{dB} \leq 0 \text{ dB} \quad (13)$$

Figure 15 provides an easy way to estimate the required amplifier SNR rise above the ADC (Δ_{dB}) to achieve the total system SNR degradation with respect to the ADC (x_{dB}).

The numbered points on the curve represent some specific cases of amplifier and ADC noise.

1. Δ_{dB} = 0 dB: the amplifier/filter and ADC have the same SNR: $SNR_{Amp,Filter} = SNR_{ADC} = SNR$, then the system SNR is 3 dB less than either → $SNR_{System} = SNR_{dB} - 3$ dB.
2. x_{dB} = –1 dB: the system SNR can be 1 dB *less* than SNR_{ADC} → $SNR_{System} = SNR_{ADC} - 1$ dB. → Δ dB = 5.9 dB: The amplifier/filter must have an SNR that is 5.9 dB *greater* than the ADC
3. If SNR_{System} to be 0.1 dB *less* than SNR_{ADC} → $SNR_{System} = SNR_{ADC} - 0.1$ dB, → Δ dB = 16.3 dB: The amplifier/filter must have an SNR that is 16.3 dB *greater* than the ADC.

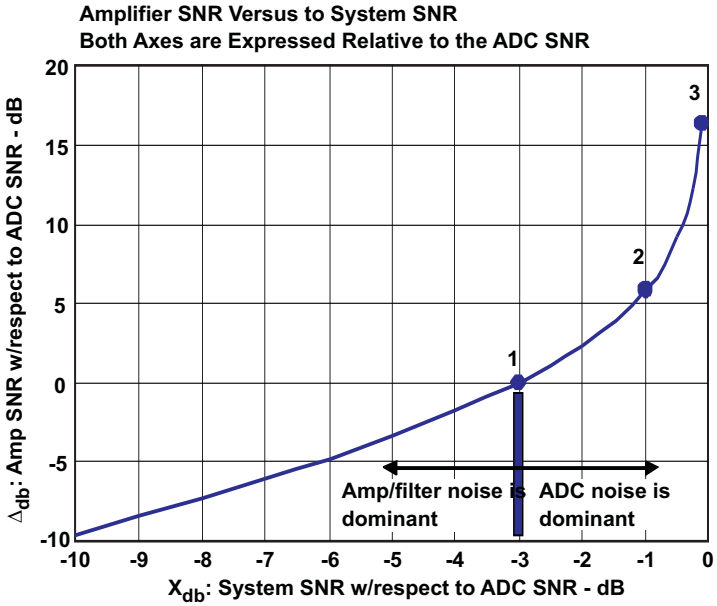

Figure 15. Relative Amplifier SNR vs Relative System SNR, Both with Respect to A/D SNR: ($SNR_{AMP} - SNR_{A/D}$) vs ($SNR_{SYS} - SNR_{A/D}$)

9 Distortion

This section presents a simple set of calculations that can help model the total distortion of this simple amplifier/ADC *system*. A complete and thorough discussion of distortion behavior for amplifiers and for ADCs is available from other sources such as the *Analog Applications Journal* (see article SLYT133, for example). The goal of this section is similar to what was presented in the amplifier/ADC noise calculations section: to focus on a method that allows a designer to pick an op amp based on the overall performance requirements. The analysis of the combined harmonic distortion for the amplifier and ADC is similar to the

SNR analysis previously shown. One important difference is that amplifier distortion products and ADC distortion products are *correlated* with one another, unlike the noise terms in the previous analysis. The result of this condition is that the analysis is restricted to a worst-case assumption that individual amplifier distortion components and individual ADC distortion components sum as *voltages* rather than as *powers* (sum-of-squares done in the previous noise analysis).

Many times, ADC distortion is specified in terms of the spurious-free dynamic range (SFDR), the worst-case spur relative to the full-scale voltage, which may not be harmonically related to the desired signal. Amplifier distortion, on the other hand, is usually specified via HD2, HD3, and/or IMD2/3, which are all harmonically related to the desired signal.

The output of the amplifier/filter contains a desired signal component, as well as HD2 and HD3 components. When the desired signal is applied to the ADC input, it generates its own harmonic distortion that sums constructively or destructively with the HD2 and HD3 from the amplifier/filter. As previously discussed, the worst-case scenario occurs when each of the amplifier and the ADC distortion components sum constructively as voltages:

$$v_{HD,Total} = v_{HD,Amp/Filter} + v_{HD,ADC} \tag{14}$$

If the voltages are referenced to the ADC full-scale voltage and the signal is a simple sinusoid (carrier), the expression becomes:

$$\frac{v_{HD,Total}}{V_{FS}} = \frac{v_{HD,Amp/Filter}}{V_{FS}} + \frac{v_{HD,ADC}}{V_{FS}} \Rightarrow \frac{1}{HD_{Total}} = \frac{1}{HD_{Amp/Filter}} + \frac{1}{HD_{ADC}} \tag{15}$$

Where no distinction has yet been made between HD2 or HD3, and the quantities in the second row of the equation are linear and have no units. Note that HD in this case refers to a single harmonic spur—such as HD2 or HD3—and not the composite total harmonic distortion (THD).

$$HD_{System} = 20\log\left(10^{HD_{Amp/Filte}/20} + 10^{HD_{ADC}/20}\right) \tag{16}$$

In a manner similar to the previous noise analysis, an expression can be developed which gives the amplifier HD performance (relative to the ADC) that results from a required, overall system HD (also relative to the ADC):

$$\Delta_{HD,dB} = \left(HD_{Amp/Filter}\right)_{dB} - \left(HD_{ADC}\right)_{dB} = 20\log_{10}\left(10^{y_{dB}/20} - 1\right)$$

where:

$$y_{dB} = \left(HD_{System}\right)_{dB} - \left(HD_{ADC}\right)_{dB} \geq 0 \text{ dB} \tag{17}$$

Figure 16 provides an easy way to estimate the required amplifier HD rise above the ADC ($\Delta_{HD,dB}$) to achieve the total system HD degradation with respect to the ADC (y_{dB}).

The numbered points on the curve represent some specific cases of amplifier and ADC noise.

1. $\Delta_{HD,dB}$ = 0 dB: the amplifier/filter and ADC have the same HD and $HD_{Amp,Filter} = HD_{ADC} = HD$, and the system HD is 6 dB greater than either → $HD_{System} = HD_{dB} + 6$ dB.
2. x_{dB} = 3 dB: the system HD can be 3 dB *worse* than HD_{ADC} so $HD_{System} = HD_{ADC} + 3$ dB and ΔHD_{dB} = –7.7 dB. The conclusion: the amplifier/filter must have an HD that is 7.7 dB *better* than the ADC.
3. If HD_{System} to be 1 dB *worse* than HD_{ADC} → $HD_{System} = HD_{ADC} + 1$ dB,
   → $\Delta_{HD,dB}$ = –18.3 dB: The amplifier/filter must have an HD that is 18.3 dB *better* than the ADC.

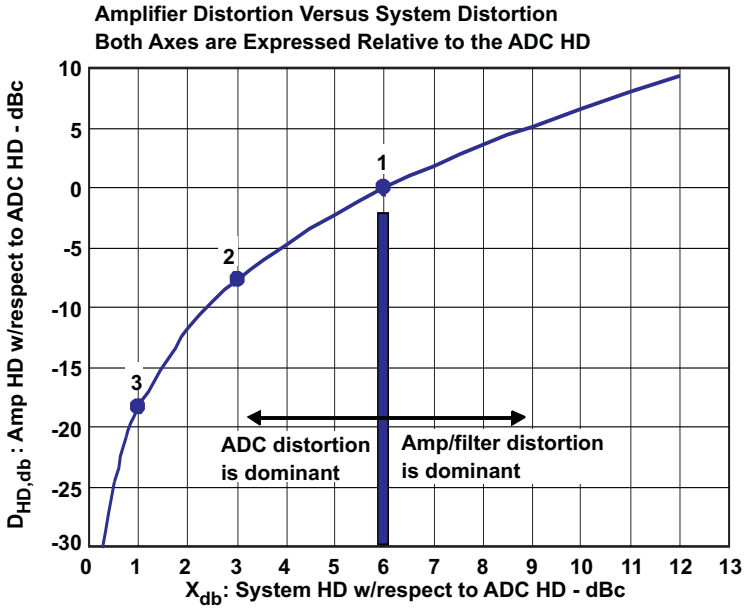

Figure 16. Amplifier Distortion vs System Distortion, Both with Respect to A/D Distortion: ($HD_{AMP} - HD_{A/D}$) vs. ($HD_{SYS} - HD_{A/D}$)

Note that many board-related factors can specifically affect HD2 and have little impact on HD3. These factors include power supply bypassing as well as mechanical and electrical symmetry of the layout. If a differential signal path is unsymmetrical in terms of component values and/or signal path routing, then its ability of the differential signal path to provide the natural attenuation of HD2 can be compromised. For additional information on best practices for high-speed PC board layouts, see application report SBAA113.

10 High-Speed Amplifier Circuit Architectures

This section provides application examples based on two ADCs, the ADS5493 and the ADS6444. The ADS5493 is a 130-MSPS, fully-differential ADC that has low-noise performance and outstanding SFDR over a wide frequency range. The ADS5493 is naturally coupled with the THS770006, a fixed-gain (+6 dB), 14-/16-bit, fully-differential, wideband op amp to provide a complete signal conditioning and data acquisition solution for high-speed applications. Interfacing the two devices with an application-specific filter allows the designer to maintain the high-performance, low-distortion characteristics desired in signal conversion.

The ADS6444 is a quad, 125-MHz, CMOS ADC that can be driven by a variety of op amp drivers depending on application and performance needs. The specific examples discussed here are taken from a prototype evaluation board that contains three active driver circuits and a single transformer-coupled passive signal path. The evaluation board features the ADS6444. The three active drivers were chosen for this EVM to provide an array of driver solutions that can operate effectively over the first three Nyquist zones of the ADC. The circuits are based on the following devices and functionality with the ADS6444:

1. OPA2695: Dual current-feedback op amp that can be easily configured as a high-gain, fast instrumentation amplifier. It can provide 14-bit noise and distortion performance through the first Nyquist zone.
2. THS4509: Fast fully-differential amplifier (FDA) that can provide excellent dynamic range for a broadband signal through the first Nyquist zone of the ADS6444, and in the second Nyquist zone with appropriate band-pass filtering.
3. THS9001: IF/RF amplifier which can serve as an effective ADC driver for high-IF narrowband signals such as those generally found in digital radio signal chains.

11 THS770006 Driving ADS5493: Single-Ended Input

Figure 17 shows a configuration that uses a transformer to convert from a single-ended input to fully-differential signaling, as is the default configuration on the ADS5493EVM. The ADS5493EVM has an onboard analog signal path with room for the THS770006 as well as a generic filter network layout that enables rapid prototyping for target frequency ranges. To ensure there are no offsets in the amplifier output, both amplifier inputs should be impedance- and bias-matched. In this example, the two 50-Ω resistors in front of the THS770006 provide termination-matching for the input transmission line before the transformer, assuming a turns ratio of 1:1.

Note: This document refers to the ADS5493EVM prototype; changes may be made in the released version of the EVM.

The gain of the THS770006 is set at +6 dB by the internal feedback resistor network, R_F and R_S. The output stage of the amplifier drives a filter, tuned for a specific response characteristic that reduces unwanted distortion, and limits the noise bandwidth. In this case, the two 200-Ω resistors and the 5-pF capacitor create a low-pass filter network, with a –3-dB frequency of approximately 80 MHz. This configuration is useful for first Nyquist zone sampling. For higher Nyquist zone sampling, a bandpass filter is required for best performance. The two 0.1-µF capacitors before the input of the ADS5493 provide dc blocking, and internal circuitry in the ADS5493 supplies the required common mode voltage (CM) for the ADC.

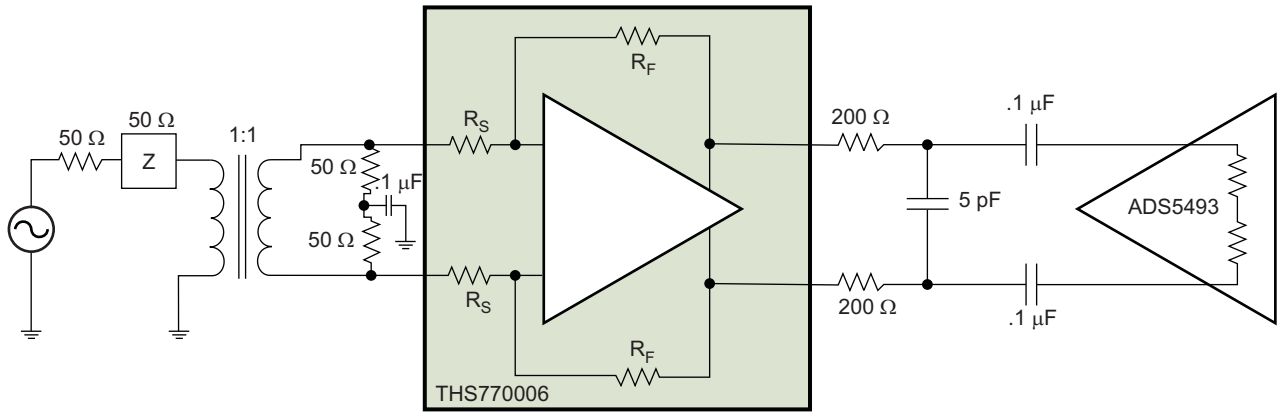

Figure 17. High-Speed ADC Driver Amplifier with Single-Ended to Differential Input Conversion

12 Dual Op Amp Active Driver Considerations

The circuit illustrated in Figure 18 uses two devices configured as noninverting gain stages. The circuit diagram is taken from the evaluation board and is used to illustrate a dc-coupled, noninverting buffer configuration. The OPA2695 is a dual, current-feedback op amp and the ADS6444 is a 125-MHz, 14-bit CMOS ADC with unbuffered inputs.

The amplifier is a source of broadband noise with a spectral bandwidth that can be higher than the analog bandwidth of the ADC. The RC network between the amplifiers and the ADC serves as a noise-limiting, low-pass filter that attenuates the out-of-band noise from the amplifier. For the values shown (100 Ω and 12 pF), the filter –3-dB bandwidth is approximately 66 MHz, and covers the first Nyquist zone of the converter. If a signal occupies the first Nyquist zone, it is often called a *broadband* signal. As mentioned in the previous section, the equivalent noise bandwidth of the single-pole LF is $(\pi/2) \times f_{-3dB} = 1.57 \times 66$ MHz = 104 MHz, so that some aliasing of the amplifier output noise occurs. The OPA2695 is an excellent low-power solution for high-gain baseband applications with bandwidths to 40 MHz, as well as for narrowband IF applications to 70 MHz.

One of the general requirements for effective amplifier performance down to dc is that the signal source has a dc common-mode voltage equal to the reference common-mode voltage provided by the ADC. Thus, the bias points at the transformer center-tap and the gain-setting resistors; therefore, one consideration is that the selected device and its power-supply voltages must support an amplifier input common-mode range (CMIR) that includes the CM voltage.

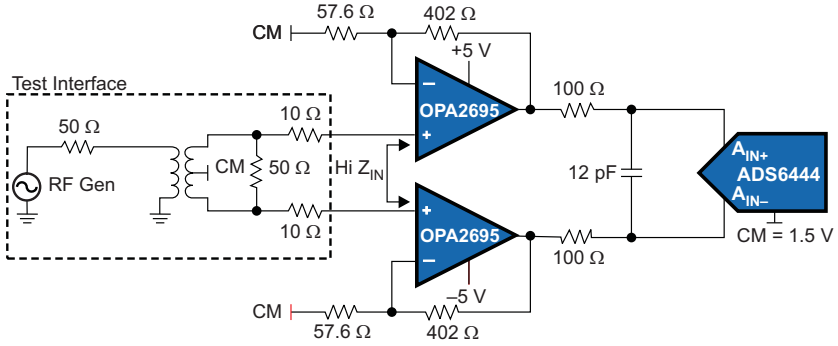

Figure 18. High-Speed, ADC Driver Amplifier with High-Impedance Inputs (Based on the OPA2695)

One feature of this circuit topology is that it can offer very high input impedances because the input nodes (the noninverting pins of the op amp) are themselves high-impedance nodes. For the OPA2695, the equivalent input impedance of the circuit is in excess of 500 kΩ. If FET-input op amps are used, such as the OPA653/659, the input resistance can be as high as 10^{12} Ω, but at the expense of increased noise that may reduce the system dynamic range to between 10 to 12 bits. Well-matched, dual op amps can offer an efficient high-speed solution.

The 100-Ω resistors and the 12-pF capacitor on the op amp outputs are a noise-limiting, low-pass filter (LF). The LF—especially the resistors—also provides some isolation of the amplifier output from A/D *kick-back* that comes in the form of common-mode transients resulting from the clock-driven S/H circuit (see application report SBAA108 for more information). Note that the driver circuit provides the bias to the ADC input via the CM reference voltage output on the ADC.

Fully-Differential Amplifier

A fully-differential amplifier (FDA) combines differential inputs and outputs in a single device that can serve as an efficient ADC driver. Figure 19 shows a THS4509 that converts a single-ended input signal into a differential output signal that in turn drives the ADS6444. The output resistors and 6.8-pF capacitor serve as a noise-limiting LF and to provide some isolation between the amplifier output and the A/D common-mode kick-back. The 69.8-Ω resistors act as matching terminations for the 50-Ω signal source as well as pull-up resistors to help center the input common mode. The 50-Ω/0.1-µF combination is intended to mirror the AC-coupled test signal source which is assumed to be an RF generator with a minimum nonzero frequency. For additional information on design and performance of FDAs, see related documents SLOA054, SLYT310, and SLYT223, all available for download from the TI web site.

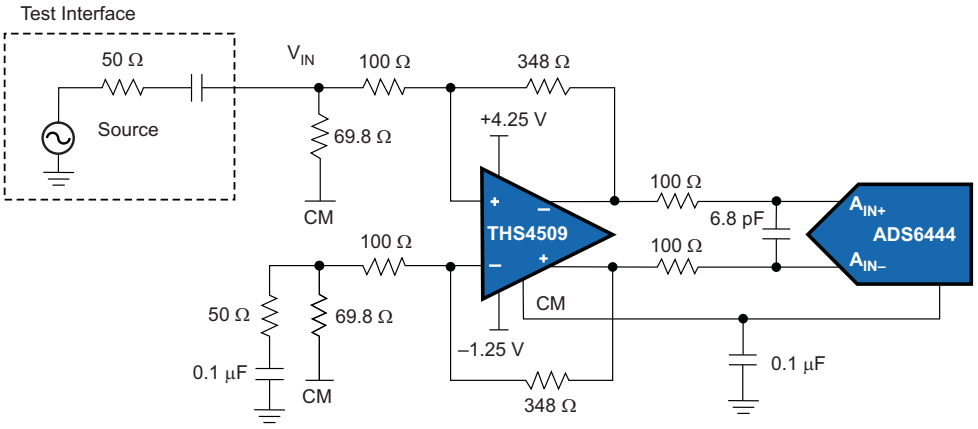

Figure 19. High-Speed ADC Driver Amplifier (Based on the THS4509)

13 IF Amplifier

If the signal is a narrowband signal, then driver-based RF/IF amplifiers might provide a cost-efficient solution. The THS9001 devices shown in Figure 20 are RF/IF amplifiers with a gain of 16 dB, and are configured as a dual differential driver. The common-mode rejection of the output transformer tends to attenuate HD2 spurs and balance small gain differences between the two amplifiers.

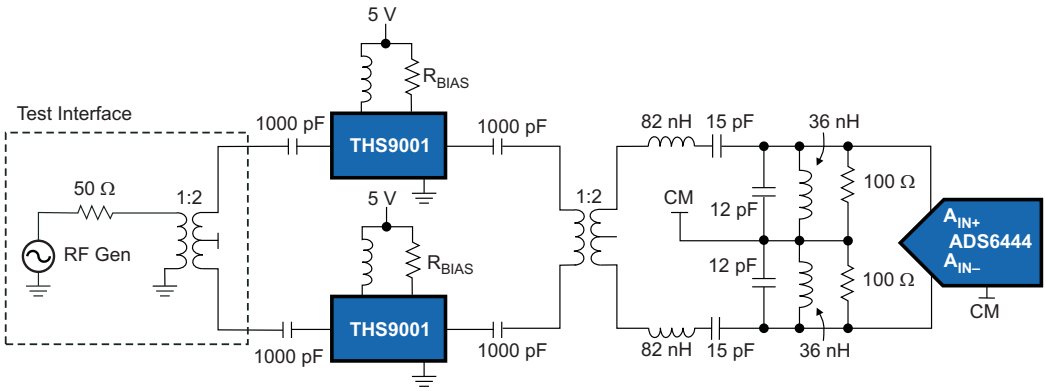

Figure 20. High-Speed A/D Driver Amplifier (Based on the THS9001)

14 References

1. *Noise Analysis in Operational Amplifier Circuits* application report (SLVA043)
2. *Fully Differential Amplifiers* application report (SLOA054)
3. *Design of Differential Filters for High Speed Signal Chains* application report (SLWA053)
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6. *Using a Decompensated Op Amp for Improved Performance*, Texas Instruments Analog Applications Journal, May 2000 (SLYT015)
7. *RLC Filter Design for ADC Interface Applications* application report (SBAA108)
8. *ADS5500, OPA695: PCB Layout for Low Distortion High Speed ADC Drivers* application report (SBAA113)
9. *Noise Analysis for High Speed Op Amps* application report (SBOA066)
10. *Low-Power, High-Intercept Interface for ADS5424 14-bit, 105-MSPS Converter for Undersampling Applications* application report (SLYT223)
11. *Voltage Feedback Vs Current Feedback Op Amps* application report (SLVA051)

Revision History

Changes from Original (November, 2009) to A Revision **Page**

- Updated graphic format for multiple figures for consistency 1
- Revised Section 10 18
- Added Section 11 and Figure 17 19

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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