

Cascading Precision Op Amp Stages for Optimal AC and DC Performance



Zach Olson

ABSTRACT

This applications note examines cascading precision op amps to optimize bandwidth, offset, and noise for high-gain applications. This document covers the benefits and disadvantages of various gain staging techniques and includes Monte Carlo analysis to consider variance in offset voltage across a large batch of amplifiers.

Table of Contents

1 Introduction.....	2
2 Voltage Offset.....	2
3 Bandwidth.....	3
4 Cascaded Amplifier Bandwidth.....	3
5 Cascaded Amplifier Offset.....	4
6 Multi-Stage Amplifiers.....	5
7 Normal Distributions in Offset Voltage.....	5
8 Noise Considerations.....	6
9 Summary.....	7
10 Resources.....	8
10.1 TI Recommended Parts.....	8
10.2 TI Precision Labs Training Videos.....	8
10.3 TI Recommended Resources.....	8

Trademarks

All other trademarks are the property of their respective owners.

1 Introduction

Operational amplifiers (op amps) employed in various applications may be called upon to amplify very small signals, requiring them to operate with high closed-loop gains in the hundreds, or thousands of volts per volt (V/V). If the required gain is in the range of tens to a few hundred V/V, a single precision op amp can provide the desired electrical performance. However, once the gain requirements become significantly higher, a single-stage approach might not provide adequate levels of performance.

2 Voltage Offset

Voltage offset occurs due to slight mismatches between transistors that make up the differential input pair of an op amp. On some products, TI employs unit-level [eTrim](#) or [laser trimming](#) during production test to reduce this offset as much as possible. However, it is not practical to remove the voltage offset entirely, so the engineer must account for it in the design process.

[Figure 2-1](#) shows how the offset voltage can be modeled as a DC voltage generator V_{osi} , in series with the non-inverting input of an op amp. The exact value of V_{osi} will vary between components and can have either positive or negative polarity. Typical and maximum V_{osi} values are specified in the op amp's datasheet Electrical Characteristics table.

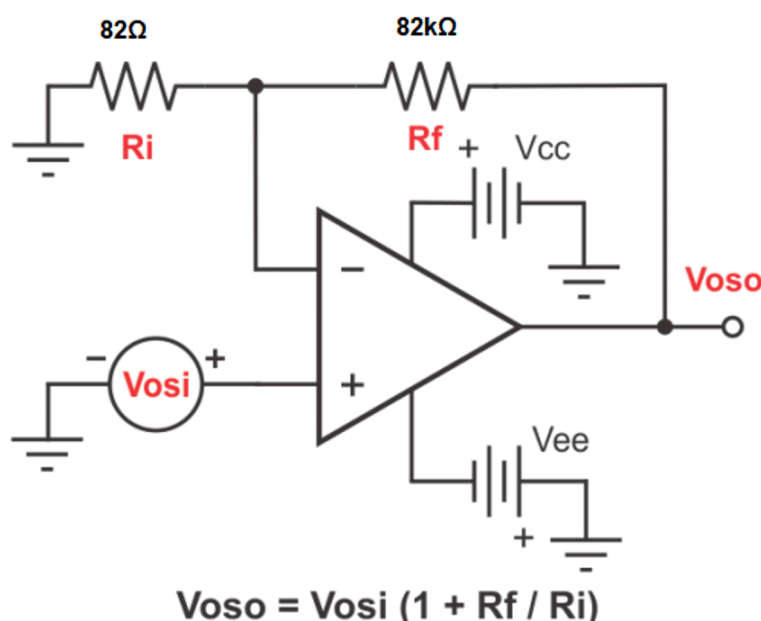


Figure 2-1. Amplifier stage with voltage offset model

There is always a DC error voltage at the output of an amplifier circuit. This output error is mainly caused by the V_{osi} multiplied by the non-inverting gain of the amplifier circuit, which appears on the output as V_{oso} . A higher gain circuit will produce a greater V_{oso} at the output.

There are additional factors that add to the total DC output error; finite common-mode rejection (CMRR), power supply rejection (PSRR), open-loop gain (A_{ol}), and input bias currents (I_b) flowing through the source resistances. Although they must be considered in every design, in the interest of brevity, these errors will not be included in this discussion.

3 Bandwidth

Typical voltage feedback op amps have a low frequency pole present in their AC response, limiting the bandwidth of the device. The frequency response is similar to that of a low pass filter, with reduced gain at higher and higher frequencies. The bandwidth of the amplifier circuit is determined by dividing the gain bandwidth product (GBW) of the op amp by the closed-loop gain of the amplifier circuit. The GBW is specified in the op amp's datasheet Electrical Characteristics table.

$$\text{Bandwidth} = \frac{\text{GBW}}{\text{Gain}} \quad (1)$$

For example, the GBW of the OPA2210, a precision op amp, is 18MHz. For an application requiring a high gain of 1000 V/V (60dB), the effective bandwidth of a single-stage amplifier is a mere 18kHz (AC response of this circuit is shown in [Figure 4-2](#)). While this may be plenty for a near-DC application, there are many applications that demand both high gain and high bandwidth. A high speed op amp with a higher GBW product can be used to extend the bandwidth of the system at high gains, but typically it will come at the expense of DC precision.

Few devices in the marketplace can satisfy the needs of high DC precision, gain and bandwidth in a single amplifier stage. Instead, multiple precision op amps can be cascaded to preserve bandwidth while maintaining low offset and low noise for high gain applications.

4 Cascaded Amplifier Bandwidth

The most common definition for effective bandwidth of a low pass filter (or amplifier in this case) is the frequency where the output voltage drops by 3dB relative to the passband. For a single stage, the cutoff frequency (or pole frequency) can be calculated using equation 1 above. For multiple stages, there are multiple poles to consider.

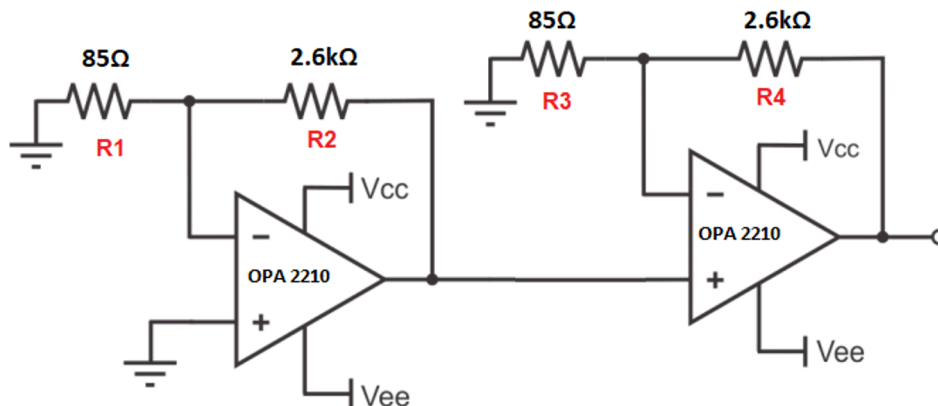


Figure 4-1. Two-stage cascade amplifier

To illustrate this, [Figure 4-1](#) shows a two-stage amplifier circuit with a non-inverting gain of 1000 V/V. The gain per stage is 31.6 V/V which corresponds to a bandwidth of about 570kHz for each stage. However, the AC transfer curve in [Figure 4-2](#) shows a drop of 6dB at 570kHz because there are two poles at this frequency, each contributing -3dB to the curve. Each pole also contributes -20dB per decade of roll-off, so the more stages in an amplifier circuit, the steeper the roll-off will be. This can be an advantage if a “brick wall” response is desired.

The effective bandwidth of the entire system is slightly less than that of each stage, at 364kHz, but much greater than the bandwidth of the single-stage amplifier.

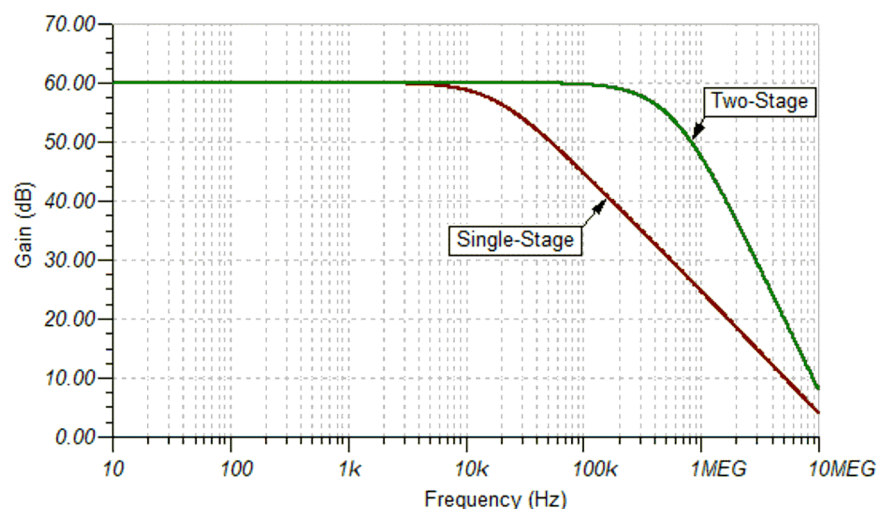


Figure 4-2. Frequency response of two-stage vs one-stage amplifier

An approximation of the total bandwidth of cascaded amplifier stages can be calculated for n stages by:

$$\left(\frac{1}{f_{c1}^2} + \frac{1}{f_{c2}^2} + \dots + \frac{1}{f_{cn}^2} \right)^{-\frac{1}{2}} \quad (2)$$

Where f_c is the cutoff frequency for each stage, as calculated by the GBW.

Note that if one stage's f_c is much lower than the other stages, the low f_c will dominate the bandwidth of the system.

5 Cascaded Amplifier Offset

Cascading gain stages is effective to increase the gain and bandwidth of the system, but at the cost of more noise and offset voltage at the output.

To mitigate this, a good rule of thumb is to design for most of the gain to be applied in the first stage of the amplifier circuit. This technique ensures that most of the output noise and V_{osi} is due to the first op amp stage, with minimal contributions from later stages. In this case, a precision op amp with low V_{osi} and low noise in the first stage will produce the best results.

The V_{osi} of the two-stage amplifier circuit in Figure 4-1 can be described by the following formula:

$$V_{oso} = V_{osi1} \times (G_{A1} \times G_{A2}) + V_{osi2} \times (G_{A2}) \quad (3)$$

Where:

$$G_{A1} = 1 + \frac{R_2}{R_1} \quad (4)$$

$$G_{A2} = 1 + \frac{R_4}{R_3} \quad (5)$$

It is apparent from equation 3 that the V_{osi} of the first op amp is amplified by the gain of the entire system. The V_{osi} of the second op amp is amplified only by the gain of the second stage, lessening its impact on V_{oso} .

6 Multi-Stage Amplifiers

[Equation 3](#) can be expanded for any number of gain stages, i.e. the sum of the offsets of each stage multiplied by the gain of every stage succeeding them.

When comparing between different op amps or circuit layouts, it is often helpful to divide V_{osi} by the total gain of the system to obtain the *input-referred offset*. [Table 6-1](#) shows simulation results for a 1000 V/V amplifier circuit from one to four gain stages. Each stage employs the OPA2210 dual channel, low-noise, low-offset, rail-to-rail output, precision amplifier.

Table 6-1. Bandwidth and offset for multi-stage amplifiers

	1 Stage	2 Stage	3 Stage	4 Stage
Gain/Stage (V/V)	1000	31.6	10	5.62
Input-Referred Offset (μV) (1)	5.02	5.17	5.59	6.17
F_c (2) (Hz)	18k	364k	957k	1530k

- (1) The typical value for V_{osi} (+5 μV) was used for each stage. This is common for spice simulations, but as it turns out the polarity of each stage's offset can be an important factor.
- (2) The typical value for gain bandwidth (18MHz) was used for simulation. In practice the bandwidth of an amplifier can vary from the typical value.

We can see that there is an inherent tradeoff between bandwidth, offset voltage, and the number of gain stages. For a low-offset precision op amp such as the OPA2210, the increase in offset voltage is minimal compared to the increase in bandwidth. This highlights the importance of using precision op amps, especially in the early stages of an amplifier circuit.

7 Normal Distributions in Offset Voltage

In reality, an op amp's V_{osi} will not always be the typical value given in the data sheet. The actual values are part of a Gaussian distribution that is limited between the min/max of the device specifications. [Figure 7-1](#) shows a Gaussian distribution of offset voltages sampled from a large batch of OPA2210 units.

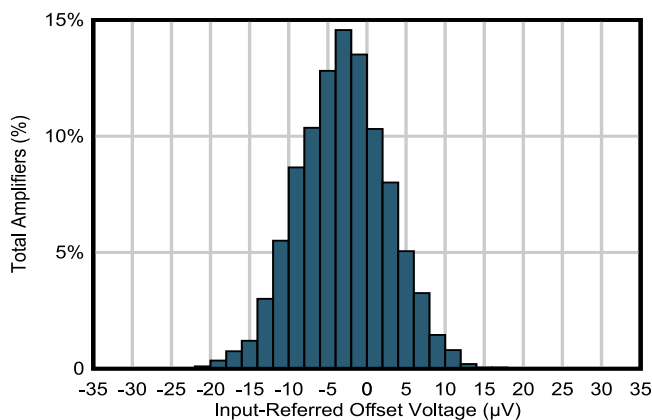


Figure 7-1. Offset voltage production distribution: OPA2210

As shown in [Table 7-1](#), it is possible for an op amp's V_{osi} to have a positive or negative polarity. This means it's possible for the offsets of various stages to either combine (same polarity) or cancel (opposite polarities).

To understand the effects of these distributions, a Monte Carlo analysis was performed on four different gain implementations of two-stage amplifier circuit, using the OPA2210 for the first stage and the OPA1656 for the second stage. The OPA1656 is a low-noise, low-distortion, precision amplifier optimized for high-performance audio applications where DC precision is not typically required. The typical V_{osi} of the OPA1656 is still very good at 500 μV , but significantly higher than the exceptional 5 μV of the OPA2210.

Ten-thousand iterations of the Monte Carlo simulation were performed for each of the four gain implementations. The four designs highlight the differences in offset and bandwidth when different amounts of gain are applied across the stages. Each design has a total gain of 1000 V/V. Results of the Monte Carlo simulation are shown in [Table 7-1](#).

Table 7-1. Monte Carlo analysis of 10,000 two-stage amplifiers in four different gain implementations

	Design 1	Design 2	Design 3	Design 4
G_{A1} (V/V) OPA2210	200	50	31.6	10
G_{A2} (V/V) OPA1656	5	20	31.6	100
Average Offset (μ V)	-0.08	-0.11	-0.12	-0.23
Standard Dev. (μ V)	5.15	7.01	9.23	25.06
Minimum Offset (μ V)	-19.03	-25.44	-32.68	-90.06
Maximum Offset (μ V)	21.53	27.05	31.96	91.54
Bandwidth (Hz)	91k	374k	580k	530k

The standard deviation of the analysis is comparable to the results of a DC simulation using the typical offset value. However, it is always necessary to consider the max/min offsets that are likely to occur in large-scale production of multi-stage amplifiers due to probability distributions.

8 Noise Considerations

Precision amplifiers not only provide low offset, but also very low noise. There are three dominant noise sources to consider in amplifier design. These are voltage noise density, current noise density, and the thermal noise of the resistors in the circuit. The voltage and current noise densities are intrinsic to the op amp and the values can be found in the Electrical Characteristics section of the datasheet.

It is important that the thermal noise of the resistors do not exceed the intrinsic noise of the op amp. It would be a shame to pay extra for a low noise precision amplifier, just to allow resistor noise to dominate the system. Using smaller resistor values will prevent this from occurring. Lower value resistors will also limit the contribution of the current noise density. Specifically, source resistance at the non-inverting input and the equivalent resistance of the feedback network $R_f \parallel R_i$ (R_{eq}) must be limited. For reference, R_{eq} for all the circuits in this document is $\sim 82\Omega$.

It is worth noting that large resistor values can also interact with parasitic capacitance in the circuit to produce unwanted poles in the frequency response. These unintentional poles can lead to stability issues and should be avoided.

Similar to offset voltage, voltage noise can be modeled as a voltage source in series with the non-inverting input of the amplifier. This noise will be amplified by the non-inverting gain of the amplifier. The same methods used to limit V_{os0} can be used to limit the output voltage noise of the amplifier.

Table 8-1 shows the input-referred noise of the various two-stage circuit designs considered in the Monte Carlo analysis. OPA2210 and OPA1656 have a broadband voltage noise density of $2.2\text{nV}/\sqrt{\text{Hz}}$ and $2.9\text{nV}/\sqrt{\text{Hz}}$ respectively.

Table 8-1. Output noise of a two-stage amplifier in four different gain implementations

	Design 1	Design 2	Design 3	Design 4
G_{A1} (V/V) OPA2210	200	50	31.6	10
G_{A2} (V/V) OPA1656	5	20	31.6	100
1/f (0.1Hz to 10Hz) (nV_{pp})	78.1	91.7	108.6	261.4
Broadband (1kHz) ($\text{nV}/\sqrt{\text{Hz}}$)	2.4	2.4	2.4	2.5
Integrated (0.1Hz to 91kHz) (μV_{pp})	3.9	4.3	4.3	4.4
Total Integrated (μV_{pp})	5.4	10.4	12	11.5

The broadband noise (noise above 1kHz) is very consistent for each design. This is because the low-noise OPA2210 was used as the first stage in all four circuits, and the contributions from thermal and current noise were greatly limited. Note that the super beta bipolar input transistors of the OPA2210 provide much lower 1/f noise compared to the FET input transistors of the OPA1656. Super beta transistors not only have lower 1/f noise, but lower bias current and bias current noise than traditional bipolar transistors.

Total noise is the integrated noise across the bandwidth of each amplifier. In this case, the broadband noise values are nearly identical, so the total noise becomes a function of bandwidth. That is, the higher the bandwidth of the circuit, the more noise is integrated as frequency increases.

9 Summary

When balancing bandwidth, offset, and noise in a high-gain, multi-stage amplifier:

- Use the lowest input offset op amps that are practical and cost permits.
- If different op amps are used in a cascade, use the lowest offset/noise op amp in the first stage.
- If low offset/noise is the highest priority, apply the highest closed-loop gain in the first stage.
- If bandwidth is the highest priority, a more even distribution of gain across stages is appropriate.
- Expect a greater variance in V_{os} across multiple boards due to Gaussian distributions of V_{osi} for each stage. Higher closed-loop gain in the first stage will result in less variance.
- Use small resistor values to keep the thermal noise well below the intrinsic noise of the op amp
- A low source impedance and a low parallel combination of the feedback resistor network (R_{eq}) will reduce the effects of current noise.

As discussed, high-gain applications typically require multiple stages to provide the desired bandwidth and performance. Precision op amps, especially in the early stages of a cascaded amplifier will provide the best performance. The dual-channel op amps recommended below can simplify layout and save board space when multiple stages are necessary.

10 Resources

10.1 TI Recommended Parts

Part Number	Description
OPA2210	Super beta bipolar input transistors, low-offset, low-noise, wide bandwidth, Rail-to-Rail output
OPA1656	FET, low-distortion, low-noise, wide bandwidth, high SNR, Rail-to-Rail output
OPA2320	CMOS, low-voltage, low-noise, wide bandwidth, Rail-to-Rail I/O

10.2 TI Precision Labs Training Videos

- [Offset Voltage](#)
- [Bandwidth](#)
- [Noise](#)

10.3 TI Recommended Resources

- [Offset Correction](#)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated