User's Guide

Interfacing AFE7769DEVM With the Hitek Agilex eSOM7 FPGA

ABSTRACT

This user's guide provides a walkthrough of hardware and software setup with supplemental images as a visual representation, followed by bringup steps, a loop-back example and a loop-back test using an LTE signal.

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1 Introduction

This user's guide introduces a wireless development platform using Texas Instruments' AFE7769D evaluation module (EVM) in collaboration with Hitek Systems, a hardware company and partner of Intel that provides field programmable gated array (FPGA)-based evaluation modules to companies within the communications industry. This reference solution serves to help customers ramp up system integration of the analog front-end (AFE), and provides a "quick evaluation and prototyping platform for 5G ORAN and wireless solutions", per Hitek Systems.

The AFE7769D is a 4T4R2F RF-sampling transceiver with integrated digital pre-distortion (DPD) that serves to linearize power amplifiers (PA's) for improved wireless coverage to the end customer. The wireless development platform utilizes the EVM version of the device, which interfaces with Hitek's component of the solution via an FPGA mezzanine card (FMC+) connector. The Agilex embedded System On Module (eSOM7) is an FPGA module that interacts with the AFE7769DEVM through the FMC+ connector. This hardware is based on Intel Agilex® 7 SoC FPGA built using intel 10 nm SuperFin process technology.

For the following sections of the document, commands are **bolded**, file paths, folders, and names are *italicized*, and titles in user interfaces are in "quotes".

2 Hardware Setup

The following section provides a step-by-step walkthrough of the reference design setup from a hardware (HW) perspective, along with a visual representation of the setup at the end.

Steps:

1. Mount the Agilex Embedded SOM7 (eSOM7) on the TI carrier board.
2. Mount the AFE7769DEVM on the FMC+ slot of the TI carrier board.
3. Plug the +12V 6-pin ATX PCIe power connector into the TI carrier.
4. Connect a micro USB from the host PC to the USB connector J23 of the TI carrier for UART access to HPS (Arm® node).
5. Connect a micro USB from the host PC to the USB connector J24 of the TI carrier for programming the Agilex FPGA image containing RF Interface framework over JTAG.
6. Connect an Ethernet cable to the RJ45 port (J21) of the TI carrier for transferring files across the network.
7. Connect a 5.5V, 5A power supply to the TI AFE7769DEVM.
8. Connect a mini-USB cable between host PC (Windows) and mini-USB port on TI AFE7769D evaluation card for configuring the chips on the evaluation card using customized TI AFE77xxD Latte software (version 0.4.0) with the provided configuration file.
9. SMA cables connected from TX RF ports to RX/FB RF ports.
    a. Connections should be as follows for TX to RX RF ports:
        i. TX1 (J7) to RX1 (J1)
        ii. TX2 (J8) to RX2 (J2)
        iii. TX3 (J9) to RX3 (J3)
        iv. TX4 (J10) to RX4 (J4)
    b. Connections should be as follows for TX to FB RF ports:
        i. TX1 (J7) to FB1 (J5)
        ii. TX2 (J8) to FB2 (J6)

When powering on the HW setup, power on the Agilex eSOM7 TI Carrier before powering on the TI AFE7769DEVM. When powering off the HW setup, power off the TI AFE7769DEVM before powering off the Agilex eSOM7 TI Carrier. For the end result of the HW setup, see Figure 2-1.

Note

The Agilex eSOM7 can come with a Skyworks Si5518 timing module (ASY-00-00048 Rev 2). This is not required for the purposes of this guide.

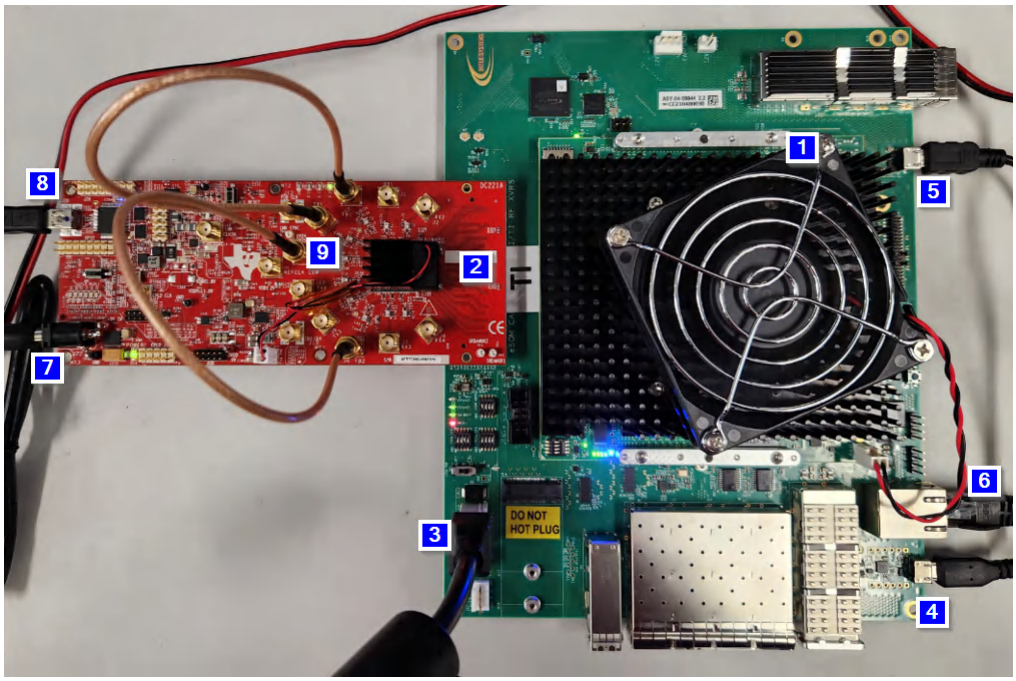

Figure 2-1. Hardware Setup, AFE7769DEVM and Agilex eSOM7

3 Software Setup

The following section provides a step-by-step walkthrough of the reference design setup from a software (SW) perspective, along with screenshots of the process throughout. A folder with the required files can be found in the following link <>. Installers for Quartus Programmer, Teraterm, and Powershell are available online.

Steps:

Install the following elements of software:

1. AFE77xxD Graphical User Interface (GUI) version 0.4.0
   a. Make the following changes to the files in the *Documents\Texas Instruments\AFE77xxDLatte* folder:
      i. Figure 3-1 (*lib\Afe77xxDLibraries\AFE77xxDLibraryPG1p0\resourceFiles\mLmk.py*) and Figure 3-2 (*lib\Afe77xxDLibraries\AFE77xxDLibraryPG1p0\resourceFiles\mSetupParams.py*) respectively show how to change the following lines of code from what is written in red to what is written in green to change some of the LMK dividers to output the correct FPGA clock for this application.

```
-       lmk.head.page.DCLK12_SDCLK13_controls.Out_control.dclkout_DIV_lt_4_0_gt_ = 12
+       lmk.head.page.DCLK12_SDCLK13_controls.Out_control.dclkout_DIV_lt_4_0_gt_ = int(round(divInputClk/setupParams.fpgaRefClk))
```

Figure 3-1. First Change in Line of Code, AFE77xxD GUI

```
-    fpgaRefClk = 245.76
+    fpgaRefClk = 368.64
```

Figure 3-2. Second Change in Line of Code, AFE77xxD GUI

2. Teraterm version 4.106
   a. Install any serial port terminal (Minicom or Gtkterm) to connect to the Agilex HPS (Arm node). In this guide, Teraterm is used.
3. PowerShell

4. Intel Quartus Programmer version 22.3
   a. Install only the “Intel® Quartus® Prime Pro Edition Programmer and Tools” under additional software: https://www.intel.com/content/www/us/en/software-kit/746667/intel-quartus-prime-pro-edition-design-software-version-22-3-for-windows.html
   b. There is also a patch on Intel’s website to fix a problem with this version: https://www.intel.com/content/www/us/en/support/programmable/articles/000092460.html.
5. IP Address Setup
   a. Set the IP address of the Ethernet port connected to the Agilex eSOM7 to 192.168.0.2. For steps on how to do this, see Appendix A.

4 Bring-Up Steps

The following section provides a step-by-step walkthrough of the reference design setup from a bring-up perspective, along with relevant screenshots of the process throughout.

Steps:

1. First, power on the Agilex eSOM7 TI Carrier and then power on the TI AFE7769DEVM.
2. Open Teraterm, click on "Serial", and click "OK".
3. Click on Setup > Serial port, see Figure 4-1.

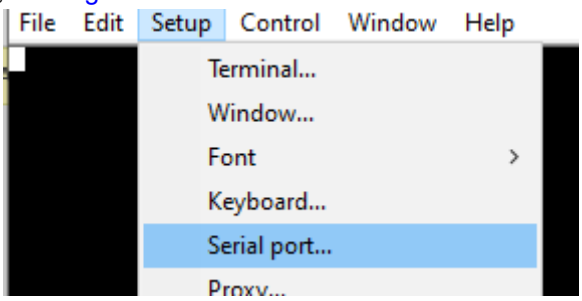

Figure 4-1. Opening Serial Port Window in Teraterm

4. A new window will appear. Select the COM port that the eSOM7 is connected to (not COM1). Change the speed to 115200 and click "Close and New open", see Figure 4-2.

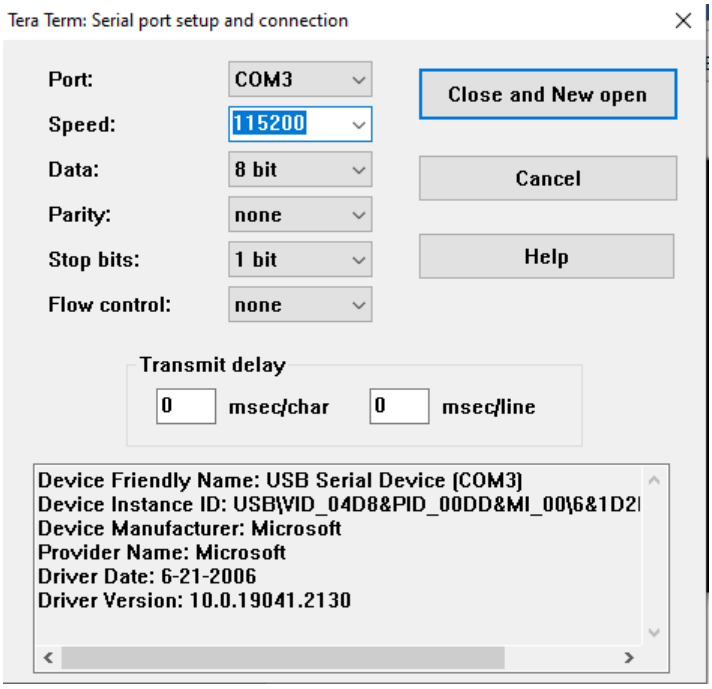

Figure 4-2. Serial Port Setup and Connection

5. You should now see "agilex login:", if you do not see any text, hit enter and "agilex login" will appear.
6. Type **root** and hit enter to login.

7. Get the IP address of the Arm node using the **ifconfig** command. If you do not see an "inet4" IP address under the eth0 interface, use the command **ifconfig eth0 192.168.0.1 netmask 255.255.255.0** to assign the 192.168.0.1 IP address to the eth0 interface, see Figure 4-3.

```
root@agilex:~# ifconfig eth0 192.168.0.1 netmask 255.255.255.0
root@agilex:~# ifconfig
eth0      Link encap:Ethernet  HWaddr 7A:AE:3A:51:8D:FC
          inet addr:192.168.0.1  Bcast:192.168.0.255  Mask:255.255.255.0
          inet6 addr: fe80::78ae:3aff:fe51:8dfc/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:7 errors:0 dropped:0 overruns:0 frame:0
          TX packets:22 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:446 (446.0 B)  TX bytes:4126 (4.0 KiB)
          Interrupt:21 Base address:0x6000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
```

Figure 4-3. IP Address Acquisition

8. On PowerShell, move your directory to the Hitek RF INTF release archive using the **cd < Hitek RF INTF release archive path>** command. In our setup, the command was **cd C:\Users\a0503061\Documents\Hitek\AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25**.
9. Copy the *software/arm_ag_/tools* folder from the *AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25* folder to the Arm node with the folder name as jesd_tools using the command **scp -r software/arm_ag/tools/ root@192.168.0.1:~/jesd_tools/**.
10. Start the TI AFE77xxD Latte GUI software and in the first dialog window titled "Latte Mode", make sure that FPGA_Type is set to "None" and the "AFE EVM Card Detected" message appears. The message "Couldn't Detect FPGA Reset FTDI. Reset FPGA manually." is expected. Then press "Continue" button to open the main Latte GUI. For proper navigation to Latte mode window, see Figure 4-4.

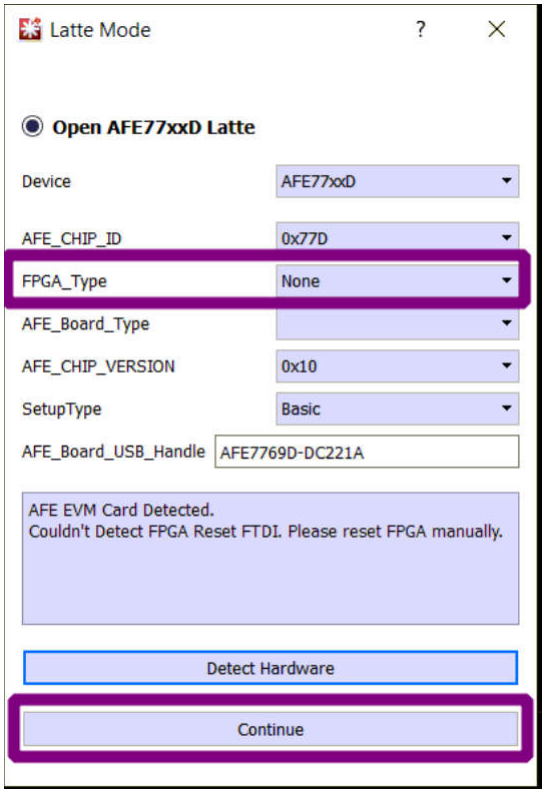

Figure 4-4. Launching the AFE77xxD Latte GUI

11. After the Latte software goes through its initialization steps, go to the AFE77xxD Params tab by clicking on AFE77xxD-Params on the left panel of the software window. Figure 4-5 shows how to navigate to the respective tab on the software panel.

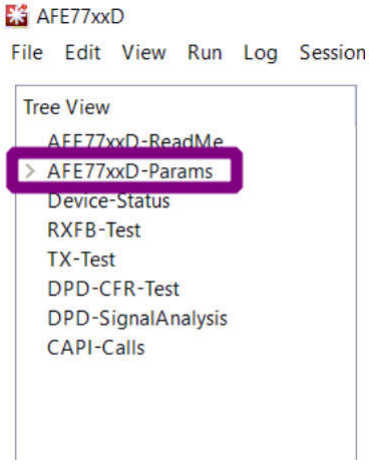

Figure 4-5. Navigating to AFE77xxD-Params

12. In the "Load System Parameters" box, click the "Browse" to search for the AFE77xxD_Config.json config file provided in *AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25\software\x64_64\utilities\AFE77xxDLatte_v0p4* and open it. For a view of the "AFE77xxD-Params" display and how to load the file, see Figure 4-6 and Figure 4-7, respectively.

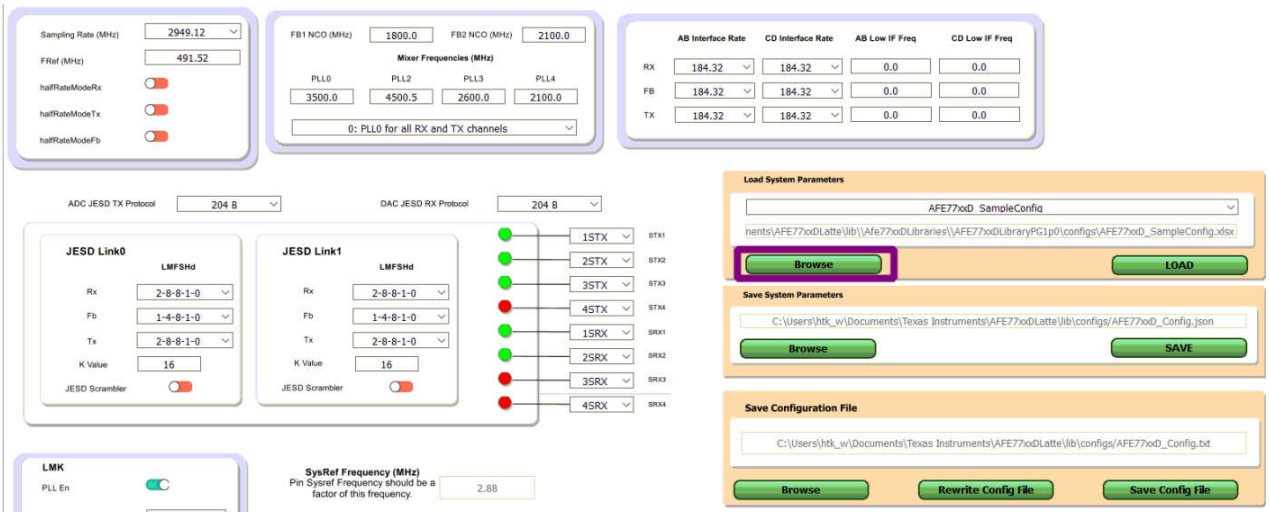

Figure 4-6. View of the AFE77xxD-Params Display

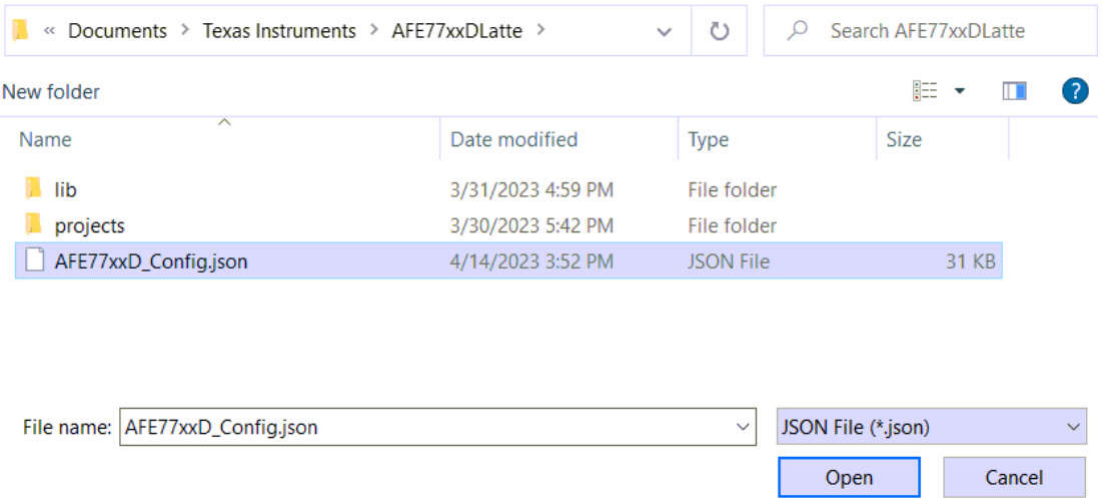

Figure 4-7. Loading the AFE77xxD Configuration File Into Latte

13. After selecting the configuration file, please click the "LOAD" button to load the configuration into the GUI. The GUI should change to the required configuration to be able to perform JESD link up with the JESD IP in the Agilex FPGA.
14. Open Quartus Prime Programmer and click the "Auto Detect" button. For navigation to the respective function, see Figure 4-8. If this is the first time the eSOM7 is connected to the PC and the "Auto Detect" button is grayed out, click on the "Hardware Setup..." button, select the "HTK USBII" in the drop down next to "Currently selected hardware" and check that the "Hardware frequency" is set to 24000000Hz.

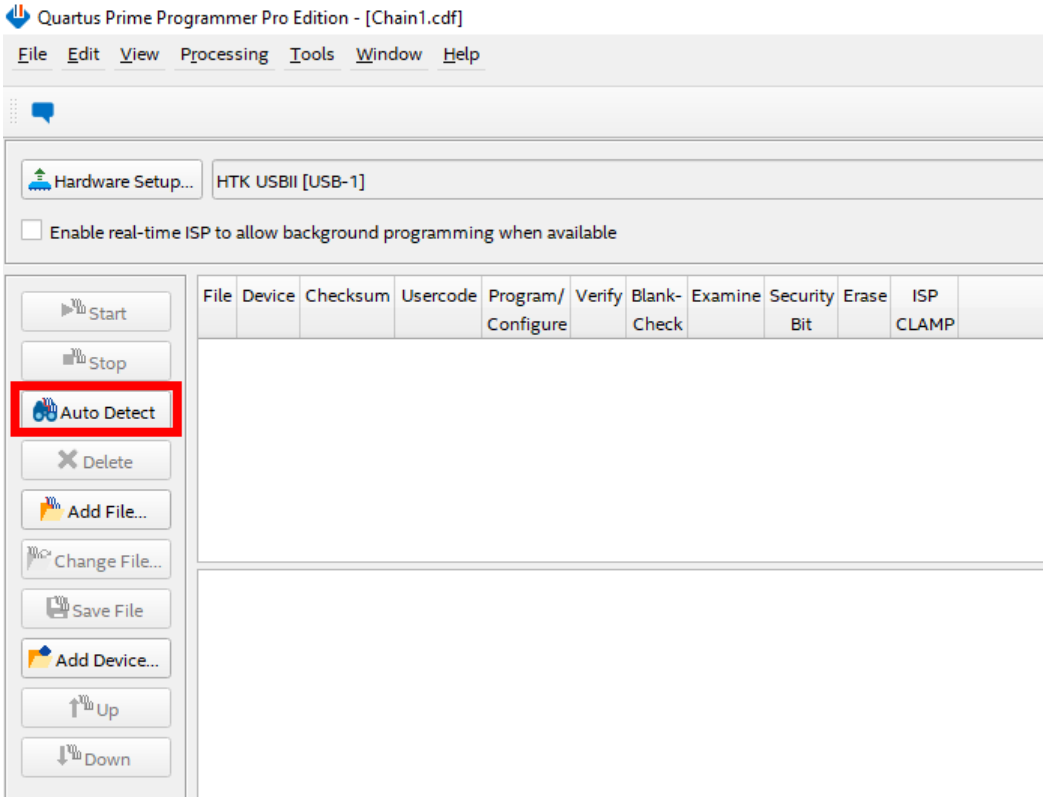

Figure 4-8. Auto Detect in Quartus Prime Programmer

15. After clicking "Auto Detect", a window will appear; select the AGFB027R24CR2 option and click "OK". Figure 4-9 shows the typical view when selecting a device.

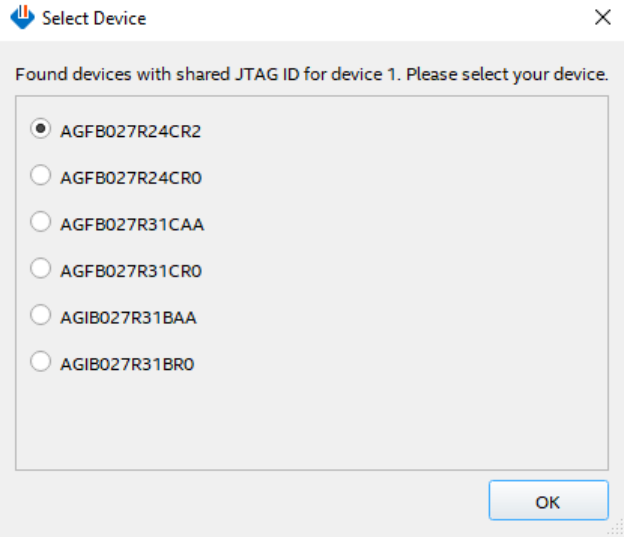

Figure 4-9. Device Selection

16. Select the only row under "File" and then click on “Change File”. Select the FPGA image called *ag_esom_top_afe77xx_jesd204c_4t4r2f_fpga_first_hps_auto.sof* that is provided in the directory *AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25\snapshots\hardware\fpga\agfb027_r24c_asyXX\ag_esom_top_afe77xx_jesd204c_4t4r2f_fpga_first_20230421_012455*, where "XX" should match the "ASY-XX-00047" label on the eSOM7 board. There is an extra copy of these files in a compressed .tar.gz folder. Figure 4-10 shows how to navigate to the proper functions.

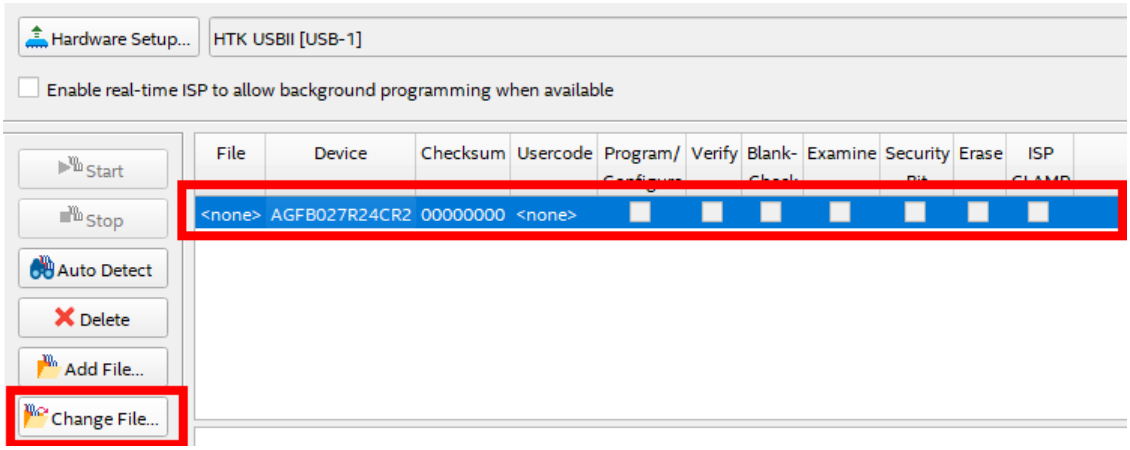

Figure 4-10. File Change

17. Next, check the box under "Program/Configure", see Figure 4-11.

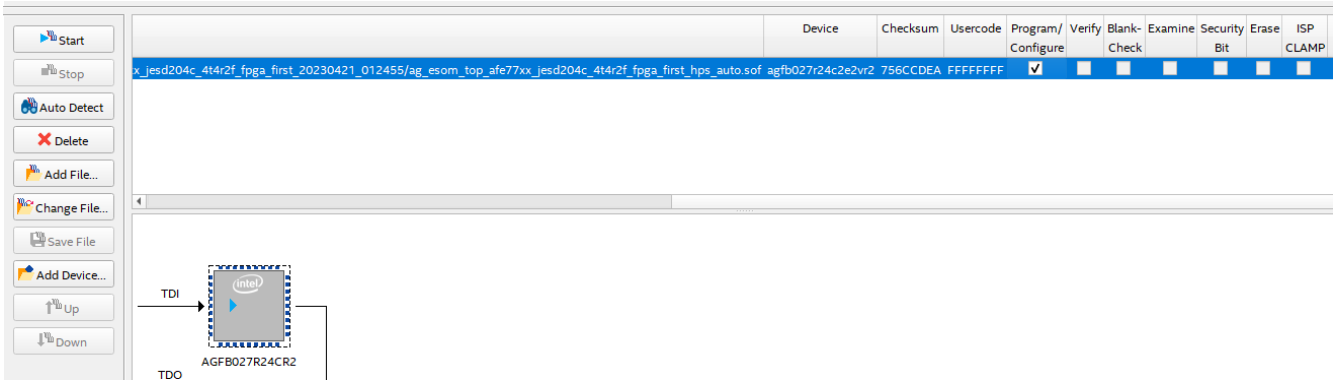

Figure 4-11. Program/Configure

18. On the AFE77xxD GUI, the “Device Bringup” button at the bottom of the AFE77xxD-Params page should be clicked to start the configuration of the LMK04828 and AFE7769D chips. Figure 4-12 shows how to navigate to the respective button.

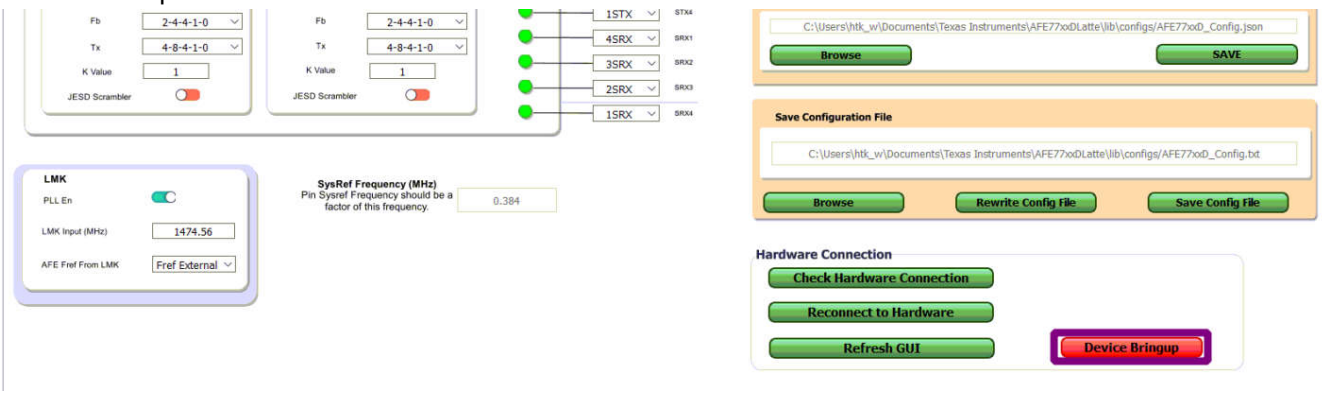

Figure 4-12. Device Bringup, AFE77xxD-Params

19. Once the “LMK Configured” message appears in the TI AFE77xxD Latte software log window indicating completion of the LMK04828 chip configuration, program the Agilex FPGA image by clicking the “Start” button on Quartus Prime Programmer. Figure 4-13 and Figure 4-14 show a visual reference of the steps to program the device.

Figure 4-13. Confirmation of LMK Configuration in the AFE77xxD Latte GUI

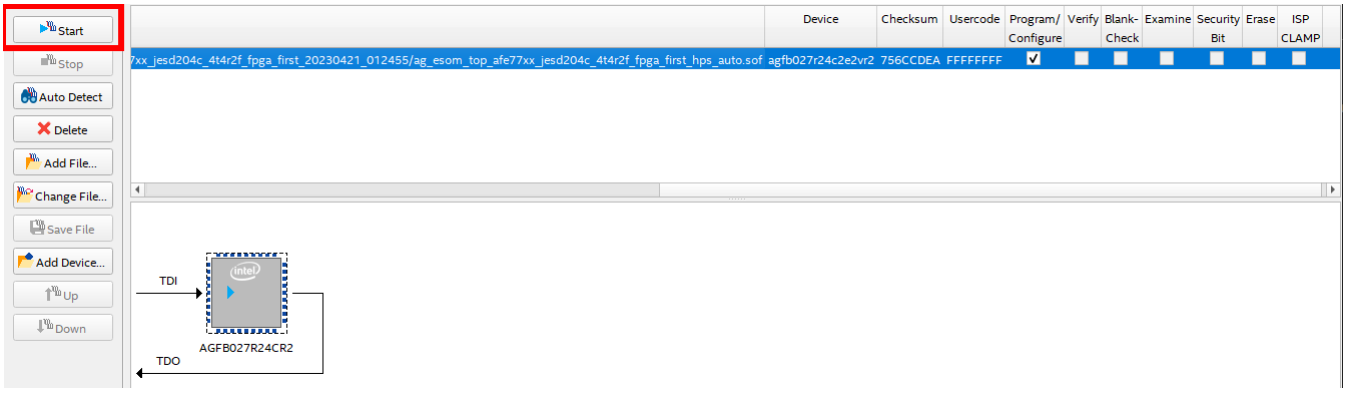

Figure 4-14. Clicking the Start Button to Program the Agilex FPGA

20. Wait for Linux bootup of the Arm node to show up on the Teraterm console and login with the **root** username. Then, use the command **source jesd_tools/init_term.sh** to execute the init_term.sh script in the jesd_tools folder, and run the **run_jesd_init_afe77xx_jesd204c_4t4r2f_board.sh** script on the Arm node. Do not hit enter yet. Figure 4-15 shows an example block of code.

```
Poky (Yocto Project Reference Distro) 3.4.2 agilex ttyS1

agilex login: root
Nov 19 17:19:43 agilex authpriv.notice login[201]: ROOT LOGIN  on '/dev/ttyS1'
root@agilex:~# source jesd_tools/init_term.sh
Setting I2C Device Environment Variables...
root@agilex:~# run_jesd_init_afe77xx_jesd204c_4t4r2f_board.sh
Checking F-Tile System PLL Lock Status
Reset ACKs are deasserted
Reset ACKs are asserted
Reset ACKs are deasserted
Press Enter to recalibrate FPGA XCVRs (Rx only) once AFE77XX eval. board bringup is complete
```

Figure 4-15. Initializing JESD IP in the Agilex FPGA

21. Wait until the AFE7769D configuration completes in the TI AFE77xxD Latte software where it should report successful JESD204C link up on the AFE7769D chip in the log window (note that the 2 errors related to FPGA reset failure are expected). Figure 4-16 shows the log window displaying that the device was able to get the link up for the device's JESD RX.

```
Log
AFE DPD Block configuration Complete
AFE RX IQMC configuration Complete
AFE RX AGC configuration Complete
Setting RBD to: 9
###########Device DAC JESD-RX 0 Link Status###########
CS State TX0: 0b10101010 . It is expected to be 0b10101010
BUF State TX0: 0b11111111 . It is expected to be 0b11111111
Could get the link up for device RX: 0
###################################
###########Device DAC JESD-RX 0 Link Status###########
CS State TX0: 0b10101010 . It is expected to be 0b10101010
BUF State TX0: 0b11111111 . It is expected to be 0b11111111
Could get the link up for device RX: 0
###################################
Setting RBD to: 6
###########Device DAC JESD-RX 0 Link Status###########
CS State TX0: 0b10101010 . It is expected to be 0b10101010
BUF State TX0: 0b11111111 . It is expected to be 0b11111111
Could get the link up for device RX: 0
###################################
AFE configuration Complete
#================ ERRORS:2, WARNINGS:0 ================#
```

Figure 4-16. AFE Configuration Complete Showing Link Up for the Device's JESD RX

22. After the AFE7769D configuration is complete in the TI AFE77xxD Latte software press enter on the Arm node (Teraterm) to recalibrate the FPGA XCVRs (Rx only) to complete the JESD204C link up on FPGA. Figure 4-17 shows the link status report in the FPGA.

```
root@agilex:~# run_jesd_init_afe77xx_jesd204c_4t4r2f_board.sh
Checking F-Tile System PLL Lock Status
Reset ACKs are deasserted
Reset ACKs are asserted
Reset ACKs are deasserted
Press Enter to recalibrate FPGA XCVRs (Rx only) once AFE77XX eval. board bringup is complete

Reset ACKs are deasserted
Reset ACKs are asserted
Reset ACKs are deasserted
Checking JESD Link Status ...
##########################################################################################################################################
##                                                      JESD Common Status                                                              ##
##########################################################################################################################################
## + Core PLL Locked                                   = Locked                                                                           ##
##########################################################################################################################################
##                                                      JESD TX Status                                                                  ##
##########################################################################################################################################
## + TX Link Ready                                     = Ready                                                                            ##
## + TX Interrupt                                      = Not asserted                                                                     ##
##########################################################################################################################################
##                                                      JESD RX/FB Status                                                               ##
##########################################################################################################################################
## + RX Link Ready                                     = Ready                                                                            ##
## + FB Link Ready                                     = Ready                                                                            ##
## + RX Interrupt                                      = Asserted                                                                         ##
## + FB Interrupt                                      = Asserted                                                                         ##
## + RX J204C Sync Header                              = Locked                                                                           ##
## + FB J204C Sync Header                              = Locked                                                                           ##
## + RX J204C EMB                                      = Locked                                                                           ##
## + FB J204C EMB                                      = Locked                                                                           ##
## + RX/FB J204C CRC Errors                            = None                                                                             ##
##########################################################################################################################################
root@agilex:~#
```

Figure 4-17. Completion of JESD204C Linkup With Status Report for the Link

23. Run the **ifconfig** command to see the IP address for the eth0 interface. Figure 4-18 shows an example block of code.

```
root@agilex:~# ifconfig
lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
```

a. If the eth0 interface does not appear like in the image above use the **ifconfig eth0 192.168.0.1 up** command to bring the interface up. Then use the **ifconfig eth0 192.168.0.1 netmask 255.255.255.0** command to set the IP address of the interface

b. Then, you can use the **ifconfig** command to check that the interface has the IP address assigned, see Figure 4-18 as reference.

```
root@agilex:~# ifconfig eth0 192.168.0.1 up
[ 2758.780518] socfpga-dwmac ff802000.ethernet eth0: PHY [stmmac-1:01] driver [Microchip KSZ9131 Gigabit PHY] (irq=P
OLL)
[ 2758.800494] socfpga-dwmac ff802000.ethernet eth0: No Safety Features support found
[ 2758.808091] socfpga-dwmac ff802000.ethernet eth0: IEEE 1588-2008 Advanced Timestamp supported
[ 2758.816905] socfpga-dwmac ff802000.ethernet eth0: registered PTP clock
[ 2758.824018] socfpga-dwmac ff802000.ethernet eth0: configuring for phy/rgmii-id link mode
root@agilex:~# [ 2761.894396] socfpga-dwmac ff802000.ethernet eth0: Link is Up - 10Mbps/Full - flow control off
[ 2761.902988] IPv6: ADDRCONF(NETDEV_CHANGE): eth0: link becomes ready
[ 2763.941004] socfpga-dwmac ff802000.ethernet eth0: Link is Down
[ 2767.015415] socfpga-dwmac ff802000.ethernet eth0: Link is Up - 1Gbps/Full - flow control rx/tx

root@agilex:~# ifconfig eth0 192.168.0.1 netmask 255.255.255.0
root@agilex:~# ifconfig
eth0      Link encap:Ethernet  HWaddr 7A:AE:3A:51:8D:FC
          inet addr:192.168.0.1  Bcast:192.168.0.255  Mask:255.255.255.0
          inet6 addr: fe80::78ae:3aff:fe51:8dfc/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:7 errors:0 dropped:0 overruns:0 frame:0
          TX packets:16 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:446 (446.0 B)  TX bytes:2501 (2.4 KiB)
          Interrupt:21 Base address:0x6000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
```

Figure 4-18. Confirmation That the eth0 Interface has the Correct IP Address

Figure 4-18. Eth0 Interface

24. To be able to output signals from the TX RF ports and input signals from the RX and FB RF ports, the "Channel TDD" needs to be set for the required channels under test. This is done by going to the "RXFB-Test" page in the AFE77xxD GUI by clicking on "RXFB-Test" on the left side of the software window. In the "Channel TDD" box on this page, click on the red dots to make them green, and finally click the "Set Tdd" button; see Figure 4-20.

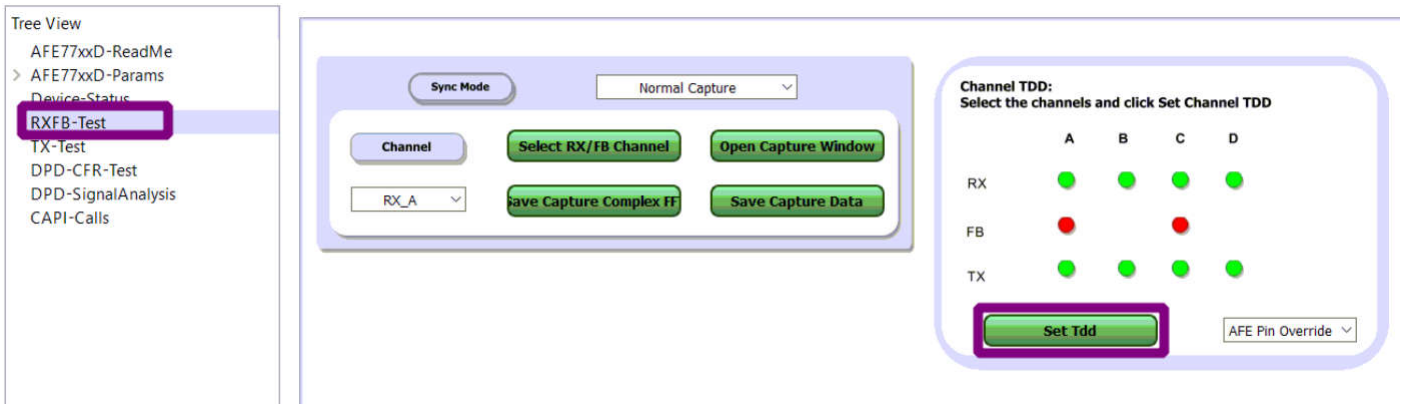

Figure 4-20. TDD Configuration for TX to RX Test

Note that when testing the FB channels, the TDD for the RX channels should not be set (such that, the dots for the RX channels are not green), see Figure 4-21.

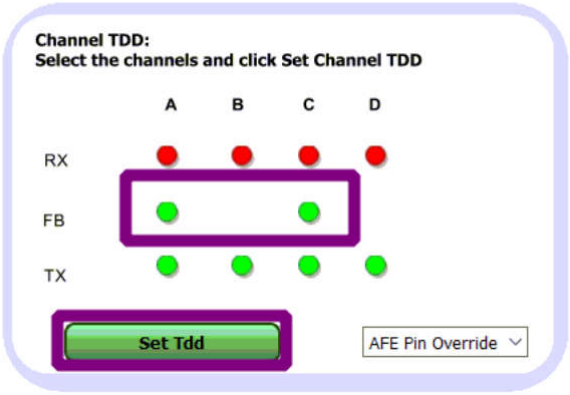

Figure 4-21. TDD Configuration for TX to FB Test

5 TX to FB Loopback With DDR Example

Steps:

1. Make sure that the SMA cables are connected so that the first two TX RF ports (TX1-TX2) are connected to the two FB RF ports (FB1-FB2, respectively).
2. Copy your waveform file from the host pc to the Arm node using the command **scp <path to the waveform file> root@192.168.0.1:/home/root/jesd_tools/data/** in PowerShell. For the setup, the command **scp .\jesd\TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt root@192.168.0.1:/home/root/jesd_tools/data/** was used.
   a. The format of the waveform file is such that each sample occupies a line with a 16-bit hex value for the I portion in the first column and a 16-bit hex value for the Q portion in the second column.
3. On the Arm node (Teraterm), run the command below to simultaneously playback the samples of the waveform to each of the first two TX channels channels from the FPGA and capture the samples from each of the two FB channels in 4T4R2F mode.
   a. **run_jesd_cw_lpbk_tests_with_ddr.sh -s=8 -n=2 -f=jesd_tools/data/TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt**
   b. The expected output is shown in Figure 5-1.

```
root@agilex:~# run_jesd_cw_lpbk_tests_with_ddr.sh -s=8 -n=2 -f=jesd_tools/data/TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt

Using /home/root/jesd_tools/data/TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt for looping playback of 7372800 samples from
DDR-A to TX0,TX1,TX2,TX3 channels
Created /home/root/jesd_tools/log/cw_capture_fb0.txt after capture of 65536 samples from FB0 channel to DDR-B
Created /home/root/jesd_tools/log/cw_capture_fb1.txt after capture of 65536 samples from FB1 channel to DDR-B
root@agilex:~#
```

Figure 5-1. Expected Output After Running the Loop-Back Command

4. At the end of the execution, there should be two capture files created with names of *cw_capture_fb[0-1].txt* in *jesd_tools/log* folder on the Arm node. Copy one of them to the host PC in the *Hitek_RF_INTF_Common_Files_2023-06-07\software\x64_64\analysis\jesd* folder using the command **scp root@192.168.0.1:/home/root/jesd_tools/log/cw_capture_fb0.txt <location to copy>**. In our setup the command, **scp root@192.168.0.1:/home/root/jesd_tools/log/cw_capture_fb0.txt jesd/** was used.
5. Run the **.\run_freq_plot.exe 2 .\\cw_capture_fb0.txt 737280000** command from the *Hitek_RF_INTF_Common_Files_2023-06-07\software\x64_64\analysis\jesd* directory to display a Fast Fourier Transform (FFT) with Hamming window of the FB capture. The FB is sampled at 737.28Msps in 4T4R2F mode and is shown in Figure 5-2. You can zoom in to adjust the view in the image.

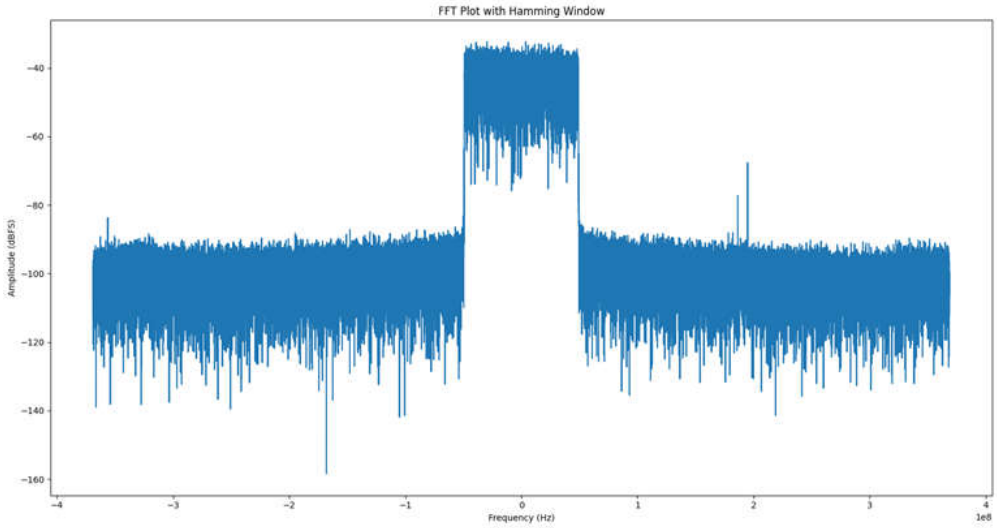

Figure 5-2. FFT Showing the Loop-Backed TM3.1a Waveform

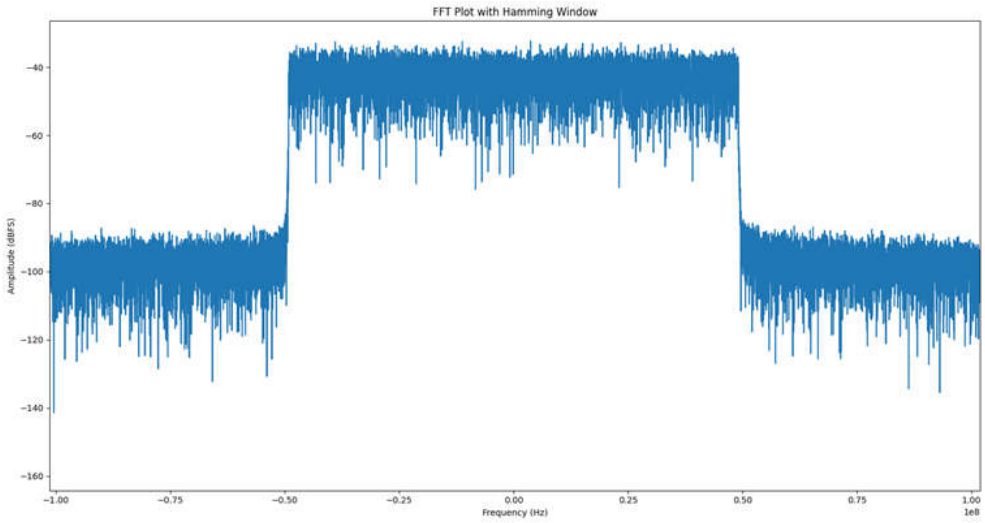

Figure 5-3. Zoom of the FFT Showing the Loop-Backed TM3.1a Waveform

A Setting Ethernet Port IP Address

1. Go to "Ethernet" under settings and double click on the "Ethernet" port connected to the Agilex eSOM7.

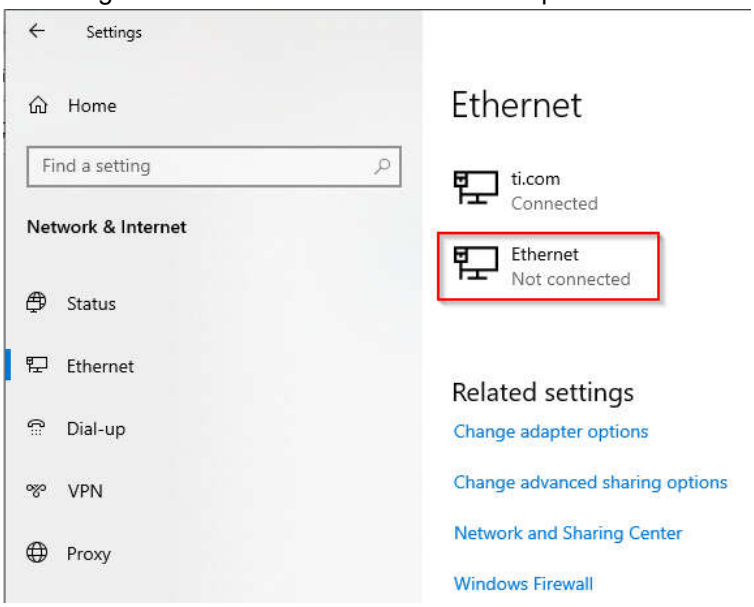

Figure A-1. Ethernet Settings

2. Under IP settings, click the “Edit” button and select “Manual” on the drop down to set the IP address manually as shown in Figure A-2. After changing the “IP address”, “Subnet prefix length”, and “Gateway” fields, click “Save”.

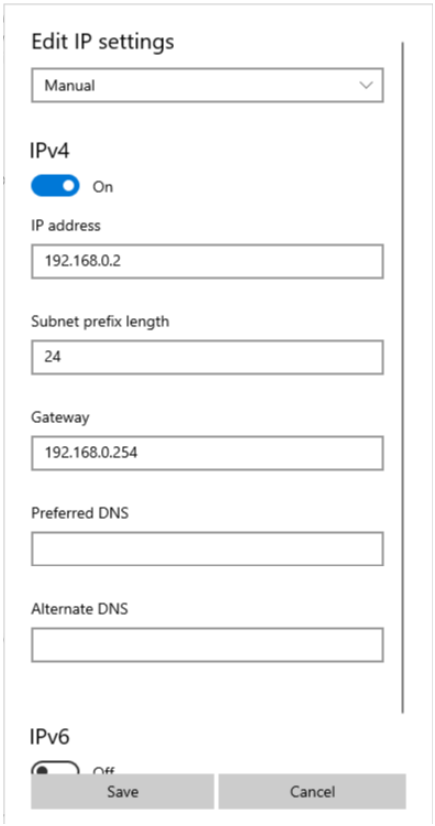

Figure A-2. Manually Setting IP Address

3. After that, open the Control Panel and navigate to “Control Panel\Network and Internet\Network and Sharing Center”. Then, click on the connection for the Agilex eSOM7 as shown in Figure A-3.

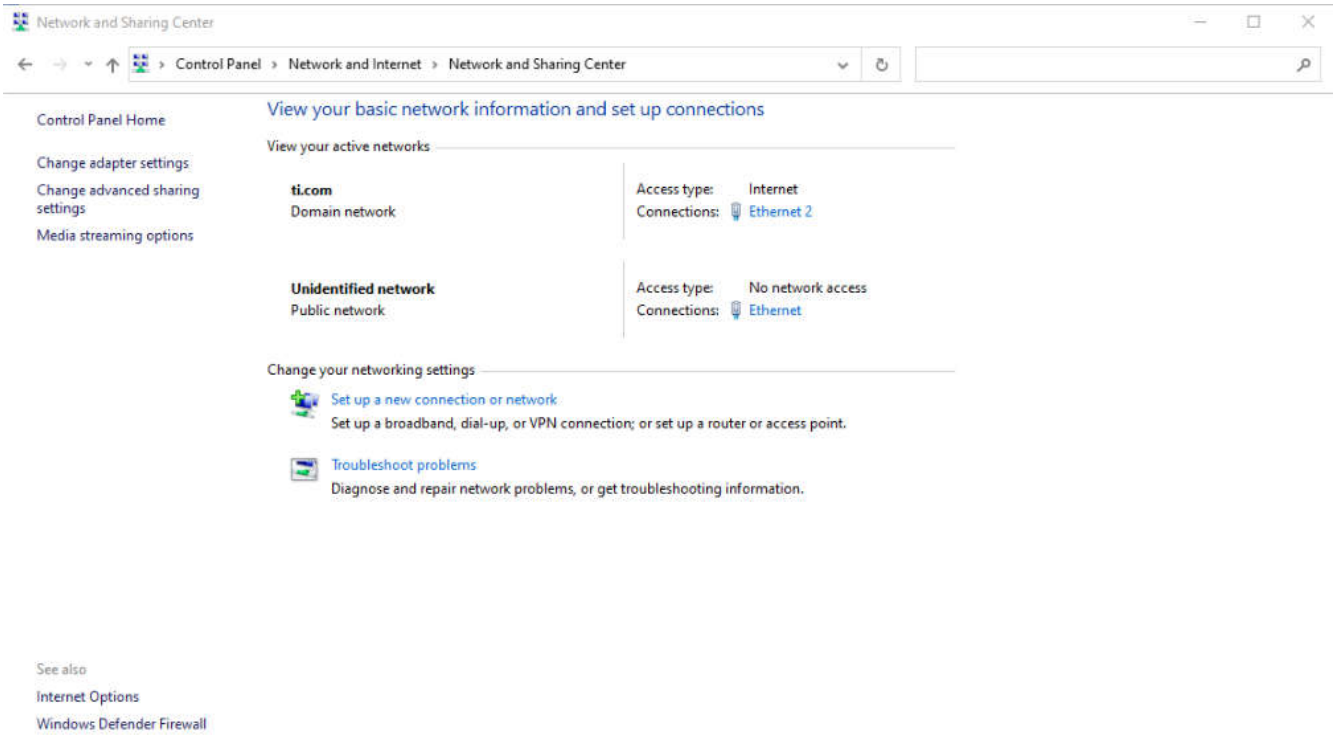

Figure A-3. Opening the Network in Control Panel

4. A window as shown in Figure A-4 will appear. Click the “Properties” button.

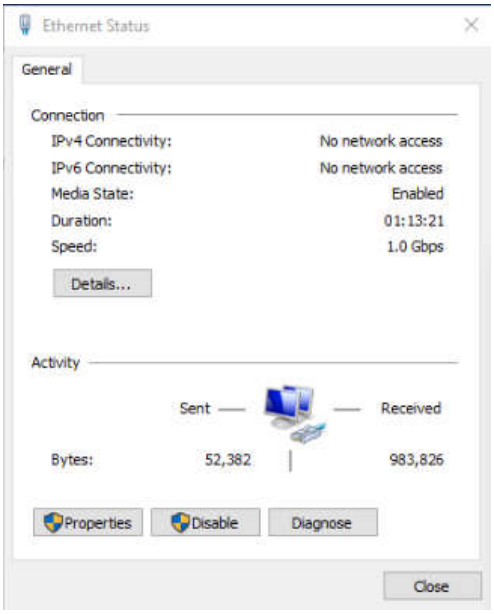

Figure A-4. Opening the Properties Tab for the Ethernet Connection

5. After that a window as shown in Figure A-5 will open. Double click the “Internet Protocol Version 4 (TCP/IPv4)” option to open its "Properties" tab.

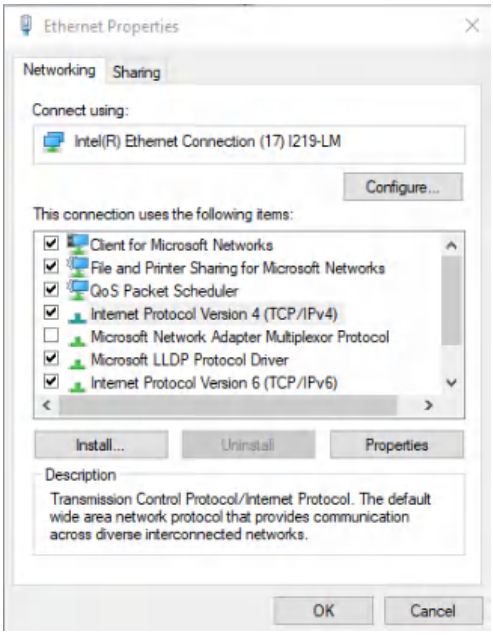

Figure A-5. Opening the IPv4 Properties

6. In the window that opens select the “Use the following IP address” option and fill out the fields as shown in Figure A-6. After filling out the fields click ok and the address will be set.

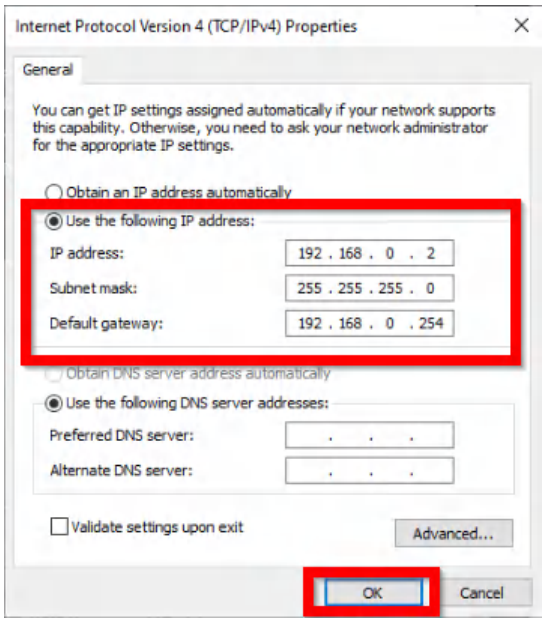

Figure A-6. Setting the IP Address Manually

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