User's Guide Interfacing AFE7769DEVM With the Hitek Agilex eSOM7 FPGA



ABSTRACT

This user's guide provides a walkthrough of hardware and software setup with supplemental images as a visual representation, followed by bringup steps, a loop-back example and a loop-back test using an LTE signal.

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1 Introduction

This user's guide introduces a wireless development platform using Texas Instruments' AFE7769D evaluation module (EVM) in collaboration with Hitek Systems, a hardware company and partner of Intel that provides field programmable gated array (FPGA)-based evaluation modules to companies within the communications industry. This reference solution serves to help customers ramp up system integration of the analog front-end (AFE), and provides a "quick evaluation and prototyping platform for 5G ORAN and wireless solutions", per Hitek Systems.

The AFE7769D is a 4T4R2F RF-sampling transceiver with integrated digital pre-distortion (DPD) that serves to linearize power amplifiers (PA's) for improved wireless coverage to the end customer. The wireless development platform utilizes the EVM version of the device, which interfaces with Hitek's component of the solution via an FPGA mezzanine card (FMC+) connector. The Agilex embedded System On Module (eSOM7) is an FPGA module that interacts with the AFE7769DEVM through the FMC+ connector. This hardware is based on Intel Agilex[®] 7 SoC FPGA built using intel 10 nm SuperFin process technology.

For the following sections of the document, commands are **bolded**, file paths, folders, and names are *italicized*, and titles in user interfaces are in "quotes".

2 Hardware Setup

The following section provides a step-by-step walkthrough of the reference design setup from a hardware (HW) perspective, along with a visual representation of the setup at the end.

Steps:

2

- 1. Mount the Agilex Embedded SOM7 (eSOM7) on the TI carrier board.
- 2. Mount the AFE7769DEVM on the FMC+ slot of the TI carrier board.
- 3. Plug the +12V 6-pin ATX PCIe power connector into the TI carrier.
- Connect a micro USB from the host PC to the USB connector J23 of the TI carrier for UART access to HPS (Arm[®] node).
- 5. Connect a micro USB from the host PC to the USB connector J24 of the TI carrier for programming the Agilex FPGA image containing RF Interface framework over JTAG.
- 6. Connect an Ethernet cable to the RJ45 port (J21) of the TI carrier for transferring files across the network.
- 7. Connect a 5.5V, 5A power supply to the TI AFE7769DEVM.
- Connect a mini-USB cable between host PC (Windows) and mini-USB port on TI AFE7769D evaluation card for configuring the chips on the evaluation card using customized TI AFE77xxD Latte software (version 0.4.0) with the provided configuration file.
- 9. SMA cables connected from TX RF ports to RX/FB RF ports.
 - a. Connections should be as follows for TX to RX RF ports:
 - i. TX1 (J7) to RX1 (J1)
 - ii. TX2 (J8) to RX2 (J2)
 - iii. TX3 (J9) to RX3 (J3)
 - iv. TX4 (J10) to RX4 (J4)
 - b. Connections should be as follows for TX to FB RF ports:
 - i. TX1 (J7) to FB1 (J5)
 - ii. TX2 (J8) to FB2 (J6)

When powering on the HW setup, power on the Agilex eSOM7 TI Carrier before powering on the TI AFE7769DEVM. When powering off the HW setup, power off the TI AFE7769DEVM before powering off the Agilex eSOM7 TI Carrier. For the end result of the HW setup, see Figure 2-1.

Note

The Agilex eSOM7 can come with a Skyworks Si5518 timing module (ASY-00-00048 Rev 2). This is not required for the purposes of this guide.





Figure 2-1. Hardware Setup, AFE7769DEVM and Agilex eSOM7

3 Software Setup

The following section provides a step-by-step walkthrough of the reference design setup from a software (SW) perspective, along with screenshots of the process throughout. A folder with the required files can be found in the following link <>. Installers for Quartus Programmer, Teraterm, and Powershell are available online.

Steps:

Install the following elements of software:

- 1. AFE77xxD Graphical User Interface (GUI) version 0.4.0
 - a. Make the following changes to the files in the *Documents\Texas Instruments\AFE77xxDLatte* folder:
 - i. Figure 3-1 (*lib\Afe77xxDLibraries\AFE77xxDLibraryPG1p0\resourceFiles\mLmk.py*) and Figure 3-2 (*lib\Afe77xxDLibraries\AFE77xxDLibraryPG1p0\resourceFiles\mSetupParams.py*) respectively show how to change the following lines of code from what is written in red to what is written in green to change some of the LMK dividers to output the correct FPGA clock for this application.

- tmk.head.page.bttk12_S0ttk13_controls.out_control.dctkout_DIV_tt_4_0_gt_ = 12
+ lmk.head.page.DCLK12_SDCLK13_controls.Out_control.dclkout_DIV_tt_4_0_gt_ = int(round(divInputClk/setupParams.fpgaRefClk))





Figure 3-2. Second Change in Line of Code, AFE77xxD GUI

- 2. Teraterm version 4.106
 - a. Install any serial port terminal (Minicom or Gtkterm) to connect to the Agilex HPS (Arm node). In this guide, Teraterm is used.
- 3. PowerShell



- 4. Intel Quartus Programmer version 22.3
 - a. Install only the "Intel® Quartus® Prime Pro Edition Programmer and Tools" under additional software: https://www.intel.com/content/www/us/en/software-kit/746667/intel-quartus-prime-pro-edition-design-software-version-22-3-for-windows.html
 - b. There is also a patch on Intel's website to fix a problem with this version: https://www.intel.com/ content/www/us/en/support/programmable/articles/000092460.html.
- 5. IP Address Setup
 - a. Set the IP address of the Ethernet port connected to the Agilex eSOM7 to 192.168.0.2. For steps on how to do this, see Appendix A.

4 Bring-Up Steps

The following section provides a step-by-step walkthrough of the reference design setup from a bring-up perspective, along with relevant screenshots of the process throughout.

Steps:

- 1. First, power on the Agilex eSOM7 TI Carrier and then power on the TI AFE7769DEVM.
- 2. Open Teraterm, click on "Serial", and click "OK".
- 3. Click on Setup > Serial port, see Figure 4-1.





4. A new window will appear. Select the COM port that the eSOM7 is connected to (not COM1). Change the speed to 115200 and click "Close and New open", see Figure 4-2.

Tera Term: Serial port setup	and connectio	n	×					
Port: Speed:	COM3	~	Close and New open					
Data:	8 bit	\sim	Cancel					
Parity:	none	\sim						
Stop bits:	1 bit	\sim	Help					
Flow control:	none	\sim						
Transmit delay 0 msec/char 0 msec/line								
Device Friendly Name: USB Serial Device [COM3] Device Instance ID: USB\VID_04D8&PID_00DD&MI_00\6&1D2 Device Manufacturer: Microsoft Provider Name: Microsoft Driver Date: 6-21-2006 Driver Version: 10.0.19041.2130								
<			>					

Figure 4-2. Serial Port Setup and Connection

- 5. You should now see "agilex login:", if you do not see any text, hit enter and "agilex login" will appear.
- 6. Type **root** and hit enter to login.

 Get the IP address of the Arm node using the ifconfig command. If you do not see an "inet4" IP address under the eth0 interface, use the command ifconfig eth0 192.168.0.1 netmask 255.255.255.0 to assign the 192.168.0.1 IP address to the eth0 interface, see Figure 4-3.

rootCagil	ex:~# ifconfig eth0 192.168.0.1 netmask 255.255.255.0
FUDCEAGIT	
eth0	Link encap:Ethernet HWaddr 7A:AE:3A:51:8D:FC
	inet addr:192.168.0.1 Bcast:192.168.0.255 Mask:255.255.255.0
	inet6 addr: fe80::78ae:3aff:fe51:8dfc/64 Scope:Link
	UP BROADCAST RUNNING MULTICAST MTU:1500 Metric:1
	RX packets:7 errors:0 dropped:0 overruns:0 frame:0
	TX packets:22 errors:0 dropped:0 overruns:0 carrier:0
	collisions:0 txqueuelen:1000
	RX butes:446 (446.0 B) TX butes:4126 (4.0 KiB)
	Interrupt:21 Base address:0x6000
10	Link encap:Local_Loopback
	inet_addr:127.0.0.1 _Mask:255.0.0.0
	inet6 addr: ::1/128 Scope:Host

Figure 4-3. IP Address Acquisition

- On PowerShell, move your directory to the Hitek RF INTF release archive using the cd < Hitek RF INTF release archive path> command. In our setup, the command was cd C:\Users\a0503061\Documents\Hitek\AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-2 5.
- Copy the software/arm_ag_/tools folder from the AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25 folder to the Arm node with the folder name as jesd_tools using the command scp -r software/arm_ag/tools/ root@192.168.0.1:~/jesd_tools/.
- 10. Start the TI AFE77xxD Latte GUI software and in the first dialog window titled "Latte Mode", make sure that FPGA_Type is set to "None" and the "AFE EVM Card Detected" message appears. The message "Couldn't Detect FPGA Reset FTDI. Reset FPGA manually." is expected. Then press "Continue" button to open the main Latte GUI. For proper navigation to Latte mode window, see Figure 4-4.

🕌 Latte Mode	? ×						
Open AFE77xxD Latte							
Device	AFE77xxD 👻						
AFE_CHIP_ID	0x77D 👻						
FPGA_Туре	None 👻						
AFE_Board_Type	.						
AFE_CHIP_VERSION	0x10 ×						
SetupType	Basic 👻						
AFE_Board_USB_Handle AFE7769D-DC221A							
AFE EVM Card Detected. Couldn't Detect FPGA Reset FTDI. Please reset FPGA manually.							
Detect H	lardware						
Continue							

Figure 4-4. Launching the AFE77xxD Latte GUI



11. After the Latte software goes through its initialization steps, go to the AFE77xxD Params tab by clicking on AFE77xxD-Params on the left panel of the software window. Figure 4-5 shows how to navigate to the respective tab on the software panel.



Figure 4-5. Navigating to AFE77xxD-Params

12. In the "Load System Parameters" box, click the "Browse" to search for the AFE77xxD_Config.json config file provided in

AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25\software\x64_64\utilities\AFE77xxDLat te_v0p4 and open it. For a view of the "AFE77xxD-Params" display and how to load the file, see Figure 4-6 and Figure 4-7, respectively.

ADC JESD TX Protocol 204 B	DAC JESD RX Protocol 204 B	. I	Load System Parameters
JESD Link0 JESD		STX V STX2	AFE77xoD SampleConfig
Rx 2-8-8-1-0 R Fb 1-4-8-1-0 FI Tx 2-8-8-1-0 T K Value 16 K Value	Larono 33 2-8-8-1-0 45 1-4-8-1-0 45 2-8-8-1-0 5 tate 16	TX V STX0 TX V STX4 SRX V SRX1 SRX SRU2 SRX SRU2	Seve System Parameters C:\Users\htc.w\Documents\Texas Instruments\AFE77xx0Latte\htb\configs\AFE77xx0_Config.json Browse SAVE
JESD Scrambler		IRX V BRX4	Save Configuration File C:\Users\htk_w\Documents\Texas Instruments\AFE77xdDLatte\Ub\configs/AFE77xdD_Config.txt

Figure 4-6. View of the AFE77xxD-Params Display



Name Date modified Type Size lib 3/31/2023 4:59 PM File folder projects 3/30/2023 5:42 PM File folder
lib 3/31/2023 4:59 PM File folder projects 3/30/2023 5:42 PM File folder
projects 3/30/2023 5:42 PM File folder
projects system interorder
AFE77xxD_Config.json 4/14/2023 3:52 PM JSON File 31 KB

Figure 4-7. Loading the AFE77xxD Configuration File Into Latte

- 13. After selecting the configuration file, please click the "LOAD" button to load the configuration into the GUI. The GUI should change to the required configuration to be able to perform JESD link up with the JESD IP in the Agilex FPGA.
- 14. Open Quartus Prime Programmer and click the "Auto Detect" button. For navigation to the respective function, see Figure 4-8. If this is the first time the eSOM7 is connected to the PC and the "Auto Detect" button is grayed out, click on the "Hardware Setup..." button, select the "HTK USBII" in the drop down next to "Currently selected hardware" and check that the "Hardware frequency" is set to 24000000Hz.

Quartus P	rime P	rog	ramn	ner Pro E	Edition - [Chain1.	cdf]								
ile <u>E</u> dit	<u>V</u> iew	PI	oces	sing <u>T</u>	ools <u>W</u>	indow	<u>H</u> elp								
-															
-															
📥 Hardwa	re Setu	ıp	н	K USBII	[USB-1]										
Enable r	eal-tim	ne IS	SP to	allow ba	ackground	d progra	mmir	ng when ava	ailable						
. 10			File	Device	Checksu	m Use	rcode	Program/	Verify	Blank-	Examine	Security	Erase	ISP	
^{™™} Sta	rt							Configure		Check		Bit		CLAMP	
[™] Sto	р														
	etect	1													
W Addo D	cicci														
× Dele	ete														
🏓 Add F	ile														
Change	File														
r10.															
Save	File														
📌 Add De	vice														
1 ¹⁰⁰ Up	0														
= = = =															
1 [™] Dov	vn														

Figure 4-8. Auto Detect in Quartus Prime Programmer



15. After clicking "Auto Detect", a window will appear; select the AGFB027R24CR2 option and click "OK". Figure 4-9 shows the typical view when selecting a device.

		for device 1. P	lease select your	uevio
 AGFB027R24CR AGFB027R24CR 	0			
O AGFB027R31CA	A			
O AGFB027R31CR	0			
O AGIB027R31BAA	x			
)			

Figure 4-9. Device Selection

16. Select the only row under "File" and then click on "Change File". Select the FPGA image called ag_esom_top_afe77xx_jesd204c_4t4r2f_fpga_first_hps_auto.sof that is provided in the directory AG_eSOM_AFE77XX_RF_INTF_DEMO_Release_v3_3_2023-04-25\snapshots\hardware\fpga\agfb027_r24 c_asyXX\ag_esom_top_afe77xx_jesd204c_4t4r2f_fpga_first_20230421_012455, where "XX" should match the "ASY-XX-00047" label on the eSOM7 board. There is an extra copy of these files in a compressed .tar.gz folder. Figure 4-10 shows how to navigate to the proper functions.

Ardware Setup HTK USBII [USB-1]												
Enable real-time	ISP to allow	w background prog	gramming w	hen availab	ole							
▶ [™] Start	File	Device	Checksum	Usercode	Program/	Verify	Blank-	Examine	Security	Erase	ISP	
Stop	<none></none>	AGFB027R24CR2	00000000	<none></none>								
Huto Detect												
× Delete												
Add File												
隆 Change File												

Figure 4-10. File Change

17. Next, check the box under "Program/Configure", see Figure 4-11.



Figure 4-11. Program/Configure



 On the AFE77xxD GUI, the "Device Bringup" button at the bottom of the AFE77xxD-Params page should be clicked to start the configuration of the LMK04828 and AFE7769D chips. Figure 4-12 shows how to navigate to the respective button.

Fb 2-4-4-1-0 ×	Fb 2-4-4-1-0 V	ISTX V STX4
2444-1-0	2-4-4-1-0	C:\Users\htk_w\Documents\Texas Instruments\AFE77xxDLatte\lib\configs/AFE77xxD_Config.json
Tx 4-8-4-1-0 ~	Tx 4-8-4-1-0 ×	Browse SAVE
K Value 1	K Value 1	350
JESD Scrambler	JESD Scrambler	2SRX V SRO
	•+	1SRX V SRX4 Save Configuration File
L.En C	Syster requency (MH2) Pin Syster Frequency should be a factor of this frequency.	Browse Rewrite Config File Save Config File
E Fref From LMK Fref External V		Check Hardware Connection
		Contract of the define t

Figure 4-12. Device Bringup, AFE77xxD-Params

19. Once the "LMK Configured" message appears in the TI AFE77xxD Latte software log window indicating completion of the LMK04828 chip configuration, program the Agilex FPGA image by clicking the "Start" button on Quartus Prime Programmer. Figure 4-13 and Figure 4-14 show a visual reference of the steps to program the device.

Log	8
laneRateRx: 24330.24	^
laneRateRx1: 24330.24	1186311
laneRateFb: 24330.24	
laneRateTx0: 24330.24	
laneRateTx1: 24330.24	
DONOT_OPEN_Afe77xxDPG1p0_FULL - Device registers reset.	
chipType: 0xa	
chipId: 0x77d	
chipVersion: 0x10	
LMK Clock Divider - Device registers reset.	
LMK Clock Divider - Device registers reset.	
REECLOCK is used from LMK source, ensure board connections are ok to do the same	
LMK Configured.	
Puse farm load autoload done successful	
No autioad error	
Fuse farm load autoload done successful	
No autioad error	
AFE Reset Done.	
pll1: True; LO Frequency: 2949.12	~



▶ [™] Start		Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
■ ³ Stop	7xx_jesd204c_4t4r2f_fpga_first_20230421_012455/ag_esom_top_afe77xx_jesd204c_4t4r2f_fpga_first_hps_auto.sc	f agfb027r24c2e2vr2	756CCDEA	FFFFFFF	V						
Auto Detect											
× Delete											
Add File											
隆 Change File)
Save File											
Add Device	(me)										
↑ [™] up ↓ [™] Down											
	AGFB027R24CR2										

Figure 4-14. Clicking the Start Button to Program the Agilex FPGA



20. Wait for Linux bootup of the Arm node to show up on the Teraterm console and login with the root username. Then, use the command source jesd_tools/init_term.sh to execute the init_term.sh script in the jesd_tools folder, and run the run_jesd_init_afe77xx_jesd204c_4t4r2f_board.sh script on the Arm node. Do not hit enter yet. Figure 4-15 shows an example block of code.



Figure 4-15. Initializing JESD IP in the Agilex FPGA

21. Wait until the AFE7769D configuration completes in the TI AFE77xxD Latte software where it should report successful JESD204C link up on the AFE7769D chip in the log window (note that the 2 errors related to FPGA reset failure are expected). Figure 4-16 shows the log window displaying that the device was able to get the link up for the device's JESD RX.



Figure 4-16. AFE Configuration Complete Showing Link Up for the Device's JESD RX



22. After the AFE7769D configuration is complete in the TI AFE77xxD Latte software press enter on the Arm node (Teraterm) to recalibrate the FPGA XCVRs (Rx only) to complete the JESD204C link up on FPGA.

Figure 4-17 shows the link status	s report in the FFGA.	
root@agilex:~# run_jesd_init_afe77xx_jesd204c	_4t4r2f_board.sh	
Checking F-Tile System PLL Lock Status		
Reset ACKs are deasserted		
Reset ACKs are asserted		
Reset ACKs are deasserted		
Press Enter to recalibrate FPGA XCVRs (Rx onl	y) once AFE77XX eval. board bringup is complete	
Reset ACKs are deasserted		
Reset ACKs are asserted		
Reset ACKs are deasserted		
Checking JESD Link Status		
***********		*************************
##	JESD Common Status	##
***********	***************************************	************************
## + Core PLL Locked	= Locked	##
***************************************	***************************************	**********
##	JESD TX Status	##
***************************************	************	********
## + TX Link Ready	= Ready	##
## + TX Interrupt	= Not asserted	##
***************************************	***************************************	***********************
##	JESD RX/FB Status	##
***************************************		************************
## + RX Link Ready	= Ready	##
## + FB Link Ready	= Ready	##
## + RX Interrupt	= Asserted	##
## + FB Interrupt	= Asserted	##
## + RX J204C Sync Header	= Locked	##
## + FB J204C Sync Header	= Locked	##
## + RX J204C EMB	= Locked	##
## + FB J204C EMB	= Locked	##
## + RX/FB J204C CRC Errors	= None	##
*******	***************************************	*******
root@agilex:~#		

Figure 4-17. Completion of JESD204C Linkup With Status Report for the Link

23. Run the **ifconfig** command to see the IP address for the eth0 interface. Figure 4-18 shows an example block of code.

rootlagilex:"# ifconfig	
lo Link encap:Local Loopback	
inet addr:127.0.0.1 Mask:255.0.0.0	
inet6 addr: ::1/128 Scope:Host	
UP LOOPBACK RUNNING MTU:65536 Metric:1	
RX packets:0 errors:0 dropped:0 overruns:0 frame:	5
TX packets:0 errors:0 dropped:0 overruns:0 carrie	r:0
collisions:0 txqueuelen:1000	
RX bytes: $0 \langle 0.0 B \rangle$ TX bytes: $0 \langle 0.0 B \rangle$	

- a. If the eth0 interface does not appear like in the image above use the **ifconfig eth0 192.168.0.1 up** command to bring the interface up. Then use the **ifconfig eth0 192.168.0.1 netmask 255.255.255.0** command to set the IP address of the interface
- b. Then, you can use the **ifconfig** command to check that the interface has the IP address assigned, see Figure 4-18 as reference.

Figure 4-18. Confirmation That the eth0 Interface has the Correct IP Address

Figure 4-18. Eth0 Interface



24. To be able to output signals from the TX RF ports and input signals from the RX and FB RF ports, the "Channel TDD" needs to be set for the required channels under test. This is done by going to the "RXFB-Test" page in the AFE77xxD GUI by clicking on "RXFB-Test" on the left side of the software window. In the "Channel TDD" box on this page, click on the red dots to make them green, and finally click the "Set Tdd" button; see Figure 4-20.

Tree View AFE77xxD-ReadMe > AFE77xxD-Params Device-Status	Sync Mode Normal Capture V Channel TDD: Select the channels and click Set Channel TDD	7
RXFB-Test TX-Test	Channel Select RX/FB Channel Open Capture Window A B C D	
DPD-CFR-Test DPD-SignalAnalysis	RX A Y Bave Canture Complex FF Save Canture Data	
CAPI-Calls	FB FB	
	тх • • •	
	Set Tdd AFE Pin Override	3



Note that when testing the FB channels, the TDD for the RX channels should not be set (such that, the dots for the RX channels are not green), see Figure 4-21.





5 TX to FB Loopback With DDR Example

Steps:

- 1. Make sure that the SMA cables are connected so that the first two TX RF ports (TX1-TX2) are connected to the two FB RF ports (FB1-FB2, respectively).
- Copy your waveform file from the host pc to the Arm node using the command scp <path to the waveform file> root@192.168.0.1:/home/root/jesd_tools/data/ in PowerShell. For the setup, the command scp .\jesd\TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt root@192.168.0.1:/home/root/jesd_tools/data/ was used.
 - a. The format of the waveform file is such that each sample occupies a line with a 16-bit hex value for the I portion in the first column and a 16-bit hex value for the Q portion in the second column.
- 3. On the Arm node (Teraterm), run the command below to simultaneously playback the samples of the waveform to each of the first two TX channels channels from the FPGA and capture the samples from each of the two FB channels in 4T4R2F mode.
 - a. run_jesd_cw_lpbk_tests_with_ddr.sh -s=8 -n=2 -f=jesd_tools/data/ TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt
 - b. The expected output is shown in Figure 5-1.



root@agilex:~# run_jesd_cw_lpbk_tests_with_ddr.sh -s=8 -n=2 -f=jesd_tools/data/TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt Jsing /home/root/jesd_tools/data/TM3.1a_FDD_737.28MHz_eSOM_ACLRver.txt for looping playback of 7372800 samples from DDR-A to TX0.TX1.TX2.TX3 channels Created /home/root/jesd_tools/log/cw_capture_fb0.txt after capture of 65536 samples from FB0 channel to DDR-B Created /home/root/jesd_tools/log/cw_capture_fb1.txt after capture of 65536 samples from FB1 channel to DDR-B

Figure 5-1. Expected Output After Running the Loop-Back Command

- 4. At the end of the execution, there should be two capture files created with names of cw_capture_fb[0-1].txt in jesd_tools/log folder on the Arm node. Copy one of them to the host PC in the Hitek_RF_INTF_Common_Files_2023-06-07\software\x64_64\analysis\jesd folder using the command scp root@192.168.0.1:/home/root/jesd_tools/log/cw_capture_fb0.txt <location to copy>. In our setup the command, scp root@192.168.0.1:/home/root/jesd_tools/log/cw_capture_fb0.txt jesd/ was used.
- Run the .\run_freq_plot.exe 2 .\\cw_capture_fb0.txt 737280000 command from the *Hitek_RF_INTF_Common_Files_2023-06-07\software\x64_64\analysis\jesd* directory to display a Fast Fourier Transform (FFT) with Hamming window of the FB capture. The FB is sampled at 737.28Msps in 4T4R2F mode and is shown in Figure 5-2. You can zoom in to adjust the view in the image.



Figure 5-2. FFT Showing the Loop-Backed TM3.1a Waveform



Figure 5-3. Zoom of the FFT Showing the Loop-Backed TM3.1a Waveform



A Setting Ethernet Port IP Address

1. Go to "Ethernet" under settings and double click on the "Ethernet" port connected to the Agilex eSOM7.



Figure A-1. Ethernet Settings

2. Under IP settings, click the "Edit" button and select "Manual" on the drop down to set the IP address manually as shown in Figure A-2. After changing the "IP address", "Subnet prefix length", and "Gateway" fields, click "Save".

Manual	~
IPv4	
On On	
P address	
192.168.0.2	
Subnet prefix length	
24	
Gateway 192.168.0.254	
Preferred DNS	
Alternate DNS	
IPv6	

Figure A-2. Manually Setting IP Address



See also Internet Options Windows Defender Firewall

3. After that, open the Control Panel and navigate to "Control Panel\Network and Internet\Network and Sharing Center". Then, click on the connection for the Agilex eSOM7 as shown in Figure A-3.

Network and Sharing Center				- 🗆	×
← → ~ ↑ 🛂 > Control I	Panel > Network and Internet > Network and	Sharing Center 🗸 උ	5		٩
Control Panel Home	View your basic network inform	ation and set up connections			
Change adapter settings	View your active networks				
Change advanced sharing settings	ti.com Domain network	Access type: Internet Connections: USE Ethernet 2			
Media streaming options					
	Unidentified network Public network	Access type: No network access Connections: Up Ethernet			
	Change your networking settings				
	Set up a new connection or new Set up a broadband, dial-up, or	vork VPN connection; or set up a router or access point.			
	Troubleshoot problems Diagnose and repair network pro	oblems or get troubleshooting information.			



4. A window as shown in Figure A-4 will appear. Click the "Properties" button.

Connection		
IPv4 Connectiv	ity:	No network access
IPv6 Connectiv	ity:	No network access
Media State:		Enabled
Duration:		01:13:21
Speed:		1.0 Gbps
the second		
Activity		
Activity	Sent —	Received
ActivityBytes:	Sent — 52,382	Received

Figure A-4. Opening the Properties Tab for the Ethernet Connection



5. After that a window as shown in Figure A-5 will open. Double click the "Internet Protocol Version 4 (TCP/ IPv4)" option to open its "Properties" tab.

letworking Sharing			
Connect using:			
Intel(R) Etheme	et Connection (17) 1219	-LM	
		Con	figure
This connection uses	the following items:		
Clent for Mic Clent for Mic File and Print Clent for Mic	rosoft Networks ter Sharing for Microsof Scheduler ocol Version 4 (TCP/IP twork Adapter Multiple	t Networks /v4) xor Protocol	Î
Internet Proto	DP Protocol Driver ocol Version 6 (TCP/IP	V6)	>
Microsoft LLI Microsoft LLI Internet Proto Install Description	DP Protocol Driver ocol Version 6 (TCP/IP Uninstall	V6) Prop	> perties
Microsoft LLI Microso	DP Protocol Driver ocol Version 6 (TCP/IP Uninstall ol Protocol/Internet Pro protocol that provides rconnected networks.	Prop Prop atocol. The communicat	> perties default tion

Figure A-5. Opening the IPv4 Properties

6. In the window that opens select the "Use the following IP address" option and fill out the fields as shown in Figure A-6. After filling out the fields click ok and the address will be set.

u can get IP settings assigned a s capability. Otherwise, you nee the appropriate IP settings.	Itomatically if your network support d to ask your network administrator	
) Obtain an IP address automat	ically	
Use the following IP address:		
IP address:	192.168.0.2	
Subnet mask:	255.255.255.0	
Default gateway:	192.168.0.254	
Obtain DNS server address au	Itomatically	
Preferred DNS server:	audresses.	
Alternate DNS server:		
Validate settings upon exit		

Figure A-6. Setting the IP Address Manually

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